16-Bit, Voltage-Output Digital-to-Analog Converter

1 FEATURES

- **Full 16-Bit Performance**
- **3 V and 5 V Single-Supply Operation**
- **Low 0.55 mW Power Dissipation**
- **1 µs Settling Time**
- **Unbuffered Voltage Output Capable of Driving 60 kΩ Loads Directly**
- **SPI-/QSPI-/MICROWIRE-Compatible Interface Standards**
- **Power-On Reset Clears DAC Output to 0 V (Unipolar Mode)**
- **6 kV HBM ESD Classification**
- **Low Glitch: 3 nV-sec**

2 APPLICATIONS

- **Digital Gain and Offset Adjustment**
- **Automatic Test Equipment**
- **Data Acquisition Systems**
- **Industrial Process Control**

Functional Block Diagram

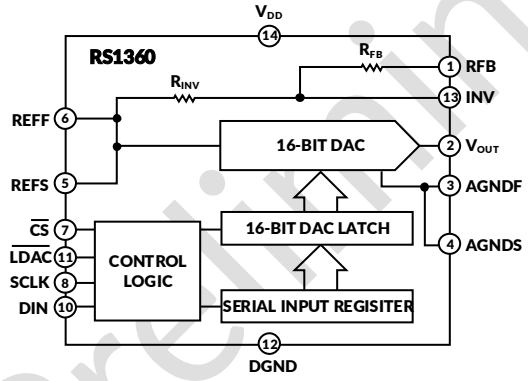


Figure 1. RS1360

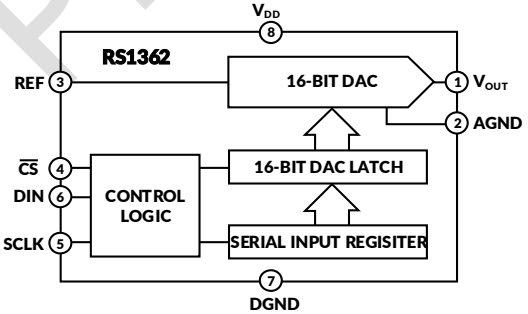


Figure 2. RS1362

3 DESCRIPTIONS

The RS1360/RS1362 are single, 16-bit, serial input, voltage output digital-to-analog converters (DACs) that operate from a single 2.7 V to 5.5 V supply. The DAC output range extends from 0 V to V_{REF}.

The DAC output range extends from 0 V to V_{REF} and is guaranteed monotonic, providing 1 LSB INL accuracy at 16 bits without adjustment over the full specified temperature range of −40°C to +105°C. Offering unbuffered outputs, the RS1360/RS1362 achieves a 1 µs settling time with low power consumption and low offset errors. Providing a low noise performance of 11.8 nV/$\sqrt{\text{Hz}}$ and low glitch, the RS1360/RS1362 is suitable for deployment across multiple end systems.

The RS1360 can be operated in bipolar mode, which generates a ±V_{REF} output swing. The RS1360 also includes Kelvin sense connections for the reference and analog ground pins to reduce layout sensitivity.

The RS1360/RS1362 utilize a versatile 3-wire interface that is compatible with SPI, QSPI™, MICROWIRE™ and DSP Interface standards.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1360	SOP14	8.65mm×3.90mm
RS1362	SOP8	4.90mm×3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 PRODUCT HIGHLIGHTS

1. Single-Supply Operation. The RS1360/RS1362 are fully specified and guaranteed for a single 2.7 V to 5.5 V supply.
2. Low Power Consumption. These parts consume typically 0.55 mW with a 5 V supply and 0.33 mW at 3 V.
3. 3-Wire Serial Interface.
4. Unbuffered Output Capable of Driving 60 kΩ Loads. This reduces power consumption because there is no internal buffer to drive.
5. Power-On Reset Circuitry.

TABLE OF CONTENTS

5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2026/08/13	Preliminary version completed

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS1360	RS1360XP	-40°C ~+105°C	SOP14	RS1360	MSL1	Tape and Reel, 4000
RS1362	RS1362XK	-40°C ~+105°C	SOP8	RS1362	MSL1	Tape and Reel, 4000

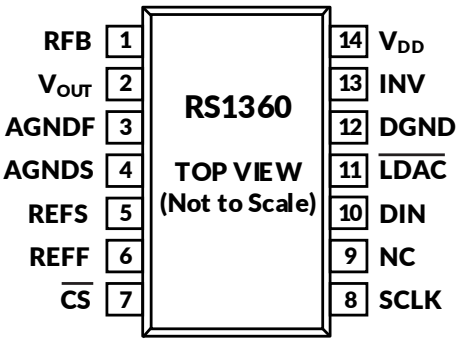
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

7 PIN CONFIGURATION AND FUNCTIONS

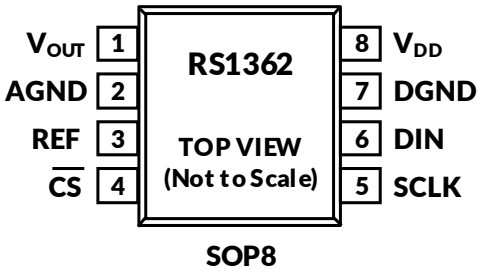


SOP14

PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
RFB	1	Feedback Resistor Pin. In bipolar mode, connect this pin to the external op amp output.
VOUT	2	Analog Output Voltage from the DAC.
AGNDF	3	Ground Reference Point for Analog Circuitry (Force).
AGNDS	4	Ground Reference Point for Analog Circuitry (Sense)
REFS	5	Voltage Reference Input (Sense) for the DAC. Connect to an external 2.5 V reference. Reference can range from 2.5 V to VDD.
REFF	6	Voltage Reference Input (Force) for the DAC. Connect to an external 2.5 V reference. Reference can range from 2.5 V to VDD.
$\overline{CS}$	7	Logic Input Signal. The chip select signal is used to frame the serial data input.
SCLK	8	Clock Input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
NC	9	No Connect.
DIN	10	Serial Data Input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
$\overline{LDAC}$	11	$\overline{LDAC}$ Input. When this input is taken low, the DAC register is simultaneously updated with the contents of the input register
DGND	12	Digital Ground. Ground reference for digital circuitry.
INV	13	Connected to the Internal Scaling Resistors of the DAC. Connect the INV pin to external op amps inverting input in bipolar mode.
VDD	14	Analog Supply Voltage.

PIN CONFIGURATION AND FUNCTIONS



SOP8

PIN FUNCTIONS

PIN		DESCRIPTION
NAME	NO.	
VOUT	1	Analog Output Voltage from the DAC.
AGND	2	Ground Reference Point for Analog Circuitry.
REF	3	Voltage Reference Input for the DAC. Connect to an external 2.5 V reference. Reference can range from 2.5 V to V_{DD}.
$\overline{CS}$	4	Logic Input Signal. The chip select signal is used to frame the serial data input.
SCLK	5	Clock Input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
DIN	6	Serial Data Input. This device accepts 16-bit words. Data is clocked into the input register on the rising edge of SCLK.
DGND	7	Digital Ground. Ground reference for digital circuitry.
VDD	8	Analog Supply Voltage.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	UNIT
V_{DD} to AGND		-0.3	6	V
Digital Input Voltage to DGND		-0.3	V_{DD}+0.3	V
V_{OUT} to AGND		-0.3	V_{DD}+0.3	V
AGND, AGNDF, AGNDS to DGND		-0.3	+0.3	V
Input Current to Any Pin Except Supplies			±10	mA
Operating Temperature Range		-40	105	°C
Storage Temperature Range		-65	150	°C
Maximum Junction Temperature (T_J max) (2)			150	°C
Package Power Dissipation		(T_J max – T_A)/θ_{JA}		
Thermal Impedance, θ_{JA} (3)	SOP8		110	°C/W
	SOP14		105	°C/W

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(3) The package thermal impedance is calculated in accordance with JESD-51.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), JESD22-A114F	±6000	V
		Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2025	±1500	V

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Supply voltage (V_{DD} to GND)	2.7		5.5	V
	Digital input voltage (D_{IN}, SCLK, and $\overline{CS}$)	0		V_{DD}	V
V_{REF}	Reference input voltage	2.5		V_{DD}	V
T_A	Operating ambient temperature	-40		105	°C

8.4 Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V and T_A= –40°C to 105°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE					
Resolution		16			Bits
Relative Accuracy (INL)			±0.5		LSB
Differential Nonlinearity (DNL)			±0.5		LSB
Gain Error	T_A = 25°C		±0.5		LSB
	T_A = -40°C ~105°C		±1		LSB
Gain Error Temperature Coefficient			±0.1		ppm/°C
Unipolar Zero Code Error	T_A = 25°C		±0.5		LSB
	T_A = -40°C ~105°C		±0.5		LSB
Unipolar Zero Code Temperature Coefficient			±0.06		ppm/°C
Bipolar Resistor Matching (1)	R_{FB}/R_{INV}, typically $R_{FB} = R_{INV}$ = 28 kΩ		1		Ω/Ω
	Ratio error		0.07		%
Bipolar Zero offset Error (1)	T_A = 25°C		±1		LSB
	T_A = -40°C ~105°C		±1		LSB
Bipolar Zero Temperature Coefficient (1)			±0.2		ppm/°C
Bipolar Zero Code Offset Error (1)	T_A = 25°C		±3		LSB
	T_A = -40°C ~105°C		±3		LSB
Bipolar Gain Error (1)	T_A = 25°C		±3		LSB
	T_A = -40°C ~105°C		±3		LSB
Bipolar Gain Temperature Coefficient (1)			±0.2		ppm/°C
OUTPUT CHARACTERISTICS					
Output Voltage Range	Unipolar operation	0		V_{REF}-1LSB	V
	bipolar operation (1)	$-V_{REF}$		$+V_{REF}$-1LSB	
Output Voltage Settling Time	To 1/2 LSB of FSR, C_L= 10 pF		1		µs
Slew Rate	C_L=10pF, measured from 0% to 63%		17		V/µs
Digital-to-Analog Glitch Impulse	1 LSB change around the major carry		3		nV-sec
Digital Feedthrough			0.3		nV-sec
DAC Output Impedance	Tolerance typically 20%		6.25		kΩ
Output Noise Spectral Density	DAC code = 0x8400, frequency = 1 kHz		11.8		$nV/\sqrt{Hz}$
Output Noise	0.1 Hz to 10 Hz		0.134		µVp-p
Power Supply Rejection Ratio	ΔV_{DD}±10%		±0.25		LSB

Electrical Characteristics (continued)

V_{DD} = 2.7 V to 5.5 V and T_A= –40°C to 105°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC REFERENCE INPUT						
Reference Input Range			2.5		V_{DD}	V
Reference Input Resistance		Unipolar operation	9			kΩ
		bipolar operation (1)	7.5			kΩ
LOGIC INPUTS						
Input Current					±1	µA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.4			V
Input Capacitance (2)					10	pF
Hysteresis Voltage				0.15		V
REFERENCE (3)						
Reference -3dB Bandwidth		All 1s loaded		1		MHz
Reference Feedthrough		All 0s loaded, V_{REF}= 1Vp-p at 100kHz		1		mVp-p
Signal-to-Noise Ratio				92		dB
Reference Input Capacitance		Code 0x0000		26		pF
		Code 0xFFFF		26		pF
POWER REQUIREMENTS						
V_{DD}			2.7		5.5	V
I_{DD}				110		µA
Power Dissipation				0.55		mW

(1) 1360 only.
(2) Reference input resistance is code-dependent, minimum at 0x8555.
(3) Guaranteed by design, not subject to production test.

8.5 Timing Characteristics

V_{DD} = 2.7 V to 5.5 V ±10%, V_{REF} = 2.5 V, V_{IH} = 3 V and 90% of V_{DD}, V_{IL} = 0 V and 10% of V_{DD}, AGND = DGND = 0 V; −40°C < T_A <+105°C, unless otherwise noted.

PARAMETER (1) (2)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK cycle frequency				25	MHz
t_1	SCLK cycle time		40			ns
t_2	SCLK HIGH time		20			ns
t_3	SCLK LOW time		20			ns
t_4	$\overline{CS}$ low to SCLK high setup		10			ns
t_5	$\overline{CS}$ high to SCLK high setup		15			ns
t_6	SCLK high to $\overline{CS}$ low hold time		30			ns
t_7	SCLK high to $\overline{CS}$ high hold time		20			ns
t_8	Data setup time		15			ns
t_9	Data hold time (V_{IH} = 90% of V_{DD}, V_{IL} = 10% of V_{DD})		4			ns
t_9	Data hold time (V_{IH} = 3V, V_{IL} = 0V)		7.5			ns
t_{10}	$\overline{LDAC}$ pulse width		30			ns
t_{11}	$\overline{CS}$ high to $\overline{LDAC}$ low setup		30			ns
t_{12}	$\overline{CS}$ high time between active periods		30			ns

(1) Guaranteed by design and characterization. Not production tested.
(2) All input signals are specified with t_R = t_F = 1 ns/V and timed from a voltage level of (V_{IL} + V_{IH})/2.

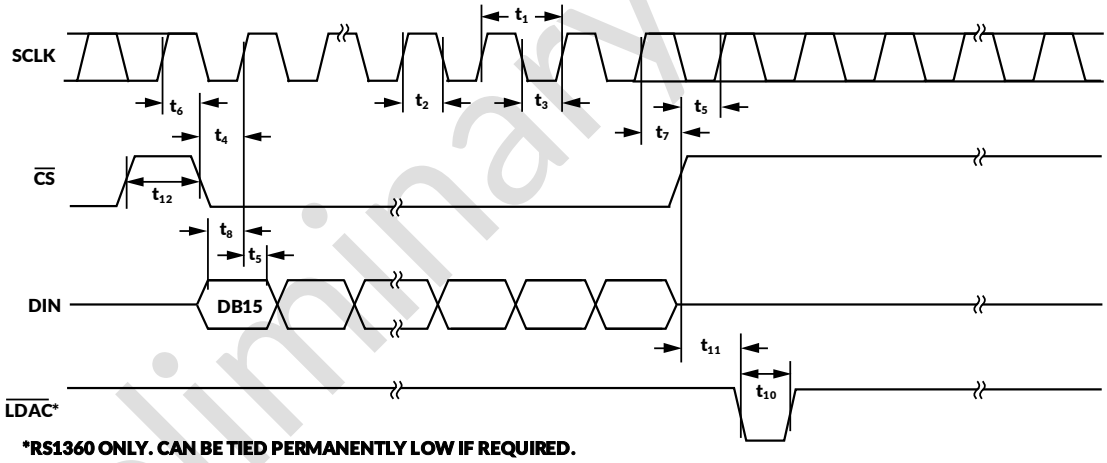


Figure 3. Timing Diagram

8.6 Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{DD} = 2.7 V, V_{REF} = 2.5 V, T_A = 25°C (unless otherwise noted).

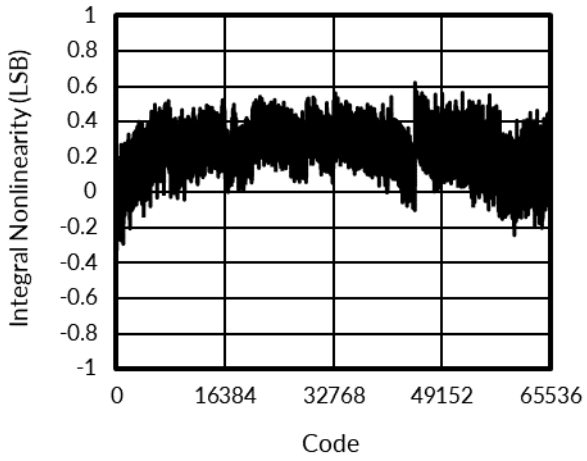


Figure 4. Integral Nonlinearity vs Code

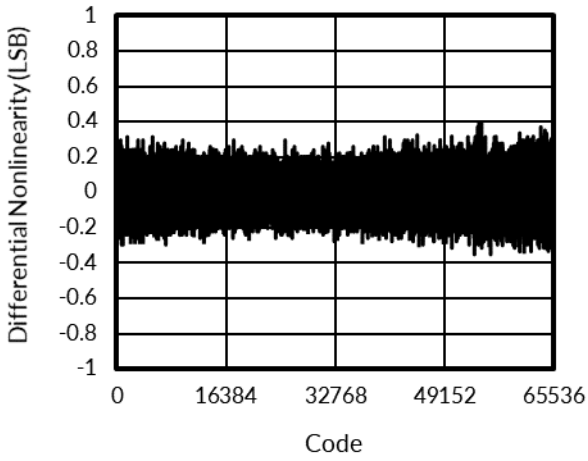


Figure 5. Differential Nonlinearity vs Code

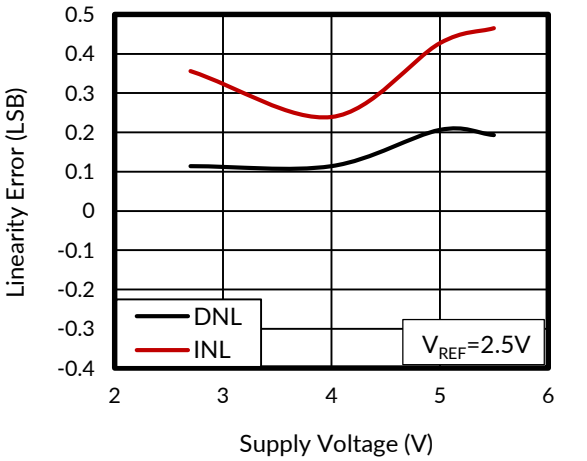


Figure 6. Linearity Error vs Supply Voltage

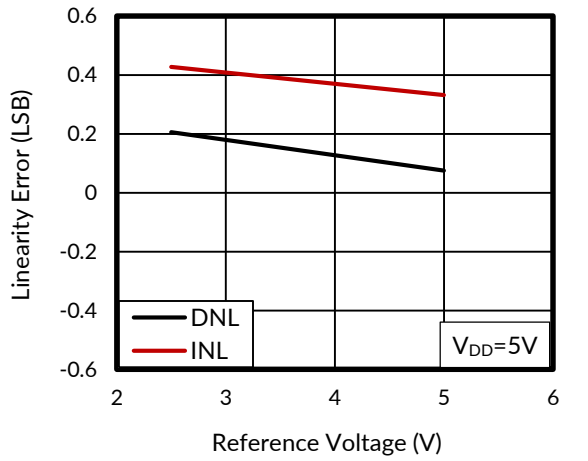


Figure 7. Linearity Error vs Reference Voltage

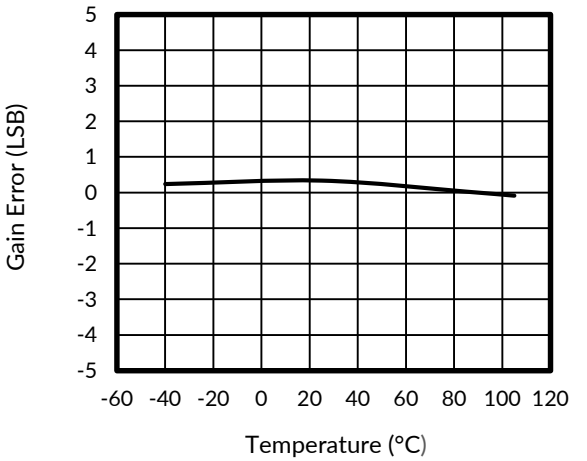


Figure 8. Gain Error vs Temperature

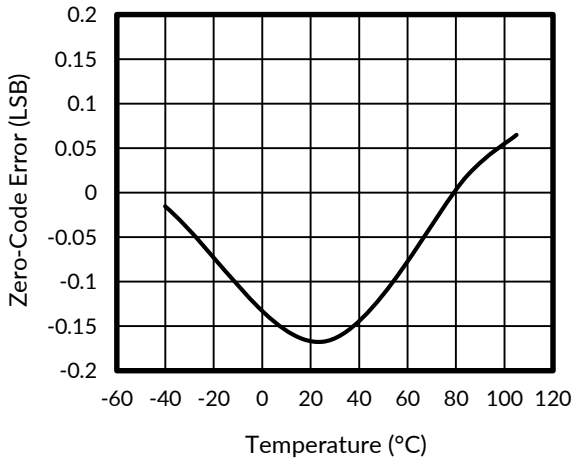


Figure 9. Zero-Code Error vs Temperature

Typical Performance Characteristics(continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{DD} = 2.7 V, V_{REF} = 2.5 V, T_A = 25°C (unless otherwise noted).

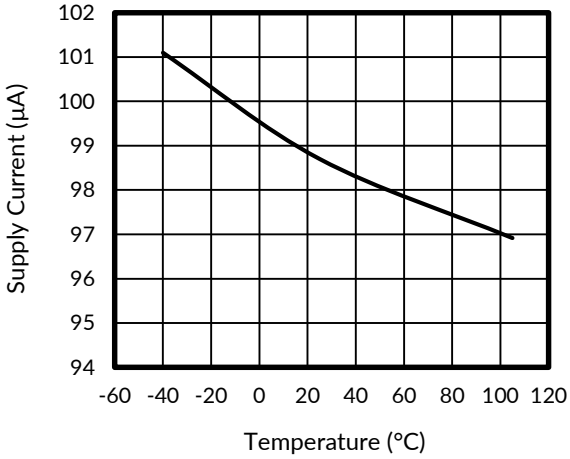


Figure 10. Supply Current vs Temperature

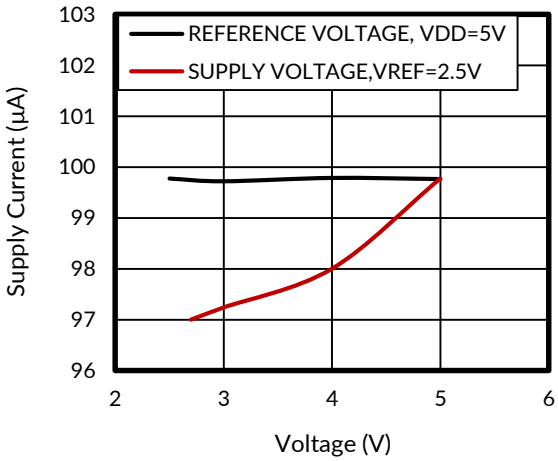


Figure 11. Supply Current vs Reference Voltage or Supply Voltage

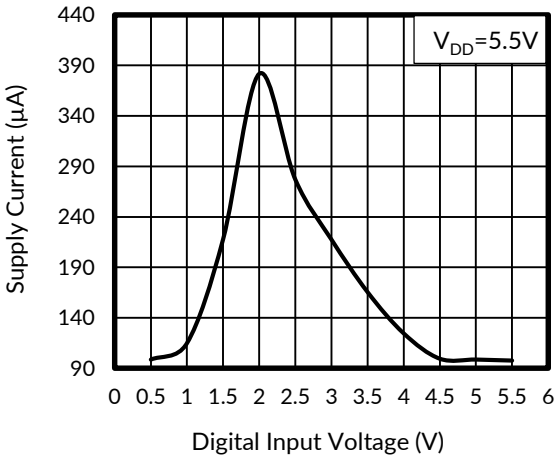


Figure 12. Supply Current vs Digital Input Voltage

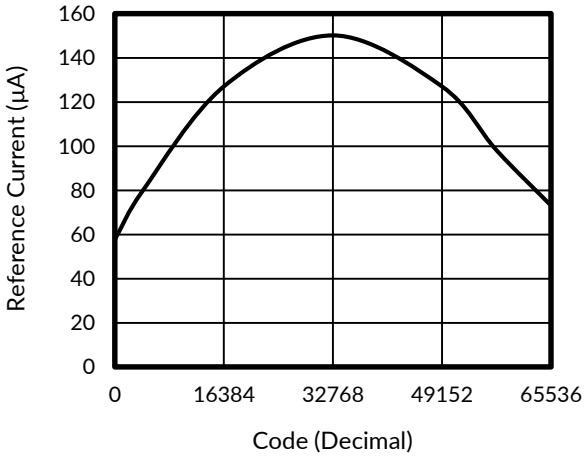


Figure 13. Reference Current vs Code

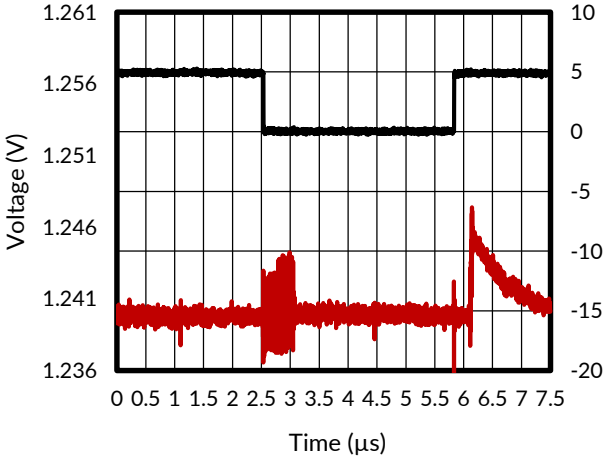


Figure 14. Digital Feedthrough

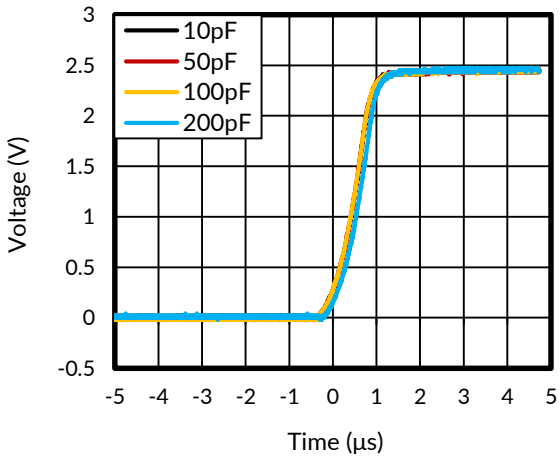


Figure 15. Large Signal Settling Time

Typical Performance Characteristics(continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{DD} = 2.7 V, V_{REF} = 2.5 V, T_A = 25°C (unless otherwise noted).

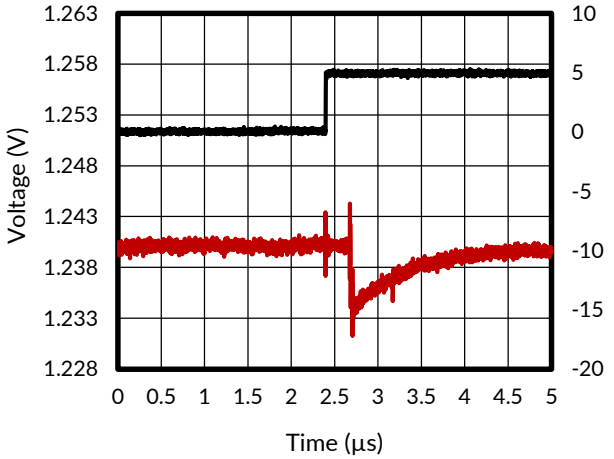


Figure 16. Digital-to-Analog Glitch Impulse

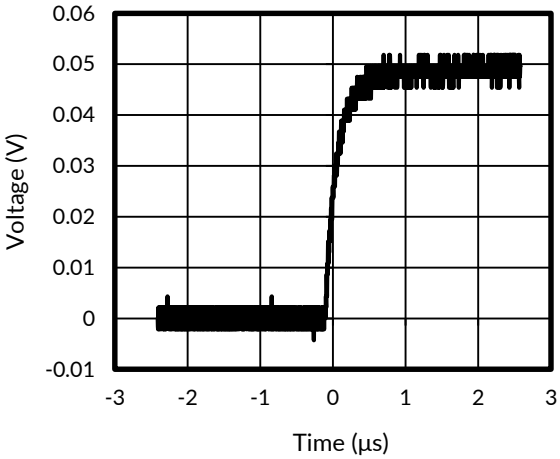


Figure 17. Small Signal Settling Time

9 TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy or INL is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs code plot can be seen in Figure 4.

Differential Nonlinearity (DNL)
DNL is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. Figure 5 illustrates a typical DNL vs code plot.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Gain Error Temperature Coefficient
Gain error temperature coefficient is a measure of the change in gain error with changes in temperature. It is expressed in ppm/°C.

Zero Code Error
Zero code error is a measure of the output error when zero code is loaded to the DAC register.

Zero Code Temperature Coefficient
This is a measure of the change in zero code error with a change in temperature. It is expressed in mV/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition. A plot of the digital-to analog glitch impulse is shown in Figure 16.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. $\overline{CS}$ is held high while the CLK and DIN signals are toggled. It is specified in nV-sec and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa. A typical plot of digital feedthrough is shown in Figure 14.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage. Power-supply rejection ratio is quoted in terms of percent change in output per percent change in V_{DD} for full-scale output of the DAC. V_{DD} is varied by ±10%.

Reference Feedthrough
Reference feedthrough is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100 kHz, 1 Vp-p is applied to V_{REF}. Reference feedthrough is expressed in mVp-p.

10 THEORY OF OPERATION

The RS1360/RS1362 is single, 16-bit, serial input, voltage output DACs. They operate from a single supply ranging from 2.7 V to 5.5 V and consume typically 110μA with a supply of 5 V. Data is written to these devices in a 16-bit word format, via a 3- or 4-wire serial interface. To ensure a known power-up state, these parts are designed with a power-on reset function. In unipolar mode, the output is reset to 0 V; in bipolar mode, the RS1360 output is set to $-V_{REF}$. Kelvin sense connections for the reference and analog ground are included on the RS1360.

10.1 Digital-to-Analog Section

The DAC architecture consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 18. The DAC architecture of the RS1360/RS1362 is segmented. The four MSBs of the 16-bit data-word are decoded to drive 15 switches, E1 to E15. Each switch connects one of 15 matched resistors to either AGND or V_{REF}. The remaining 12 bits of the data-word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

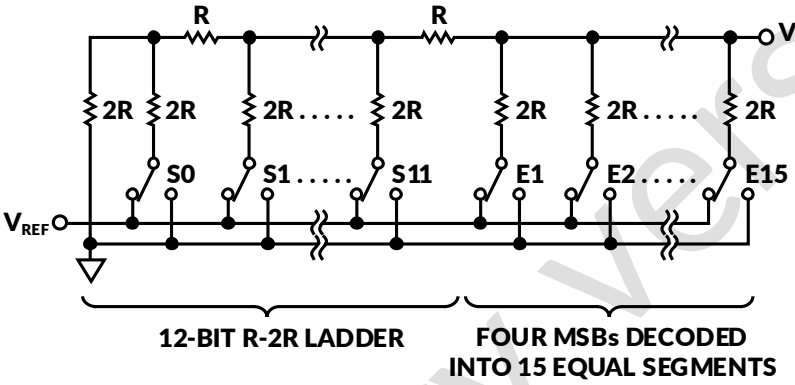


Figure 18. DAC Architecture

With this type of DAC configuration, the output impedance is independent of code, while the input impedance seen by the reference is heavily code dependent. The output voltage is dependent on the reference voltage, as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} * D}{2^N}$$

where:
D is the decimal data-word loaded to the DAC register.
N is the resolution of the DAC.
For a reference of 2.5 V, the equation simplifies to the following:

$$V_{OUT} = \frac{2.5 * D}{65536}$$

This gives a V_{OUT} of 1.25 V with midscale loaded and 2.5 V with full-scale loaded to the DAC.
The LSB size is V_{REF} /65,536.

10.2 Serial Interface

The RS1360/RS1362 is controlled by a versatile 3- or 4-wire serial interface that operates at clock rates up to 25 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. The timing diagram is shown in Figure 3. Input data is framed by the chip select input, $\overline{CS}$. After a high-to-low transition on $\overline{CS}$, data is shifted synchronously and latched into the input register on the rising edge of the serial clock, SCLK. Data is loaded MSB first in 16-bit words. After 16 data bits have been loaded into the serial input register, a low-to-high transition on $\overline{CS}$ transfers the contents of the shift register to the DAC. Data can be loaded to the part only while $\overline{CS}$ is low. The RS1360 has an $\overline{LDAC}$ function that allows the DAC latch to be updated asynchronously by bringing $\overline{LDAC}$ low after $\overline{CS}$ goes high. $\overline{LDAC}$ should be maintained high while data is written to the shift register. Alternatively, $\overline{LDAC}$ can be tied permanently low to update the DAC synchronously. With $\overline{LDAC}$ tied permanently low, the rising edge of $\overline{CS}$ loads the data to the DAC.

10.3 Unipolar Output Operation

These DACs are capable of driving unbuffered loads of 60 kΩ. The RS1362 provides a unipolar output swing ranging from 0 V to V_{REF}. The RS1360 can be configured to output both unipolar and bipolar voltages. Figure 19 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table 1.

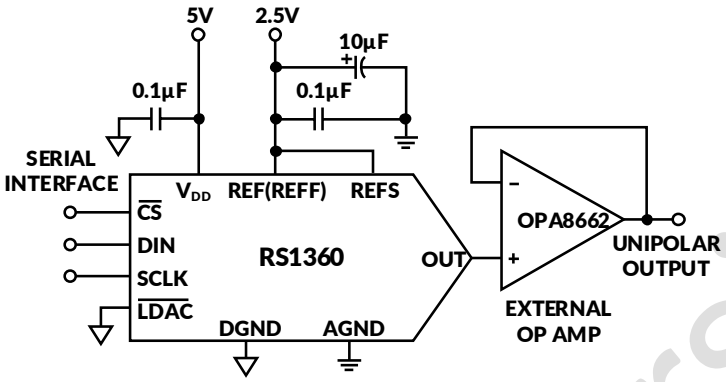


Figure 19. Unipolar Output

Table 1. Unipolar Code Table

DAC Latch Contents	Analog Output
MSB LSB	
1111 1111 1111 1111	V_{REF}*(65535/65536)
1000 0000 0000 0000	V_{REF}*(32768/65536)=1/2V_{REF}
0000 0000 0000 0001	V_{REF}*(1/65536)
0000 0000 0000 0000	0V

Assuming a perfect reference, the unipolar worst-case output voltage can be calculated from the following equation:

$$V_{OUT.UNI} = \frac{D}{2^{16}} * (V_{REF} + V_{GE}) + V_{ZSE} + INL$$

where:
$V_{OUT-UNI}$ is unipolar mode worst-case output.
D is code loaded to DAC.
V_{REF} is reference voltage applied to the part.
V_{GE} is gain error in volts.
V_{ZSE} is zero scale error in volts.
INL is integral nonlinearity in volts.

10.4 Bipolar Output Operation

With the aid of an external op amp, the RS1360 can be configured to provide a bipolar voltage output. A typical circuit of such operation is shown in Figure 20. The matched bipolar offset resistors, R_{FB} and R_{INV}, are connected to an external op amp to achieve this bipolar output swing, typically R_{FB} = R_{INV} = 28 kΩ. Table 2 shows the transfer function for this output operating mode. Also provided on the RS1360 are a set of Kelvin connections to the analog ground inputs.

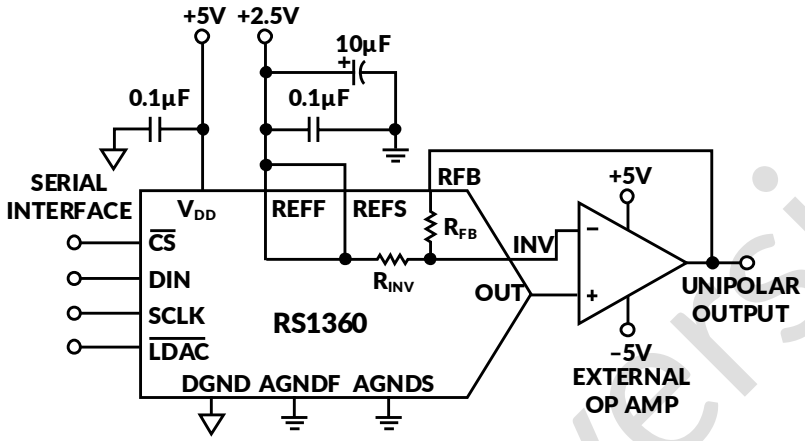


Figure 20. Bipolar Output (RS1360 Only)

Table 2. Bipolar Code Table

DAC Latch Contents	Analog Output
MSB LSB	
1111 1111 1111 1111	$+V_{REF}$ * (32767/32768)
1000 0000 0000 0001	$+V_{REF}$ * (1/32768)
1000 0000 0000 0000	0V
0111 1111 1111 1111	$-V_{REF}$ * (1/32768)
0000 0000 0000 0000	$-V_{REF}$ * (32768/32768)=$-V_{REF}$

Assuming a perfect reference, the worst-case bipolar output voltage can be calculated from the following equation:

$$V_{OUT-BIP} = \frac{[(V_{OUT-UNI} + V_{OS})(2 + RD) - V_{REF}(1 + RD)]}{1 + (2 + RD)/A}$$

where:
$V_{OUT-BIP}$ is the bipolar mode worst-case output.
$V_{OUT-UNI}$ is the unipolar mode worst-case output.
V_{OS} is the external op amp input offset voltage.
RD is the R_{FB} and R_{INV} resistor matching error.
A is the op amp open-loop gain.

10.5 Output Amplifier Selection

For bipolar mode, a precision amplifier should be used and supplied from a dual power supply. This provides the ±V_{REF} output. In a single-supply application, selection of a suitable op amp may be more difficult as the output swing of the amplifier does not usually include the negative rail, in this case, AGND. This can result in some degradation of the specified performance unless the application does not use codes near zero.

The selected op amp needs to have a very low-offset voltage (the DAC LSB is 38 µV with a 2.5 V reference) to eliminate the need for output offset trims. Input bias current should also be very low because the bias current, multiplied by the DAC output impedance (approximately 6 kΩ), adds to the zero code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the op amp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code-independent, but to minimize gain errors, the input

impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, hence increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a shorter effective settling time of the combined DAC and amplifier.

10.6 Force Sense Amplifier Selection

Use single-supply, low-noise amplifiers. A low-output impedance at high frequencies is preferred because the amplifiers need to be able to handle dynamic currents of up to ±20 mA.

10.7 Reference And Ground

Because the input impedance is code-dependent, the reference pin should be driven from a low impedance source. The RS1360 operate with a voltage reference ranging from 2.5 V to V_{DD}. References below 2.5 V result in reduced accuracy. The full scale output voltage of the DAC is determined by the reference. Table 1 and Table 2 outline the analog output voltage or particular digital codes. For optimum performance, Kelvin sense connections are provided on the RS1360. If the application does not require separate force and sense lines, tie the lines close to the package to minimize voltage drops between the package leads and the internal die.

10.8 Power-On Reset

The RS1360/RS1362 have a power-on reset function to ensure that the output is at a known state on power-up. On power-up, the DAC register contains all 0s until the data is loaded from the serial register. However, the serial register is not cleared on power-up, so its contents are undefined. When loading data initially to the DAC, 16 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 16 bits are loaded, the last 16 are kept, and if less than 16 bits are loaded, bits remain from the previous word. If the RS1360 need to be interfaced with data shorter than 16 bits, the data should be padded with 0s at the LSBs.

10.9 Power Supply And Reference Bypassing

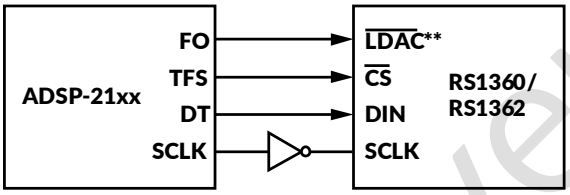
For accurate high-resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor.

11 MICROPROCESSOR INTERFACING

Microprocessor interfacing to the RS1360 is via a serial bus that uses standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 3- or 4-wire interface consisting of a clock signal, a data signal and a synchronization signal. The RS1360 require a 16-bit data-word with data valid on the rising edge of SCLK. The DAC update can be done automatically when all the data is clocked in or it can be done under control of the $\overline{\text{LDAC}}$.

11.1 RS1360 to ADSP-21XX Interface

Figure 21 shows a serial interface between the RS1360 and the ADSP-21xx. The ADSP-21xx should be set to operate in the SPORT transmit alternate framing mode. The ADSP-21xx are programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out on each rising edge of the serial clock, an inverter is required between the DSP and the DAC, because the RS1360 clock data in on the falling edge of the SCLK.

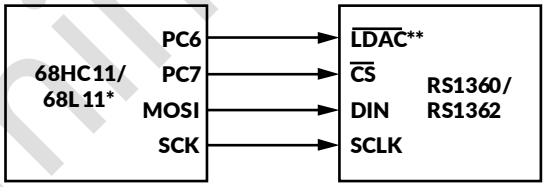


*ADDITIONAL PINS OMITTED FOR CLARITY.
**RS1360 ONLY

Figure 21. RS1360/RS1362 to ADSP-21xx Interface

11.2 RS1360 to 68HC11/68L11 Interface

Figure 22 shows a serial interface between the RS1360 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/ 68L11 drives the SCLK of the DAC, and the MOSI output drives the serial data line serial DIN. The $\overline{\text{CS}}$ signal is driven from one of the port lines. The 68HC11/68L11 is configured for master mode: MSTR = 1, CPOL = 0, and CPHA = 0. Data appearing on the MOSI output is valid on the rising edge of SCK.

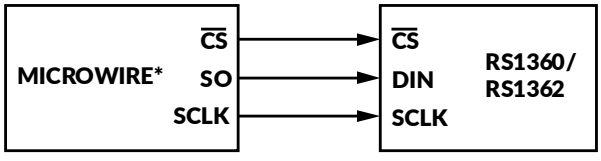


*ADDITIONAL PINS OMITTED FOR CLARITY.
**RS1360 ONLY

Figure 22. RS1360/RS1362 to 68HC11/68L11 Interface

11.3 RS1360 to MICROWIRE Interface

Figure 23 shows an interface between the RS1360 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and into the RS1360 on the rising edge of the serial clock. No glue logic is required because the DAC clocks data into the input shift register on the rising edge.



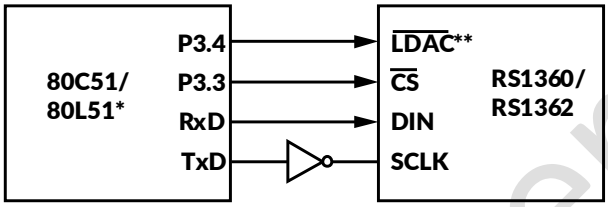
*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 23. RS1360/RS1362 to MICROWIRE Interface

11.4 RS1360 to 80C51/80L51 Interface

A serial interface between the RS1360 and the 80C51/ 80L51 microcontroller is shown in Figure 24. TxD of the micro controller drives the SCLK of the RS1360, and RxD drives the serial data line of the DAC. P3.3 is a bit programmable pin on the serial port that is used to drive $\overline{CS}$.

The 80C51/80L51 provide the LSB first, whereas the RS1360 expects the MSB of the 16-bit word first. Care should be taken to ensure the transmit routine takes this into account. When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is valid on the falling edge of TxD, so the clock must be inverted as the DAC clocks data into the input shift register on the rising edge of the serial clock. The 80C51/80L51 transmit data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. As the DAC requires a 16-bit word, P3.3 must be left low after the first eight bits are transferred, and brought high after the second byte is transferred. $\overline{LDAC}$ on the RS1360 can also be controlled by the 80C51/ 80L51 serial port output by using another bit programmable pin, P3.4.



*ADDITIONAL PINS OMITTED FOR CLARITY.

**RS1360 ONLY

Figure 24. RS1360/RS1362 to 80C51/80L51 Interface

12 APPLICATIONS INFORMATION

12.1 Optocoupler Interface

The digital inputs of the RS1360 is Schmitt-triggered so that they can accept slow transitions on the digital input lines. This makes these parts ideal for industrial applications where it may be necessary to isolate the DAC from the controller via optocouplers. Figure 25 illustrates such an interface.

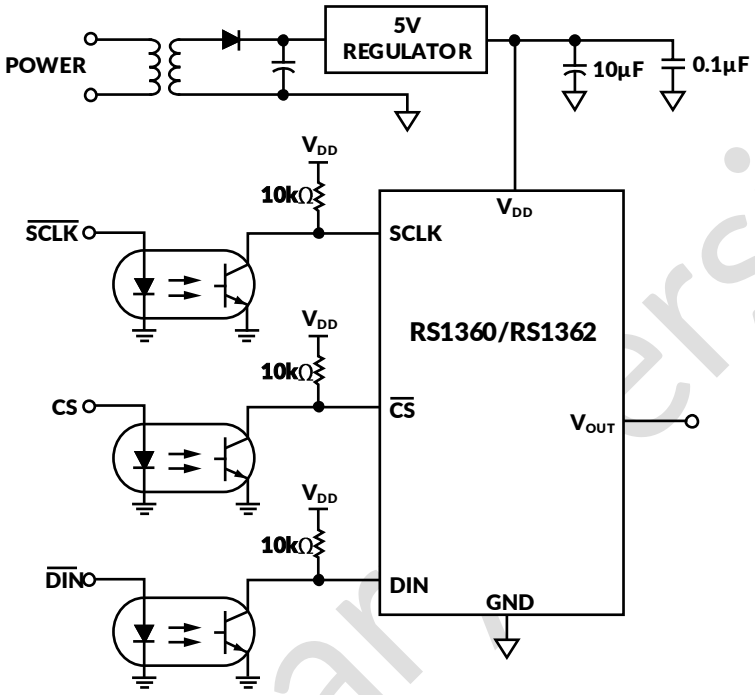


Figure 25. RS1360/RS1362 in an Optocoupler interface

12.2 Decoding Multiple RS1360

The $\overline{CS}$ pin of the RS1360 can be used to select one of a number of DACs. All devices receive the same serial clock and serial data, but only one device receives the CS signal at any one time. The DAC addressed is determined by the decoder. There is some digital feedthrough from the digital input lines. Using a burst clock minimizes the effects of digital feedthrough on the analog signal channels. Figure 26 shows a typical circuit.

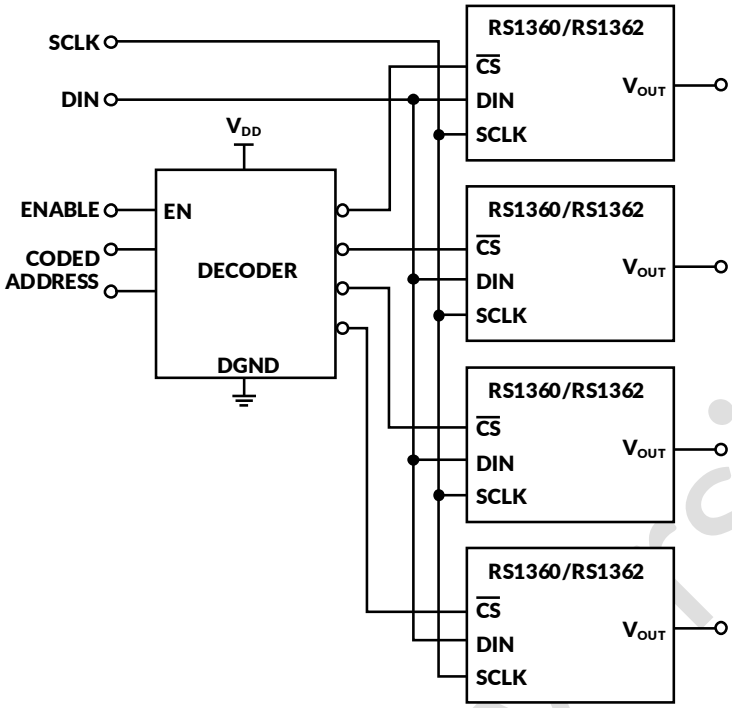
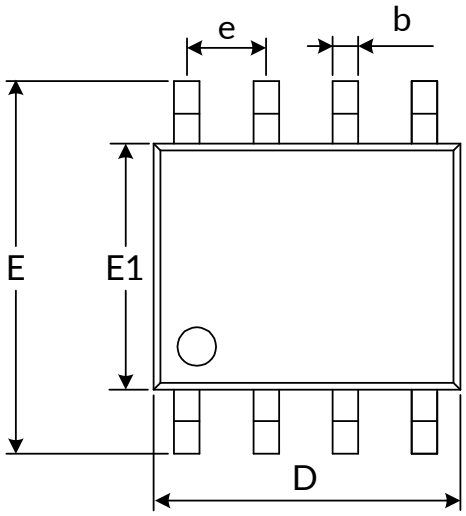
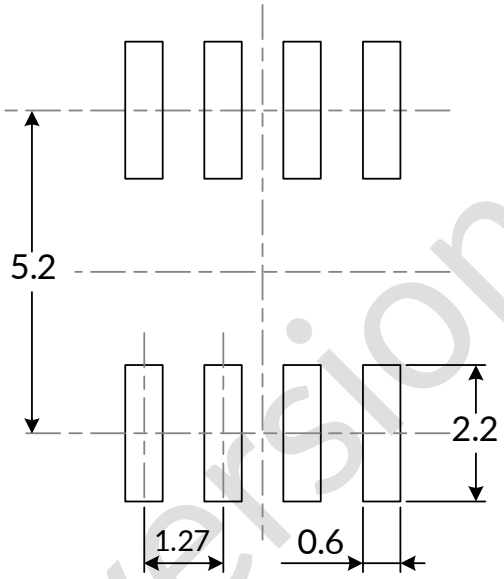


Figure 26. Addressing Multiple RS1360/RS1362

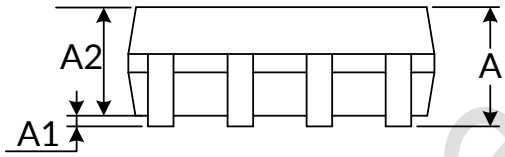
13 PACKAGE OUTLINE DIMENSIONS

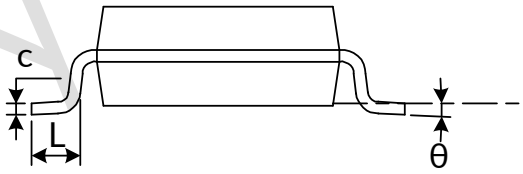
SOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



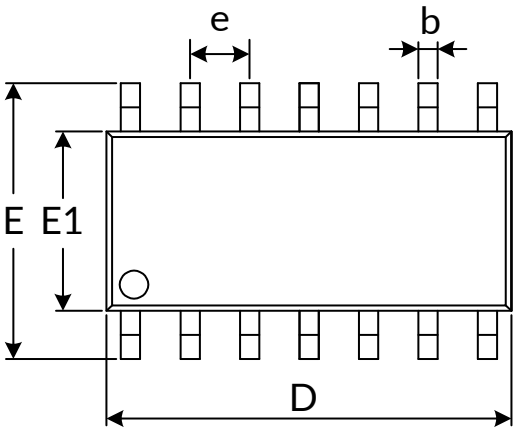


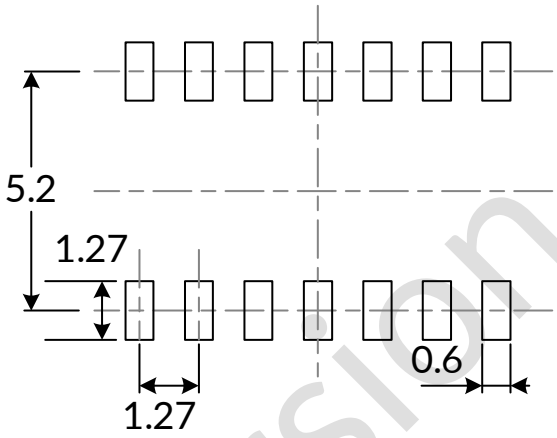
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A(1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D(1)	4.800	5.000	0.189	0.197
e	1.270(BSC)(2)		0.050(BSC)(2)	
E	5.800	6.200	0.228	0.244
E1(1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

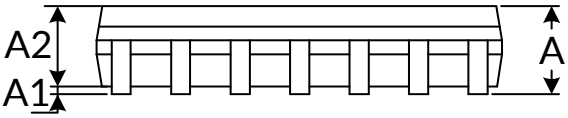
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers),"Basic" spacing is nominal.
3. This drawing is subject to change without notice.

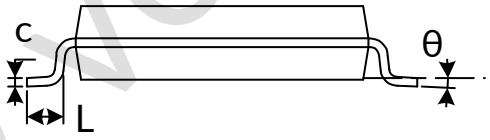
SOP14 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A(1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D(1)	8.450	8.850	0.333	0.348
e	1.270(BSC)(2)		0.050(BSC)(2)	
E	5.800	6.200	0.228	0.244
E1(1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

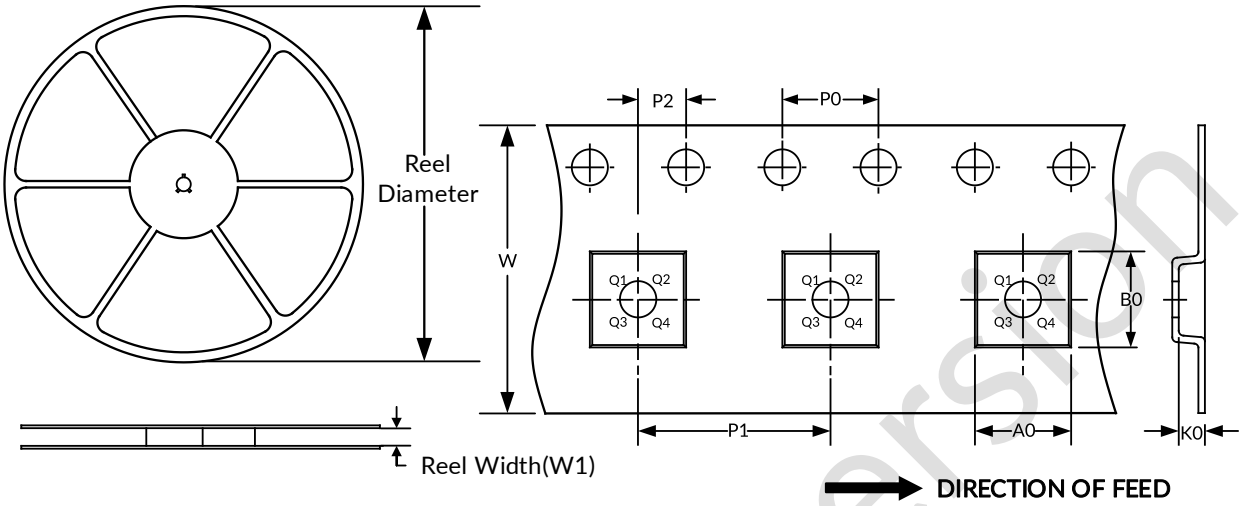
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers),"Basic" spacing is nominal.
3. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOP8	13”	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
SOP14	13”	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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