

250mA, Low Power Consumption, High Voltage CMOS LDO Regulator

1 FEATURES

- **Input Voltage Range: 2.5 V to 36 V**
- **Output Voltage Range:**
 - Fixed Option: 3V, 3.3V, 3.6V, 5V, 9V and 12V
 - Adjustable Option: 1.0 V to 12 V
- **Very low I_Q: 1.9μA (TYP)**
- **Up to 250mA Load Current**
- **Low Dropout Voltage**
- **Low Temperature Coefficient**
- **Over Temperature Protection**
- **Over Current Limit Protection**
- **Short Circuit Protection is Typical 40mA**
- **Output Voltage Accuracy: ±1%**
- **SOT23-3, SOT23-5, SOT89-3 and UDFN1.6X1.6-6 Packages**

3 DESCRIPTIONS

The RS75XX-2H series are a group of positive voltage regulators manufactured by CMOS technologies with low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small. The RS75XX-2H series can deliver 250mA output current and allow an input voltage as high as 36V. The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

The RS75XX-2H is available in Green SOT23-3, SOT23-5, SOT89-3 and UDFN1.6X1.6-6 variety of packages, for the different application's requirements.

2 APPLICATIONS

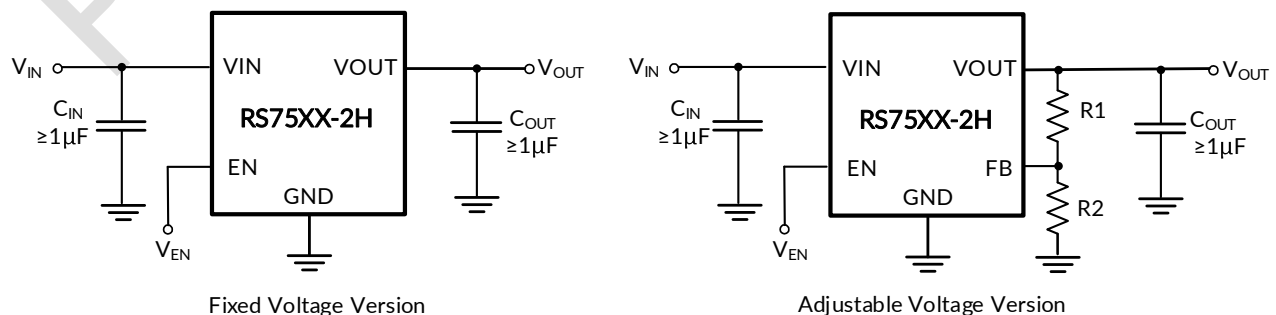
- **Smart Power Network Equipment**
- **Portable Power Tools**
- **BMS Systems**
- **Motor Control System/Industrial Control System**
- **Power Meter/Instrument**
- **White Goods**
- **Vehicle-Mounted System**
- **Battery-Powered Equipment**
- **Automotive Head Unit**
- **Security Equipment**
- **Communication Equipment**

Device Information ⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS75XX-2H	SOT23-3	1.60mm×2.92mm
	SOT23-5	1.60mm×2.92mm
	SOT89-3	2.45mm×4.50mm
	UDFN1.6X1.6-6	1.60mm×1.60mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 TYPICAL APPLICATION SCHEMATIC



5 FUNCTIONAL BLOCK DIAGRAM

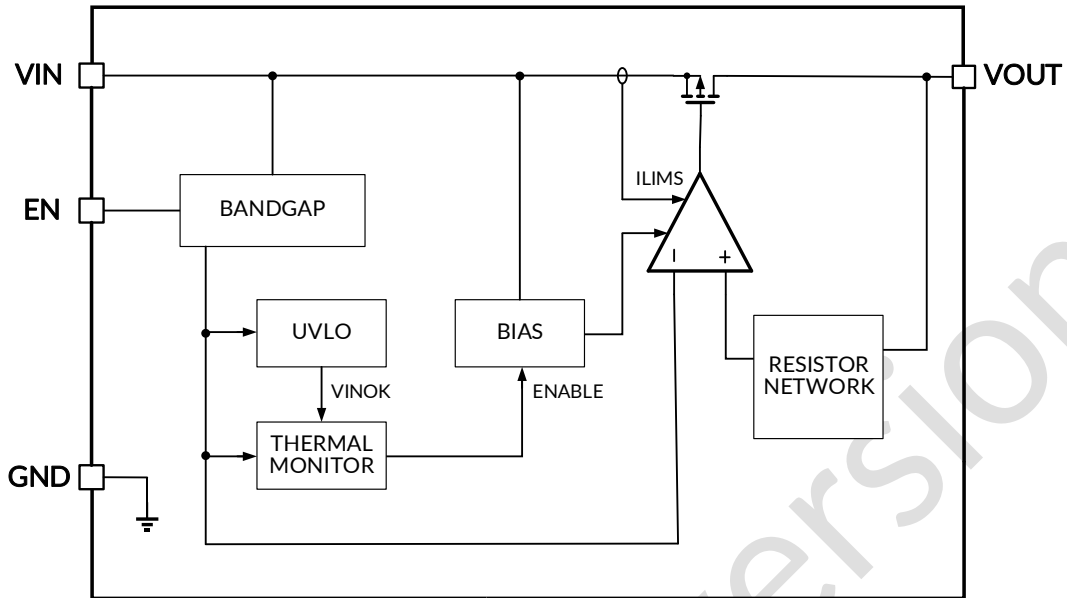


Figure 1. Fixed Voltage Version

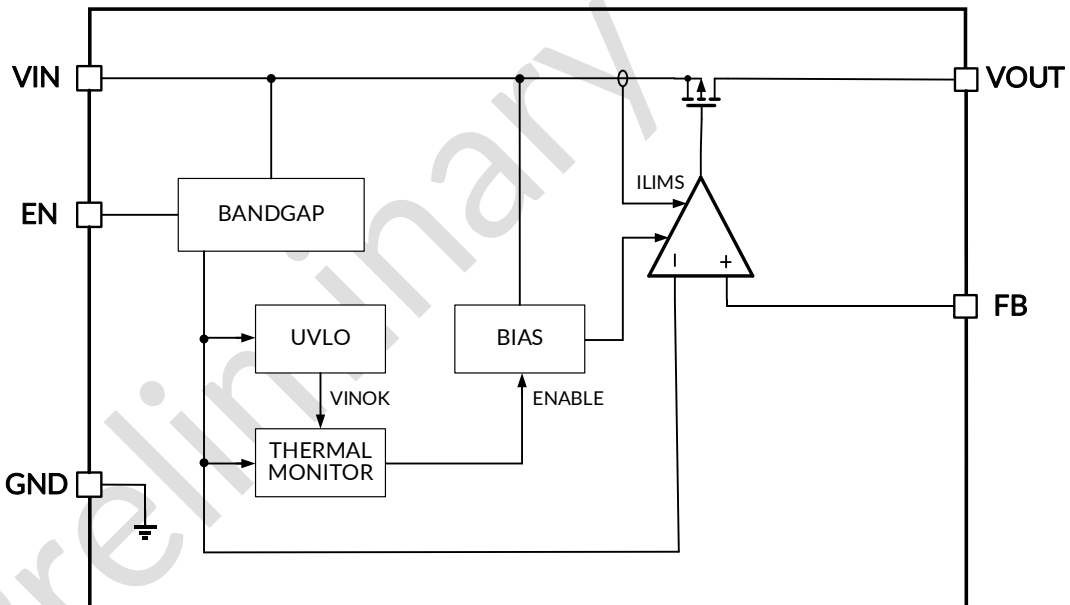


Figure 2. Adjustable Voltage Version

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6 REVISION HISTORY

Note: Page numbers for previous revisions may differ from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2025/09/08	Preliminary version completed
A.0.1	2025/11/06	1. Update PACKAGE/ORDERING INFORMATION 2. Update Electrical Characteristics
A.0.2	2026/03/03	Update SPECIFICATIONS
A.0.3	2026/06/04	Add the θ_{JA} values for SOT23-3 and SOT23-5 packages in Absolute Maximum Ratings

Preliminary version

7 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER (2)	V _{OUT} (V)	PACKAGE LEAD	PACKAGE MARKING (3)	MSL (4)	PACKAGE OPTION
RS7530-2H	RS7530-2HXF3	3.0	SOT23-3	SH30	MSL3	Tape and Reel, 3000
	RS7530-2HXE3	3.0	SOT89-3	SH30	MSL3	Tape and Reel, 1000
	RS7530-2HXE3L	3.0	SOT89-3(L-Type)	SH30L	MSL3	Tape and Reel, 1000
	RS7530-2HXS F5	3.0	SOT23-5(S-Type)	SH30S	MSL3	Tape and Reel, 3000
RS7533-2H	RS7533-2HXF3	3.3	SOT23-3	SH33	MSL3	Tape and Reel, 3000
	RS7533-2HXE3	3.3	SOT89-3	SH33	MSL3	Tape and Reel, 1000
	RS7533-2HXE3L	3.3	SOT89-3(L-Type)	SH33L	MSL3	Tape and Reel, 1000
	RS7533-2HXS F5	3.3	SOT23-5(S-Type)	SH33S	MSL3	Tape and Reel, 3000
	RS7533-2HXF5	3.3	SOT23-5	SH33	MSL3	Tape and Reel, 3000
	RS7533-2HXUTDL6	3.3	UDFN1.6X1.6-6	SH33	MSL3	Tape and Reel, 3000
RS7536-2H	RS7536-2HXS F5	3.6	SOT23-5(S-Type)	SH36S	MSL3	Tape and Reel, 3000
RS7550-2H	RS7550-2HXF3	5.0	SOT23-3	SH50	MSL3	Tape and Reel, 3000
	RS7550-2HXE3	5.0	SOT89-3	SH50	MSL3	Tape and Reel, 1000
	RS7550-2HXE3L	5.0	SOT89-3(L-Type)	SH50L	MSL3	Tape and Reel, 1000
	RS7550-2HXS F5	5.0	SOT23-5(S-Type)	SH50S	MSL3	Tape and Reel, 3000
	RS7550-2HXF5	5.0	SOT23-5	SH50	MSL3	Tape and Reel, 3000
	RS7550-2HXUTDL6	5.0	UDFN1.6X1.6-6	SH50	MSL3	Tape and Reel, 3000
RS7590-2H	RS7590-2HXF3	9.0	SOT23-3	SH90	MSL3	Tape and Reel, 3000
RS7512-2H	RS7512-2HXE3	12.0	SOT89-3	SH12	MSL3	Tape and Reel, 1000
RS75ADJ-2H	RS75ADJ-2HXS F5	ADJ	SOT23-5(S-Type)	SHADJ	MSL3	Tape and Reel, 3000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) RS75□□-2HX□□

→ **Package Type**

F3: SOT23-3
 F5: SOT23-5
 SF5: SOT23-5 (S-Type)
 E3: SOT89-3
 E3L: SOT89-3 (L-Type)
 UTDL6: UDFN1.6X1.6-6

→ **Output Voltage**

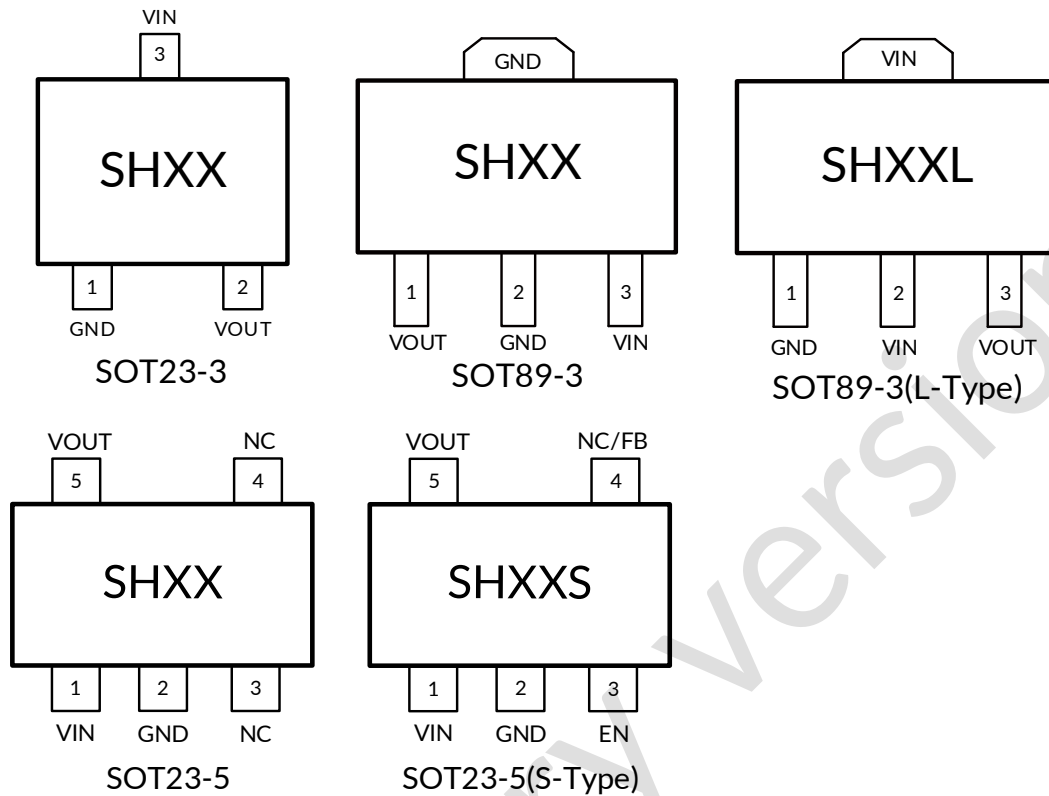
30: 3.0V
 33: 3.3V
 36: 3.6V
 50: 5.0V
 90: 9.0V
 12: 12.0V
 ADJ: Adjustable Output from 1.0V to 12V

*Special Request: Any Voltage between 1.8V and 12V under specific business agreement

(3) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(4) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

8 PIN CONFIGURATION AND FUNCTIONS



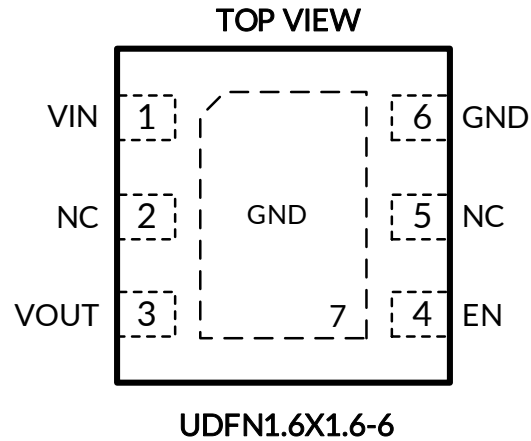
NOTE: XX indicate Output Voltage, xx indicate Date Code
For example: SH33 (V_{OUT}=3.3V)

PIN DESCRIPTION

NAME	PIN					I/O ⁽¹⁾	FUNCTION
	SOT23-3	SOT89-3	SOT89-3 (L-Type)	SOT23-5	SOT23-5 (S-Type)		
GND	1	2	1	2	2	G	Ground
VOUT	2	1	3	5	5	O	Regulated output voltage. Connect a minimum 1μF low-ESR capacitor to this pin.
VIN	3	3	2	1	1	I	Input voltage supply. Must be closely decoupled to GND with a 1μF or greater capacitor.
EN	-	-	-	-	3	I	Enable input. A low voltage (< V _{IL}) on this pin turns the regulator off. A high voltage (> V _{IH}) on this pin enables the regulator output. The EN pin can be connected to the VIN pin if not used. Do not leave floating.
NC	-	-	-	3,4	4	-	No internal connection.
FB	-	-	-	-	4	-	The FB pin is only available for the adjustable voltage versions. This pin is the input to the control-loop error amplifier, and is used to set the output voltage of the device.

(1) I=input, O=output, G= Ground.

PIN CONFIGURATION AND FUNCTIONS



PIN DESCRIPTION

NAME	PIN	I/O ⁽¹⁾	FUNCTION
	UDFN1.6X1.6-6		
GND	6,7	G	Ground
VOUT	3	O	Regulated output voltage. Connect a minimum 1 μ F low-ESR capacitor to this pin.
VIN	1	I	Input voltage supply. Must be closely decoupled to GND with a 1 μ F or greater capacitor.
EN	4	I	Enable input. A low voltage ($< V_{IL}$) on this pin turns the regulator off. A high voltage ($> V_{IH}$) on this pin enables the regulator output. The EN pin can be connected to the VIN pin if not used. Do not leave floating.
NC	2,5	-	No internal connection.

(1) I=input, O=output, G= Ground.

9 SPECIFICATIONS

9.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ^{(1) (2)}

		MIN	MAX	UNIT
V _{IN}	Input voltage	-0.3	40	V
V _{EN}	V _{EN} voltage range	-0.3	40	V
V _{OUT}	V _{OUT} voltage range	-0.3	13	V
T _J	PN Junction temperature ⁽³⁾	-40	150	°C
P _D	Continuous power dissipation ⁽⁴⁾	Internally limited		W
θ _{JA}	Package thermal impedance ⁽⁵⁾	SOT23-3	230	°C/W
		SOT23-5	160	
		SOT23-5(S-Type)	160	
		SOT89-3	105	
		SOT89-3(L-Type)	135	
		UDFN1.6X1.6-6	TBD	
T _{stg}	Storage temperature range	-65	150	°C
T _{solder}	Lead temperature (Soldering, 10 sec)		260	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the GND pin.
- (3) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.
- (4) Internal thermal shutdown circuitry protects the device from permanent damage. The actual chip output current is subject to the input-output voltage difference, ambient temperature and PCB heat dissipation design.
- (5) The package thermal impedance is calculated in accordance with JESD-51.

9.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-Body Model (HBM), ANSI/ESDA/JEDEC JS-001-2023	±2000
		Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1000



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Input Voltage Range on VIN	2.5	36	V
V _{OUT}	Output Voltage Range on VOUT	V _{FB}	12	V
I _{OUT}	Output Current Range on VOUT	1	250	mA
C _{OUT}	Capacitor of VOUT pin	1	47	μF
T _J	PN Junction temperature	-40	125	°C

9.4 Electrical Characteristics

Over operating temperature range ($-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$), $V_{IN} = V_{OUTnom} + 2\text{V}$ ⁽¹⁾, $C_{IN} = C_{OUT} = 1\mu\text{F}$, $V_{OUT}=3.3\text{V}$, $I_{OUT}=1\text{mA}$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}\text{C}$.

PARAMETER	SYMBOL	CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
POWER SUPPLY AND CURRENTS						
Input Voltage ⁽¹⁾	V_{IN}		2.5		36	V
Under Voltage Lockout	UVLO	V_{IN} rising		2.25		V
Hysteresis	V_{HYS}	V_{IN} falling		50		mV
Quiescent Current	I_Q	$V_{IN}=12\text{V}$, $I_{OUT}=0\text{mA}$	$T_J = 25^{\circ}\text{C}$	1.9		μA
			$T_J = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$		4	
			$T_J = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$		5	
Ground Pin Current	I_{GND}	$I_{OUT} = 150\text{mA}$		0.55		mA
Shutdown Current	I_{SD}	$V_{IN}=36\text{V}$, $EN=0$		0.4	1	μA
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT}	Adjustable Version	V_{FB}		12	V
Feedback Voltage ⁽¹⁾	V_{FB}	Adjustable Version, $T_J = 25^{\circ}\text{C}$, $I_{OUT}=1\text{mA}$		1.000		V
Feedback Pin Current	I_{FB}	Adjustable Version, $V_{FB}=1.1\text{V}$		0.001	0.05	μA
DC Output Accuracy ⁽¹⁾	ΔV_{OUT}	$T_J = 25^{\circ}\text{C}$, $I_{OUT} = 1\text{mA}$	-1		1	%
Line Regulation ⁽¹⁾	$\Delta V_{OUT}(\Delta V_{IN})$	$V_{IN} = V_{OUT} + 2\text{V}$ to 36V , $I_{OUT} = 1\text{mA}$		0.001		%/V
Load Regulation ⁽¹⁾	$\Delta V_{OUT}(\Delta I_{OUT})$	$V_{IN} = V_{OUT} + 2\text{V}$, $I_{OUT} = 1\text{mA}$ to 250mA		40		mV
Output Voltage Temperature Coefficient ⁽⁴⁾	$\frac{\Delta V_{OUT}}{\Delta T_A \times V_{OUT}}$	$I_{OUT} = 1\text{mA}$, $T_J = -40^{\circ}\text{C} \sim 85^{\circ}\text{C}$		85		ppm/ $^{\circ}\text{C}$
		$I_{OUT} = 1\text{mA}$, $T_J = -40^{\circ}\text{C} \sim 125^{\circ}\text{C}$		70		
Maximum Output Current ⁽⁵⁾	I_{OUTMAX}	$V_{IN} > 4.0\text{V}$ or $V_{OUT} + V_{DO}$, whichever is greater	250			mA
OUTPUT VOLTAGE						
Dropout Voltage ⁽⁶⁾	V_{DO}	$I_{OUT}=150\text{mA}$	$V_{OUT}=3.0\text{V}$		1050	mV
			$V_{OUT}=3.3\text{V}$		1000	
			$V_{OUT}=5.0\text{V}$		850	
			$V_{OUT}=9.0\text{V}$		750	
			$V_{OUT}=12.0\text{V}$		750	
POWER SUPPLY REJECTION RATIO AND NOISE						
Power Supply Rejection Ratio ⁽⁷⁾	PSRR	$V_{IN}=5.3\text{V}$, $V_{OUT}=3.3\text{V}$, $I_{OUT}=50\text{mA}$	$f = 100\text{Hz}$		65	dB
			$f = 1\text{KHz}$		65	dB
			$f = 100\text{KHz}$		49	dB
			$f = 1\text{MHz}$		45	dB
Output Noise Voltage ⁽⁷⁾	V_N	$BW=10\text{Hz}$ to 100kHz , $V_{OUT}=3.3\text{V}$, $I_{OUT}=100\text{mA}$		135		μV_{RMS}
ENABLE AND STARTUP TIME						
EN Input Logic High Voltage	V_{IH}	$V_{IN} = 2.5\text{V}$ to 36V , EN rising	1.2			V
EN Input Logic Low Voltage	V_{IL}	$V_{IN} = 4.3\text{V}$ to 36V , EN falling			0.4	V
	$V_{IL,2.5}$	$V_{IN} = 2.5\text{V}$ to 4.3V , EN falling			0.2	V
EN Input Leakage Current	I_{EN}	$V_{IN}=36\text{V}$, $EN=0\text{V}$			1	μA
		$V_{IN}=36\text{V}$, $EN=36\text{V}$			1	μA
Output Voltage Delay Time	TD	From $V_{EN} > V_{IH}$ to $V_{OUT} = 10\%$ of V_{OUTnom}		125		μs
Output Rise Time	TR	From $V_{OUT} = 10\%$ to 90% of V_{OUTnom}		95		μs

PROTECTIONS						
Over Current Limit	I_{LMT}	$V_{OUT}=0.8*V_{OUTnom}$	300	450		mA
Short-Circuit Current Limit	I_{SC}	$V_{OUT}=0V$		40		mA
Thermal Shutdown Threshold ⁽⁷⁾	T_{TSD}	T_J rising		150		°C
Thermal Shutdown Hysteresis ⁽⁷⁾	T_{HYS}	T_J falling from shutdown		25		°C

NOTE:

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.5V, whichever is greater.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) Output voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.

(5) Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when $V_{IN} < V_{OUT} + V_{DROP}$.

(6) The dropout voltage is defined as $V_{IN} - V_{OUT}$, when V_{OUT} is 2% below the value of V_{OUT} for $V_{IN} = V_{OUTnom} + 2V$ ⁽¹⁾.

(7) Guaranteed by design and characterization, not a FT item.

Preliminary version

9.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

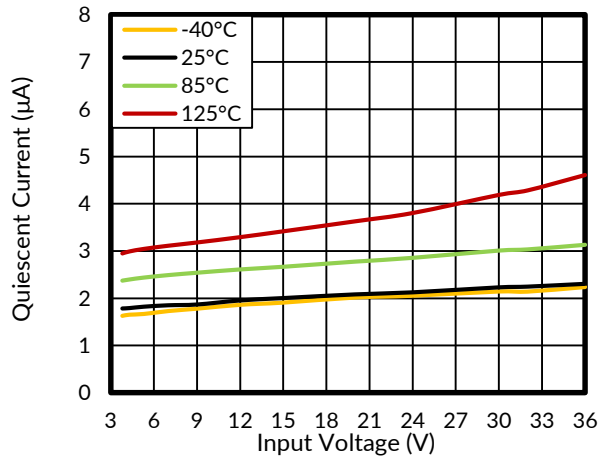


Figure 3. Quiescent Current vs Input Voltage

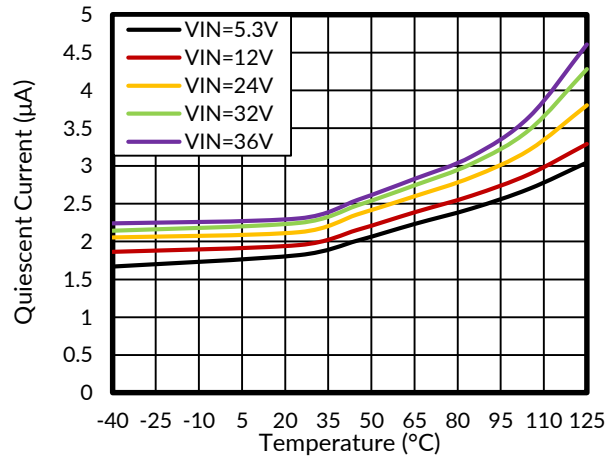


Figure 4. Quiescent Current vs Temperature

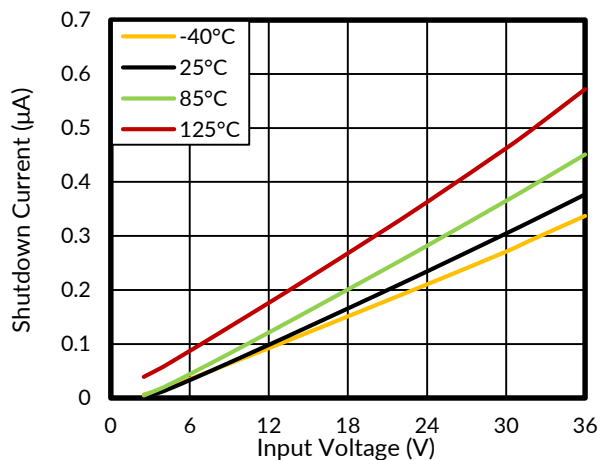


Figure 5. Shutdown Current vs Input Voltage

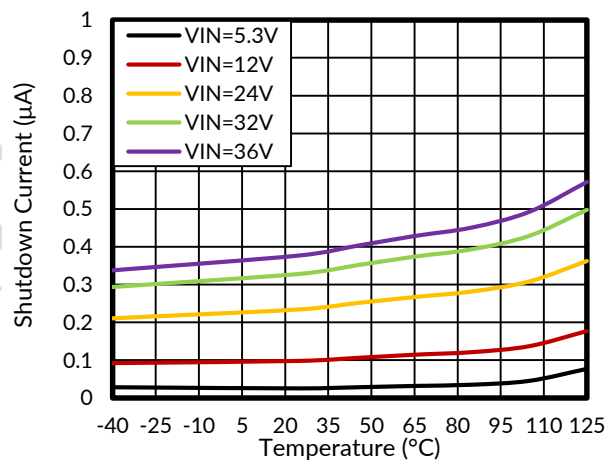


Figure 6. Shutdown Current vs Junction Temperature

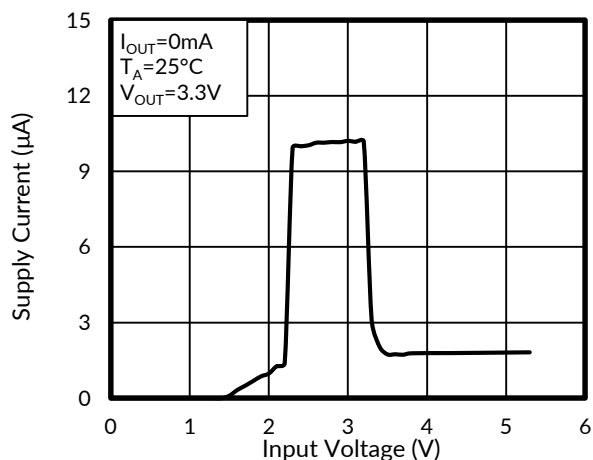


Figure 7. Supply Current vs Input Voltage

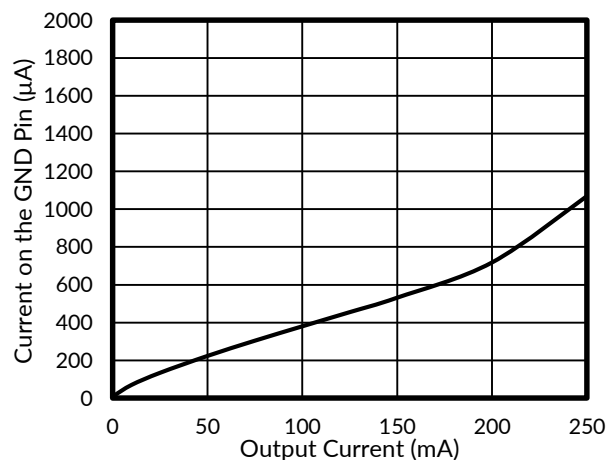


Figure 8. Ground Pin Current vs Output Current

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

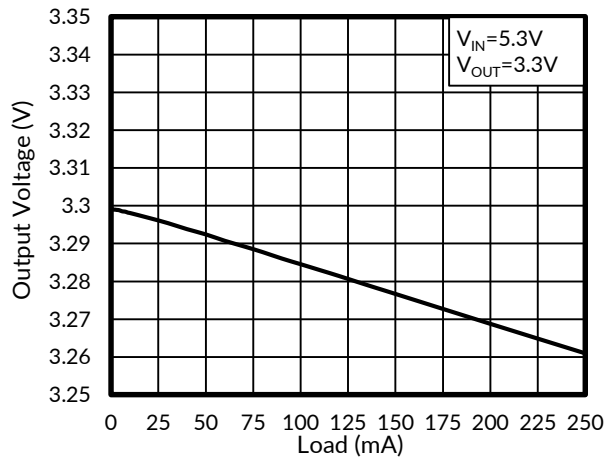


Figure 9. Load Regulation

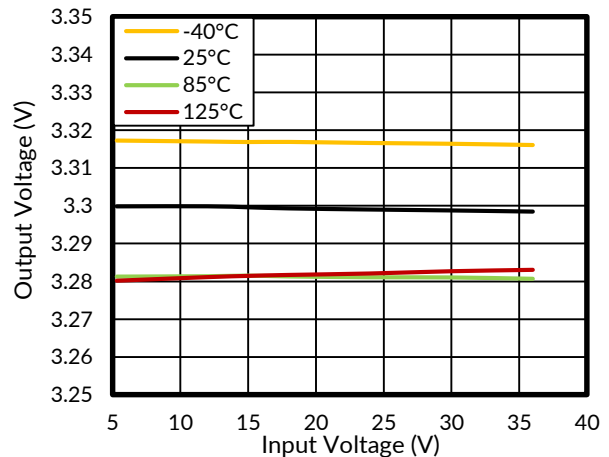


Figure 10. Line Regulation

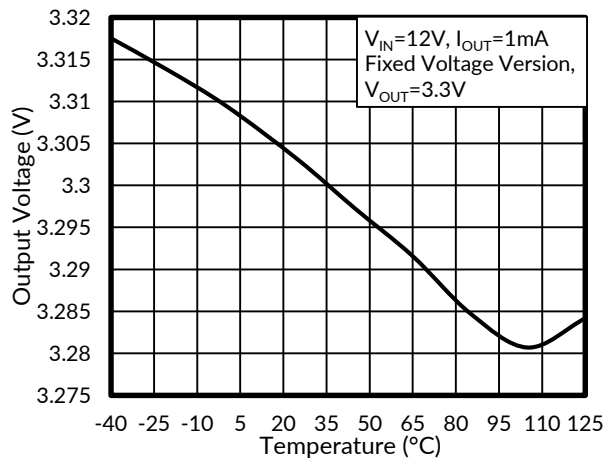


Figure 11. Output Voltage vs Junction Temperature

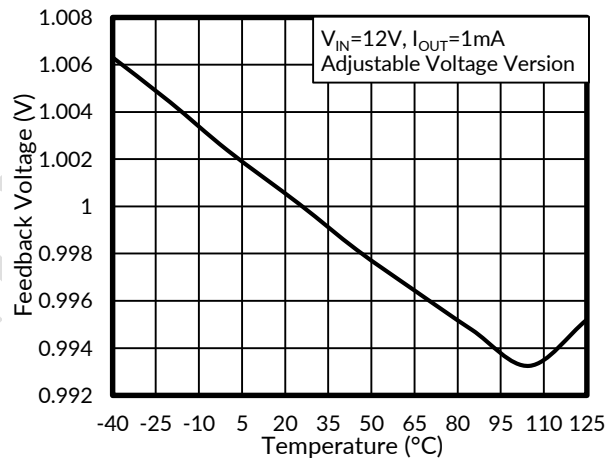


Figure 12. Feedback Voltage vs Junction Temperature

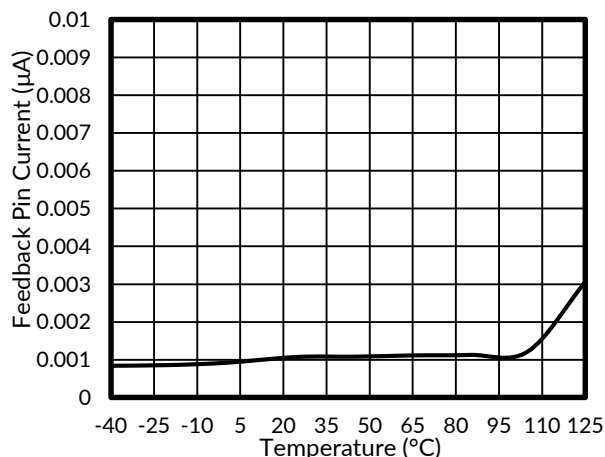


Figure 13. Feedback Pin Current vs Junction Temperature

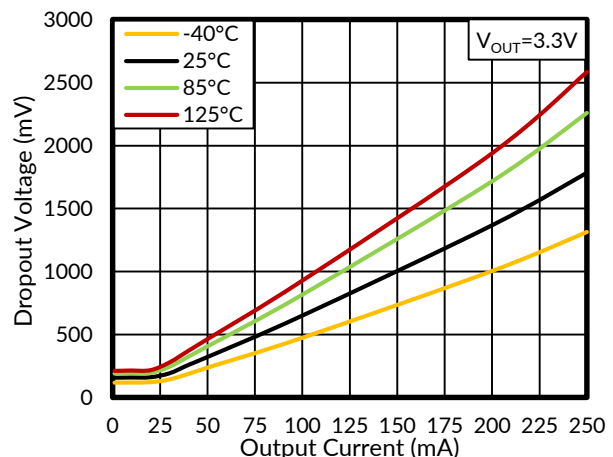


Figure 14. Dropout Voltage vs Output Current

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

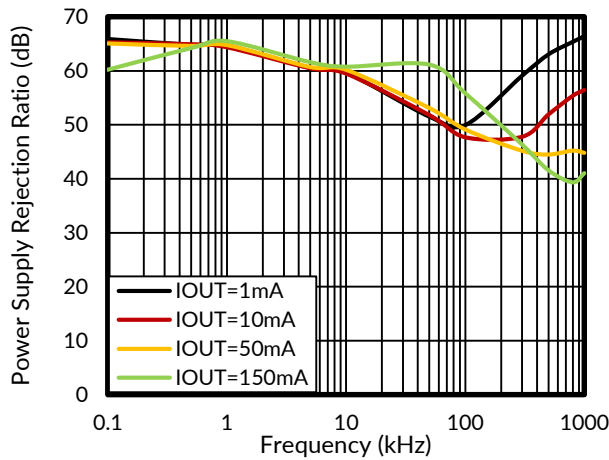


Figure 15. Power Supply Rejection Ratio vs Frequency

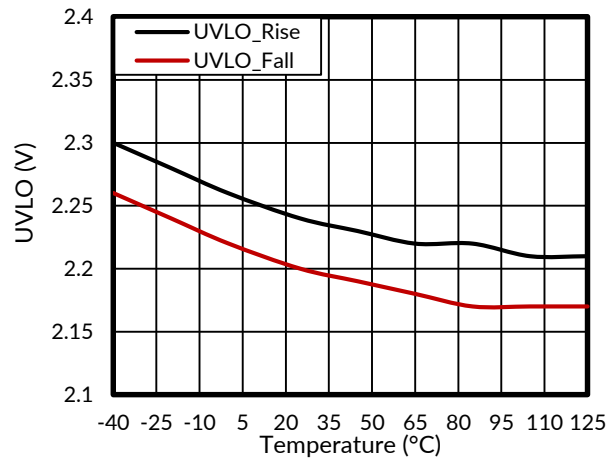


Figure 16. UVLO vs Junction Temperature

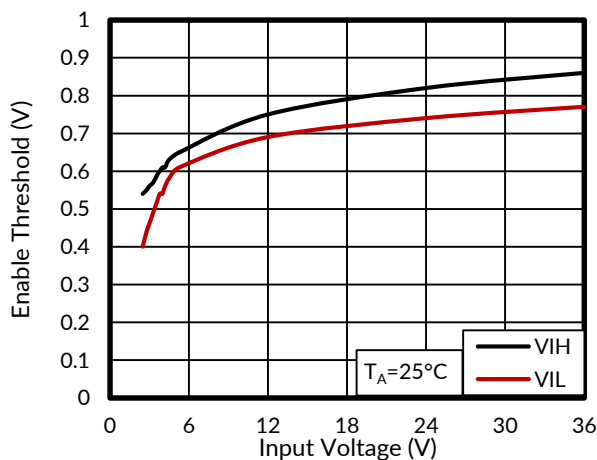


Figure 17. Enable Threshold vs Input Voltage

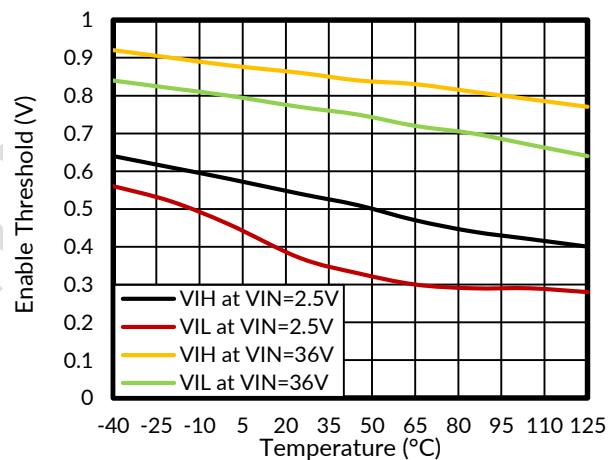


Figure 18. Enable Threshold vs Junction Temperature

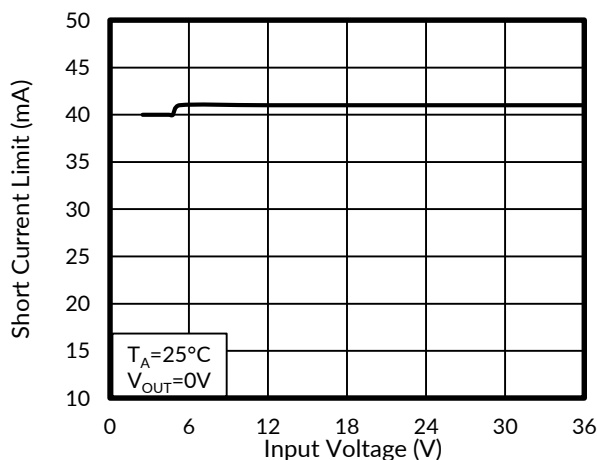


Figure 19. Short Current Limit vs Input Voltage

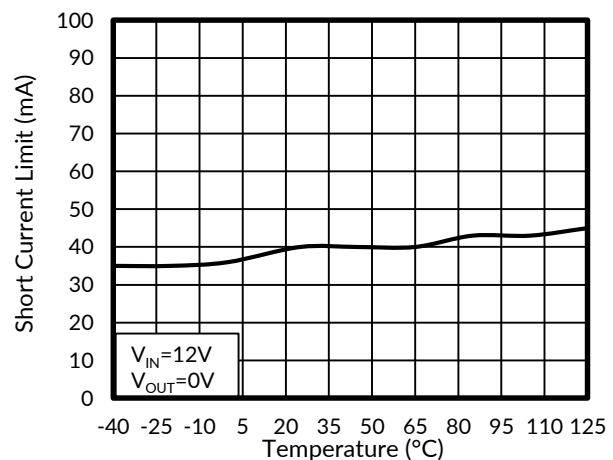


Figure 20. Short Current Limit vs Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

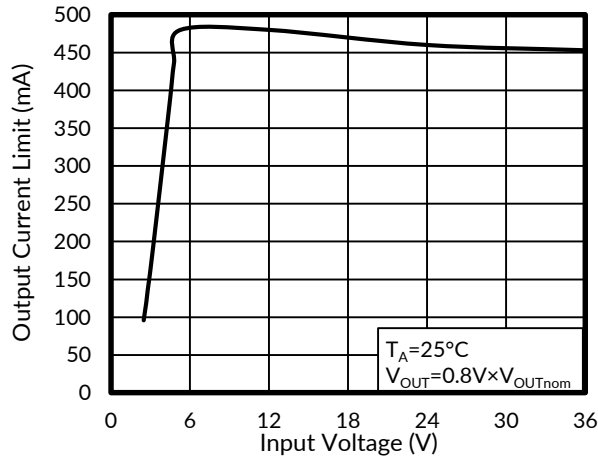


Figure 21. Output Current Limit vs Input Voltage

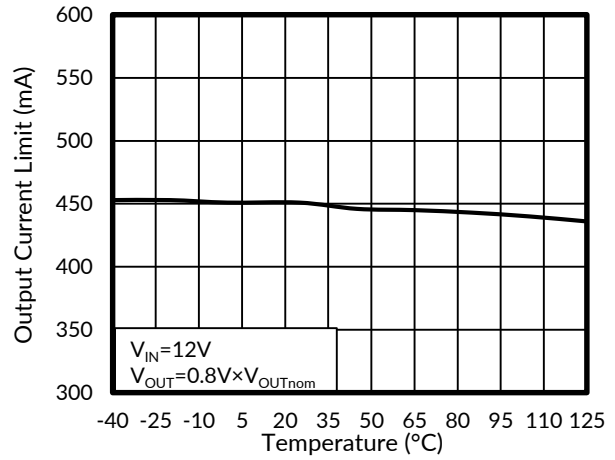


Figure 22. Output Current Limit vs Temperature

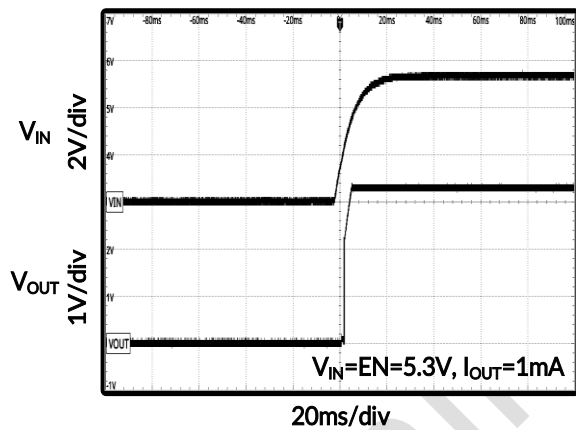


Figure 23. Power On

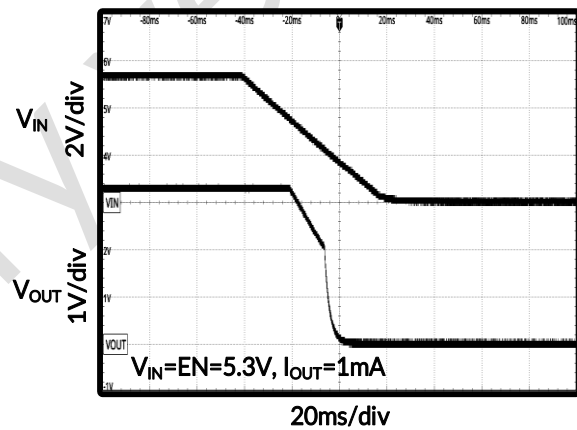


Figure 24. Power Off

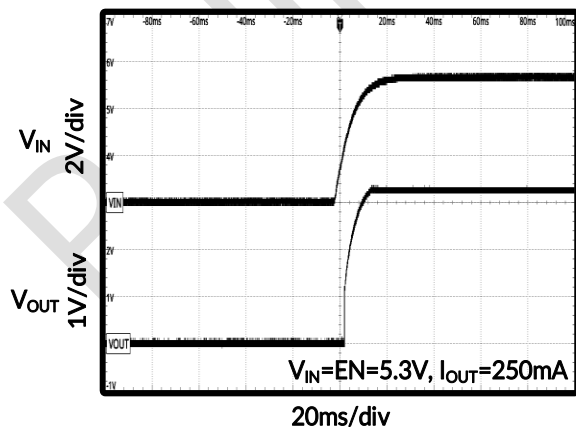


Figure 25. Power On

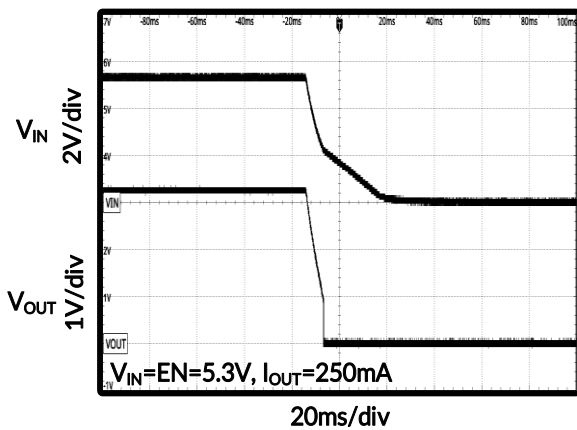


Figure 26. Power Off

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

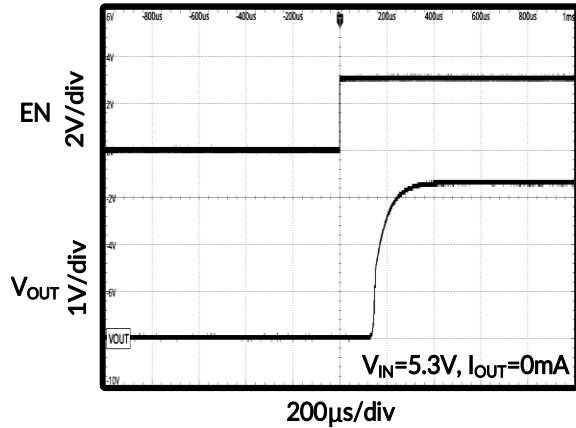


Figure 27. Turn On

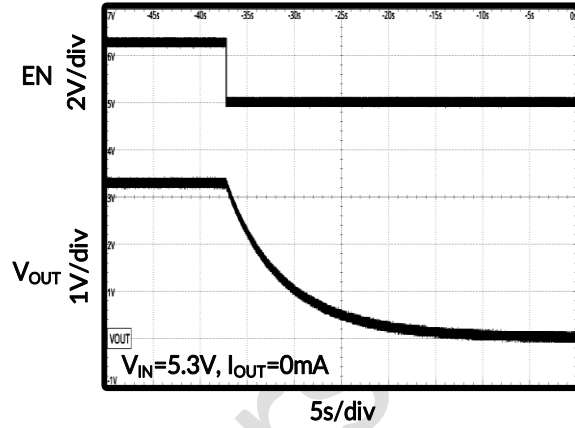


Figure 28. Turn Off

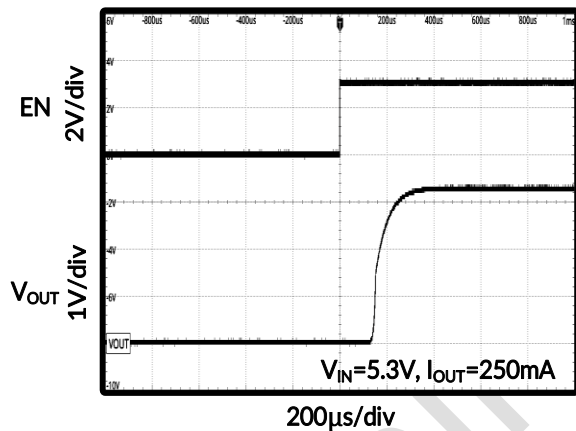


Figure 29. Turn On

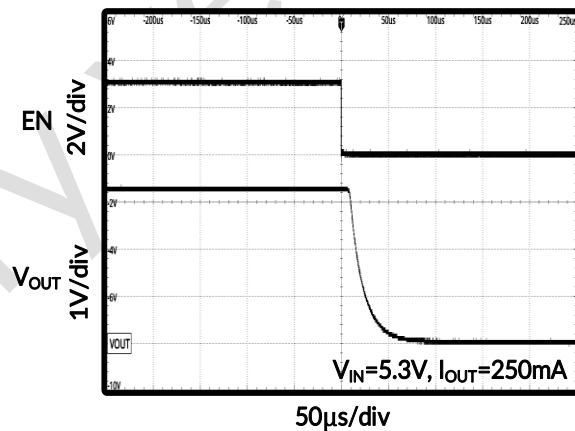


Figure 30. Turn Off

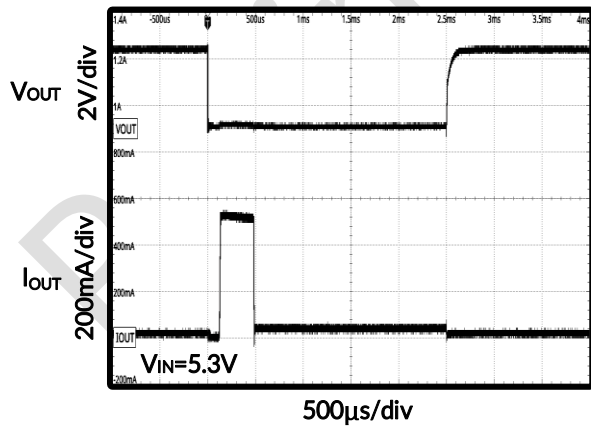


Figure 31. Turn On First, Then Short Circuit

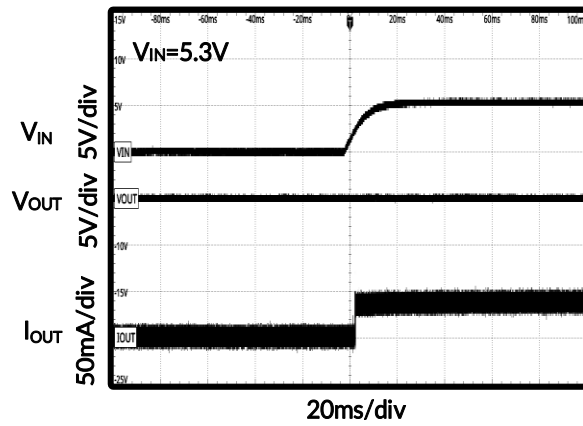


Figure 32. Short Circuit First, Then VIN Power ON

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

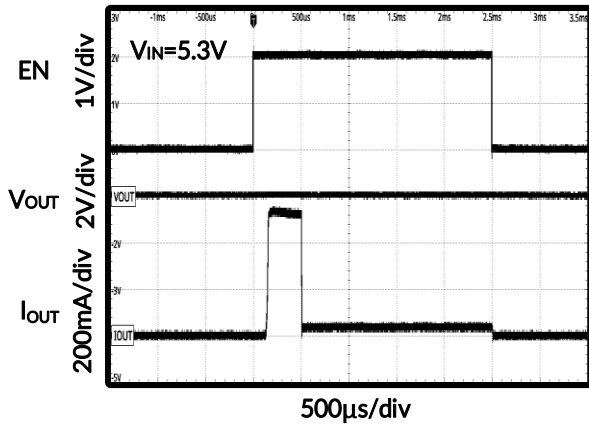


Figure 33. Short Circuit First, Then Enable

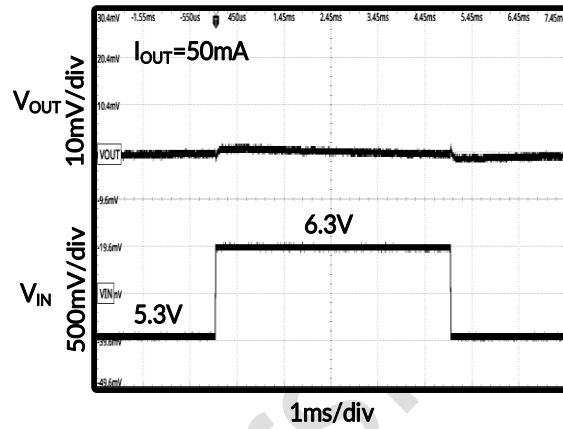


Figure 34. Line Transient Response

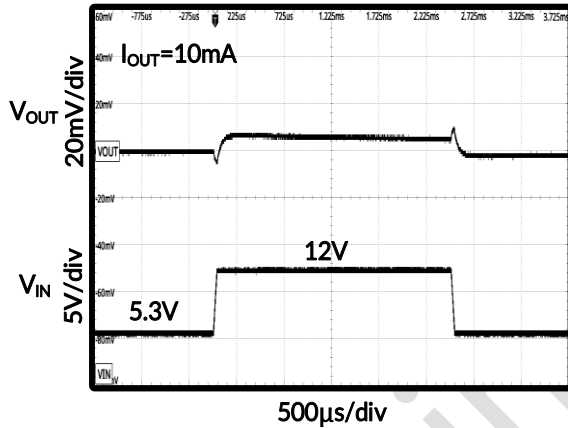


Figure 35. Line Transient Response

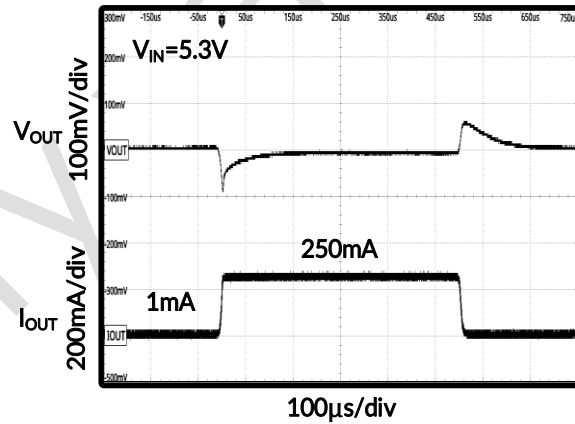


Figure 36. Load Transient Response

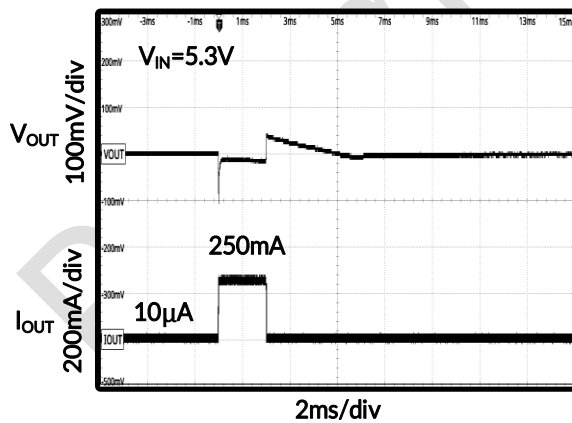


Figure 37. Load Transient Response

10 DETAILED DESCRIPTION

10.1 Overview

The RS75XX-2H series are a group of positive voltage regulators manufactured by CMOS technologies with low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small. The RS75XX-2H series can deliver 250mA output current and allow an input voltage as high as 36V. The series are very suitable for the battery-powered equipment, such as RF applications and other systems requiring a quiet voltage source.

10.2 Under Voltage Lockout (UVLO)

The RS75XX-2H family of devices uses an under voltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

10.3 Shutdown

Enable input. A low voltage ($< V_{IL}$) on this pin turns the regulator off. A high voltage ($> V_{IH}$) on this pin enables the regulator output. The EN pin can be connected to the VIN pin if not used. Do not leave floating.

10.4 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 150°C which allows the device to cool. When the junction temperature cools to approximately 125°C, the output circuitry enables.

Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the RS75XX-2H has been designed to protect against temporary thermal overload conditions. The T_{SD} circuitry was not intended to replace proper heat-sinking. Continuously running the RS75XX-2H device into thermal shutdown may degrade device reliability.

10.5 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO threshold minus V_{HYS} , or has not yet exceeded the UVLO threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

10.6 Current-Limit Protection

The RS75XX-2H monitors the current flowing through the output PMOS and limits the maximum current to prevent load and RS75XX-2H from damages during current overload conditions.

10.7 Short Current-Limit Protection

The short current-limit function reduces the current limit to 40mA (typical) during short circuit conditions.

10.8 Input and Output Capacitor Requirements

Connecting a 1 μ F low-equivalent series resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher value capacitor can be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the power source.

The RS75XX-2H family of devices is designed to be stable with standard ceramic output capacitors of values 1 μ F or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature.

10.9 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2 , according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (1)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the Electrical Characteristics table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (2)$$

Preliminary version

11 POWER SUPPLY RECOMMENDATIONS

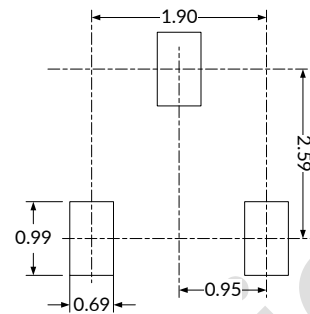
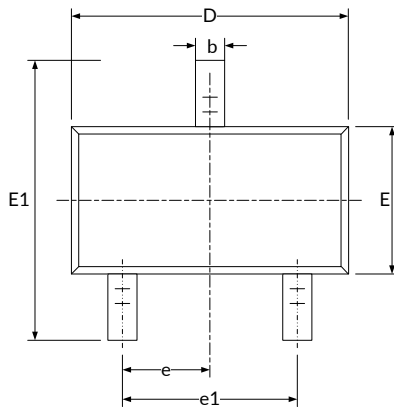
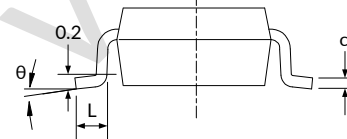
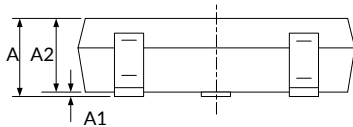
The device is designed to operate from an input voltage supply range between 2.5V and 36V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

12 LAYOUT

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

To improve ac performance (such as PSRR, output noise, and transient response), designing the board with separate ground planes for V_{IN} and V_{OUT} is recommended, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

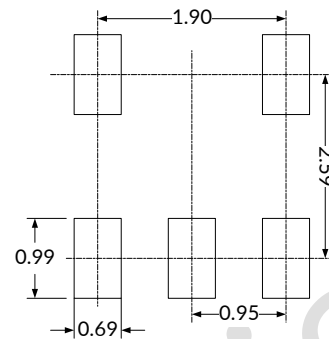
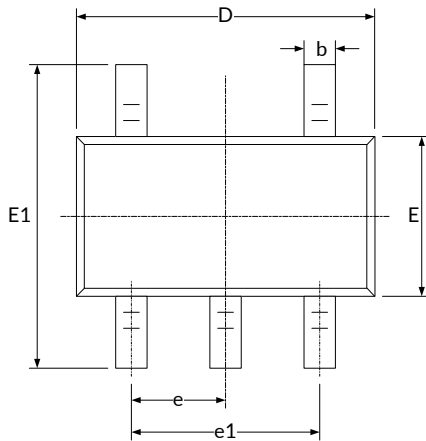
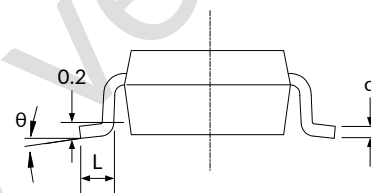
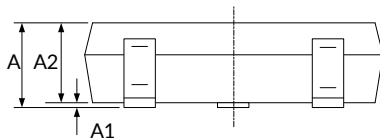
13 PACKAGE OUTLINE DIMENSIONS SOT23-3⁽³⁾


RECOMMENDED LAND PATTERN (Unit: mm)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D ⁽¹⁾	2.820	3.020	0.111	0.119
E ⁽¹⁾	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) ⁽²⁾		0.037(BSC) ⁽²⁾	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

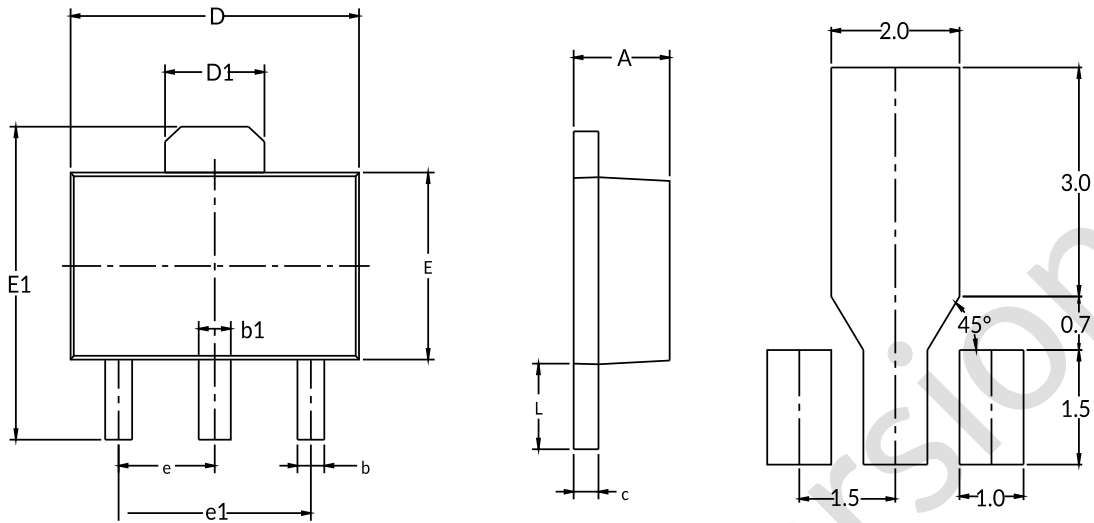
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

SOT23-5⁽³⁾

RECOMMENDED LAND PATTERN (Unit: mm)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D ⁽¹⁾	2.820	3.020	0.111	0.119
E ⁽¹⁾	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) ⁽²⁾		0.037(BSC) ⁽²⁾	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

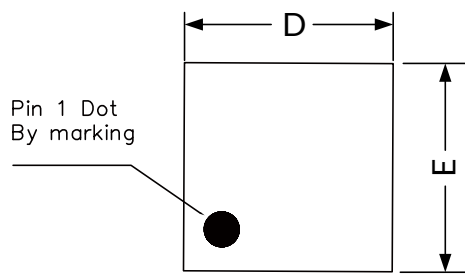
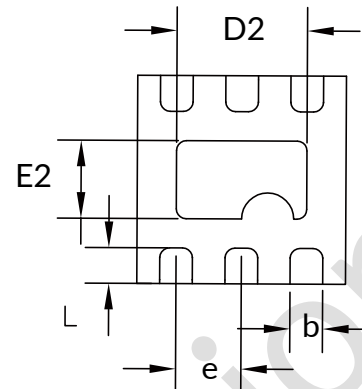
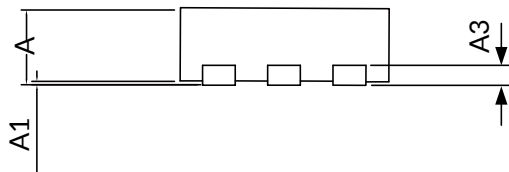
SOT89-3 (4)


RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D ⁽¹⁾	4.400	4.600	0.173	0.181
D1	1.550 REF ⁽²⁾		0.061 REF ⁽²⁾	
E ⁽¹⁾	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 BSC ⁽³⁾		0.060 BSC ⁽³⁾	
e1	3.000 BSC ⁽³⁾		0.118 BSC ⁽³⁾	
L	0.900	1.200	0.035	0.047

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
4. This drawing is subject to change without notice.

UDFN1.6X1.6-6⁽⁴⁾

TOP VIEW

BOTTOM VIEW

SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.150 REF ⁽²⁾		0.006 REF ⁽²⁾	
D ⁽¹⁾	1.550	1.650	0.061	0.065
E ⁽¹⁾	1.550	1.650	0.061	0.065
D2	0.900	1.050	0.035	0.041
E2	0.500	0.650	0.020	0.025
L	0.200	0.300	0.008	0.012
b	0.200	0.300	0.008	0.012
e	0.500 BSC ⁽³⁾		0.020 BSC ⁽³⁾	

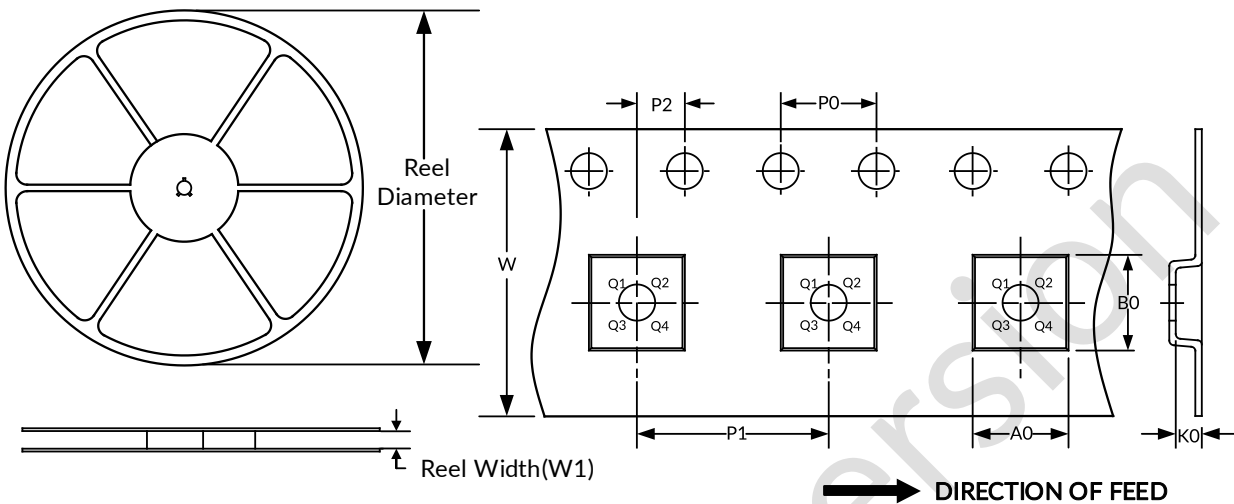
NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
4. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-3	7"	9.0	3.20	3.30	1.30	4.0	4.0	2.0	8.0	Q3
SOT23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOT89-3	7"	13.2	4.85	4.45	1.85	4.0	8.0	2.0	12.0	Q3
UDFN1.6X1.6-6	7"	9.5	1.86	1.90	0.88	4.0	4.0	2.0	8.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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Preliminary version