14-Bit 20MSps/40MSps 1.8V Dual Analog-to-Digital Converter

1 FEATURES

- **1.8V Analog Supply Operation**
- **1.8V to 3.3V Output Supply**
- **SNR**
  74.2dBFS at 9.9MHz Input
  70.5dBFS at 200MHz Input
- **HD3**
  93dBc at 9.9MHz input
  80dBc at 200MHz input
- **On-Chip Voltage Reference and Sample-and-Hold Circuit**
- **Flexible Analog Input Range: 1Vpp to 2Vpp**
- **ADC Clock Duty Cycle Stabilizer**
- **Serial Port Control**
- **Offset Binary, Gray Code, Twos Complement Data Format or Random Code**
- **Data Clock Out (DCO) With Programmable Clock and Data Alignment**

2 APPLICATIONS

- **Communications**
- **Diversity Radio Systems**
- **Multimode Digital Receivers GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA**
- **I/Q Demodulation System**
- **Smart Antenna Systems**
- **Battery-Powered Instruments**
- **Ultrasound**

3 DESCRIPTIONS

The RS1522 operates from a single 1.8 V analog power supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.

The sample-and-hold circuit maintains excellent performance for input frequencies up to 200 MHz and is designed for low cost, low power, and ease of use.

A standard serial port interface (SPI) supports various product features and functions, such as data output format ting, internal clock divider, power-down, DCO, data output (D13 to D0) timing and offset adjustments, and voltage reference modes.

The RS1522 is packaged in a 64-lead QFN package.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1522	QFN9X9-64	9.00mm×9.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

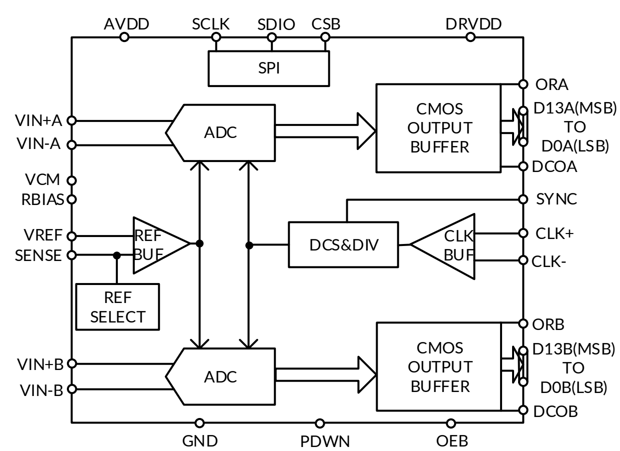

Figure 1. RS1522 Functional Block Diagram

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2024/11/27	Preliminary version completed

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	PACKAGE LEAD	TEMPERATURE RANGE	PACKAGE MARKING (2)	MSL (3)
RS1522	RS1522YQAB64	QFN9X9-64	-40°C ~85°C	RS1522	MSL3

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

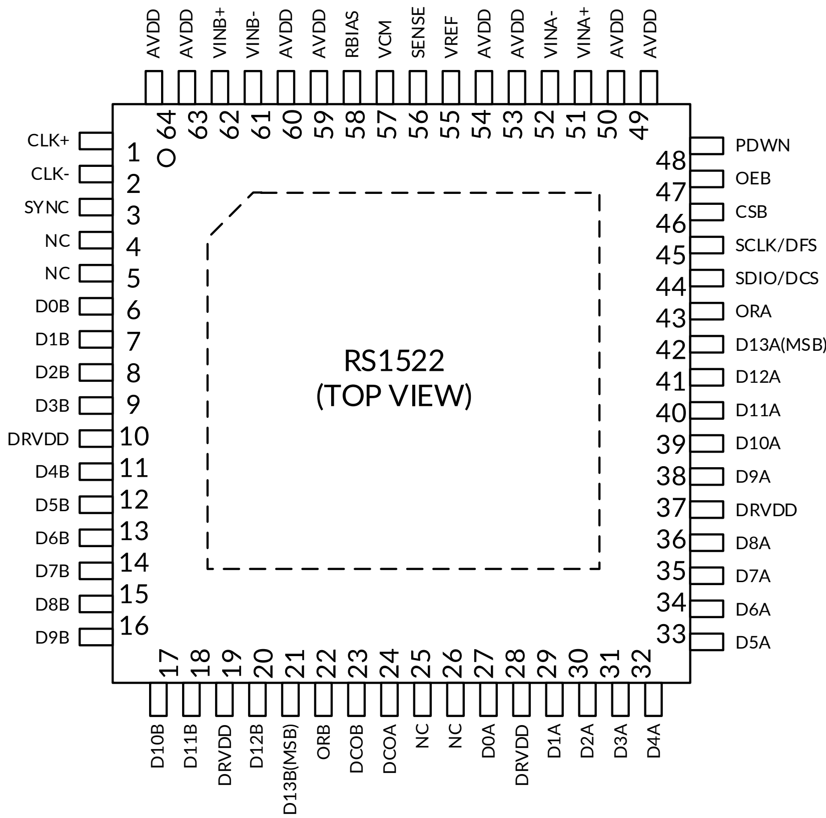
(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 GENERAL DESCRIPTION

The RS1522 is a monolithic, dual-channel, 1.8 V supply, 14-bit, 20/40 MSPS analog-to-digital converter (ADC). It features a high performance sample-and-hold circuit and on-chip voltage reference. The product uses multistage differential pipeline architecture with output error correction logic to provide 14-bit accuracy at 40 MSPS data rates and to guarantee no missing codes over the full operating temperature range. The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. A differential clock input controls all internal conversion cycles. An optional duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance. The digital output data is presented in offset binary, gray code, or twos complement format. A data output clock (DCO) is provided for each ADC channel to ensure proper latch timing with receiving logic. Both 1.8 V and 3.3 V CMOS levels are supported and output data can be multiplexed onto a single output bus. The RS1522 is available in a 64-lead QFN and is specified over the industrial temperature range (−40°C to +85°C).

7 PIN CONFIGURATION AND FUNCTIONS



QFN9X9-64

PIN FUNCTIONS

Pin No	Mnemonic	Description
0	GND	Exposed paddle is the only ground connection for the chip. Must be connected to PCB AGND
1, 2	CLK+, CLK−	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
3	SYNC	Digital Input. SYNC input to clock divider. 30kΩ internal pull-down.
4, 5, 25, 26	NC	Do Not Connect.
6 to 9, 11 to 18, 20, 21	D0B to D13B	Channel B Digital Outputs. D13B = MSB.
10, 19, 28, 37	DRVDD	Digital Output Driver Supply (1.8 V to 3.3 V).
22	ORB	Channel B Out-of-Range Digital Output.
23	DCOB	Channel B Data Clock Digital Output.
24	DCOA	Channel A Data Clock Digital Output.
27, 29 to 36, 38 to 42	D0A to D13A	Channel A Digital Outputs. D13A = MSB.
43	ORA	Channel A Out-of-Range Digital Output.
44	SDIO/DCS	SPI Data Input/Output (SDIO). Bidirectional SPI Data I/O in SPI mode. Internal pull-down in SPI mode. Duty Cycle Stabilizer (DCS)
45	SCLK/DFS	SPI Clock (SCLK) Input in SPI mode. Internal pull-down. Data Format Select (DFS).
46	CSB	SPI Chip Select. Active low enable; internal pull-up.
47	OEB	Digital Input. Enable Channel A and Channel B digital outputs if low, tristate outputs if high. Internal pull-down.

48	PDWN	Digital Input. Internal pull-down.
49, 50, 53, 54, 59, 60, 63, 64	AVDD	1.8 V Analog Supply Pins.
51, 52	VINA+, VINA−	Channel A Analog Inputs.
55	VREF	Voltage Reference Input/Output.
56	SENSE	Reference Mode Selection.
57	VCM	Analog output voltage at midsupply to set common mode of the analog inputs.
58	RBIAS	Sets Analog Current Bias. Connect to 10kΩ (1% tolerance) resistor to ground.
61,62	VINB−, VINB+	Channel B Analog Inputs.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNIT
AVDD to AGND	-0.3	2	V
DRVDD to AGND	-0.3	3.9	V
VIN+/-, CLK+/-, SYNC, VREF, SENSE, VCM, RBIAS	-0.3	2	V
CSB, SCLK, SDIO, PDWN, OEB	-0.3	3.9	V
DCOA/B, D0A/B- D13A/B	-0.3	3.9	V
Maximum Junction Temperature, $T_{J,MAX}$		150	°C
Operating Temperature Range	-40	85	°C
Storage Temperature Range	-65	150	°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

8.2 ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

8.3 Thermal Characteristics

The exposed paddle is the only ground connection for the chip and must be soldered to the analog ground plane of the user's PCB. Soldering the exposed paddle to the user's board also increases the reliability of the solder joints and maximizes the thermal capability of the package.

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane, and its typical value is about 19.2°C/W. Airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

8.4 DC Specifications

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V pp differential input, 1.0 V internal reference; AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

PARAMETER	TEMP	20MSps/40MSps			UNIT
		MIN	TYP	MAX	
Resolution			14		Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full		±0.1	±0.7	%FSR
Gain Error	Full		±0.8		%FSR
Differential Nonlinearity (DNL) [1]	Full	-1		+0.7	LSB
	25°C		±0.45		LSB
Integral Nonlinearity (INL) [1]	Full			+2	LSB
	25°C		±0.65		LSB
MATCHING CHARACTERISTICS					
Offset Error	Full			±0.7	%FSR
Gain Error	Full		±0.2		%FSR
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	Full	0.98		1.005	V
Load Regulation Error at 1.0 mA	Full		2		mV
Input-Referred Noise, VREF=1V	25°C		0.98		LSBrms
ANALOG INPUT					
Input Span, VREF=1V	Full		2		Vp-p
Input Capacitance [2]	Full		6		pF
Input Common-Mode Voltage	Full		0.9		%FSR
REFERENCE INPUT RESISTANCE	Full		6		kΩ
POWER SUPPLY VOLTAGE/CURRENT					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7		3.6	V
IAVDD [1]	Full		39.7/59.5		mA
IDRVDD (1.8V) [1]	Full		3.8/6.2		mA
IDRVDD (3.3V) [1]	Full		7.3/11.8		mA
POWER CONSUMPTION					
DC Input	Full		72/108		mW
Sine Wave Input (1.8V) [1]	Full		78.3/118.3		mW
Sine Wave Input (3.3V) [1]	Full		95.5/146.0		mW
Standby Power [3]	Full		20		mW
Power-Down Power	Full		1		mW

(1) Measured with a low input frequency at rated sample rate, full-scale sine wave, with approximately 5 pF loading on each output bit.
(2) Input capacitance refers to the effective capacitance between one differential input pin and AGND.
(3) Standby power is measured with a dc input and the CLK inactive.

8.5 AC Specifications

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V pp differential input, 1.0 V internal reference; AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

PARAMETER	TEMP	20MSps/40MSps			UNIT
		MIN	TYP	MAX	
SIGNAL-TO-NOISE RATIO (SNR)					
f_{in}=9.9MHz	25°C		75.4		dBFS
f_{in}=27MHz	25°C		74.7		dBFS
	Full	73.5			dBFS
f_{in}=200MHz	25°C		70.5		dBFS
SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)					
f_{in}=9.9MHz	25°C		74.7		dBFS
f_{in}=27MHz	25°C		74.0		dBFS
	Full	73.3			dBFS
f_{in}=200MHz	25°C		70.0		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{in}=9.9MHz	25°C		12.1		Bits
f_{in}=27MHz	25°C		12.0		Bits
f_{in}=200MHz	25°C		11.3		Bits
THIRD HARMONIC (HD3)					
f_{in}=9.9MHz	25°C		93		dBc
f_{in}=27MHz	25°C		84		dBc
	Full	80			dBc
f_{in}=200MHz	25°C		80		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{in}=9.9MHz	25°C		93		dBc
f_{in}=27MHz	25°C		84		dBc
	Full	80			dBc
fin=200MHz	25°C		80		dBc
TWO-TONE SFDR					
f_{in}=25.1/27.1MHz (-7dBFS)	25°C		75		dBc
CROSSTALK [4]	Full		-95		dBc

(4) Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.

8.6 Digital Specifications

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V pp differential input, 1.0 V internal reference; AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

PARAMETER	TEMP	MIN	TYP	MAX	UNIT
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	Vp-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full		0.9		V
High Level Input Current	Full	-100		+100	µA
Low Level Input Current	Full	-100		+100	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
SYNCHRONOUS INPUTS (SYNC)					
Logic Compliance			CMOS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	Vp-p
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	-100		+100	µA
Low Level Input Current	Full	-100		+100	µA
Input Capacitance	Full		2		pF
Input Resistance	Full		16		kΩ
LOGIC INPUTS (CSB) [5]					
High Level Input Voltage		1.2		DRVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	-100		+100	µA
Low Level Input Current	Full	-100		+100	µA
Input Resistance	Full		20		kΩ
Input Capacitance	Full		3		pF
LOGIC INPUTS (SCLK/DFS) [6]					
High Level Input Voltage		1.2		DRVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	-100		+100	µA
Low Level Input Current	Full	-100		+100	µA
Input Resistance	Full		20		kΩ
Input Capacitance	Full		3		pF
LOGIC INPUTS/OUTPUTS (SDIO/DCS) [6]					
High Level Input Voltage		1.2		DRVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	-100		+100	µA
Low Level Input Current	Full	-100		+100	µA
Input Resistance	Full		20		kΩ
Input Capacitance	Full		3		pF

LOGIC INPUTS (OEB, PDWN) [6]					
High Level Input Voltage		1.2		DRVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	-100		+100	µA
Low Level Input Current	Full	-100		+100	µA
Input Resistance	Full		20		kΩ
Input Capacitance	Full		3		pF
DIGITAL OUTPUTS					
DRVDD=1.8V					
High Level Output Voltage					
I_{OH}=50µA	Full	1.79			V
I_{OH}=0.5mA	Full	1.75			V
Low Level Output Voltage					
I_{OL}=50µA	Full			0.05	V
I_{OL}=1.6mA	Full			0.2	V
DRVDD=3.3V					
High Level Output Voltage					
I_{OH}=50µA	Full	3.29			V
I_{OH}=0.5mA	Full	3.25			V
Low Level Output Voltage					
I_{OL}=50µA	Full			0.05	V
I_{OL}=1.6mA	Full			0.2	V

(5) Internal pull-up.
(6) Internal pull-down.

8.7 Switching Specifications

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V pp differential input, 1.0 V internal reference; AIN = −1.0 dBFS, DCS disabled, unless otherwise noted.

PARAMETER	TEMP	20MSps/40MSps			UNIT
		MIN	TYP	MAX	
CLOCK INPUT PARAMETERS					
Input Clock Rate	Full			160/320	MHz
Conversion Rate	Full	3		20/40	MSps
CLK Period-Divide-by-1 Mode (t_{CLK})		50/25			ns
CLK Pulse Width High (t_{CH})			25/12.5		ns
Aperture Delay (t_A)	Full		1.0		ns
Aperture Uncertainty (t_j)	Full		0.1		ps rms
DATA OUTPUT PARAMETERS					
Data Propagation Delay (t_{PD})	Full		3		ns
DCO Propagation Delay(t_{DCO})	Full		5		ns
DCO to Data Skew (t_{SKEW})	Full	0.1	0.3	0.6	ns
Pipeline Delay (Latency)	Full		9		Cycles
Wake-Up Time	Full		350		µs
OUT-OF-RANGE RECOVERY TIME	Full		2		Cycles

8.8 Timing Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to rising edge of CLK+ setup time		0.3		ns
t_{HSYNC}	SYNC to rising edge of CLK+ hold time		0.4		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

9 TIMING DIAGRAMS

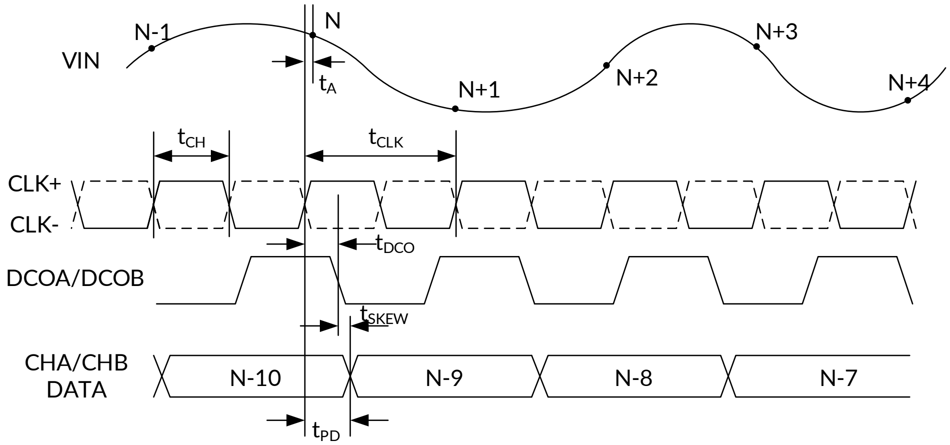


Figure 2. CMOS Output Data Timing

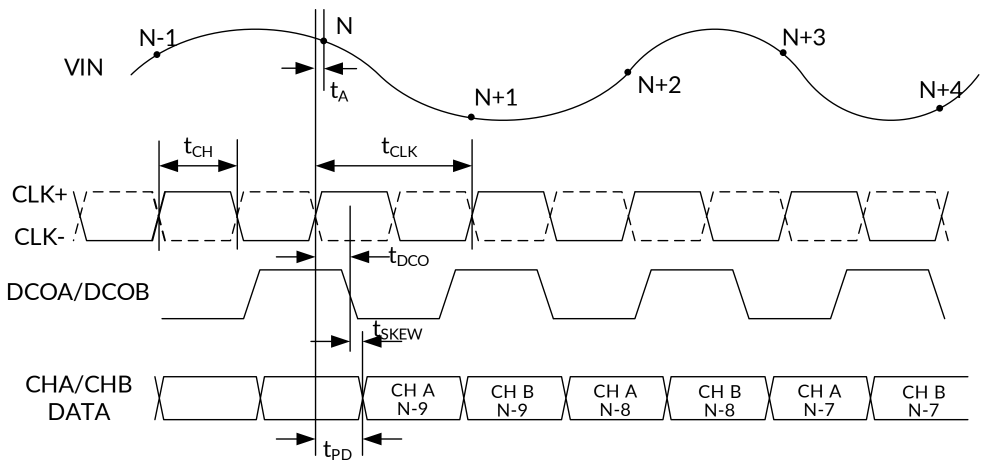


Figure 3. CMOS Interleaved Output Timing

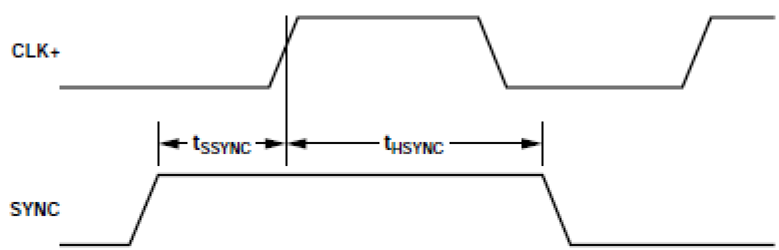


Figure 4. SYNC Input Timing Requirements

10 THEORY OF OPERATION

10.1 Analog Input Considerations

For baseband applications below ~10 MHz where SNR is a key parameter, differential transformer-coupling is the recommended input configuration. An example is shown in Figure 5. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

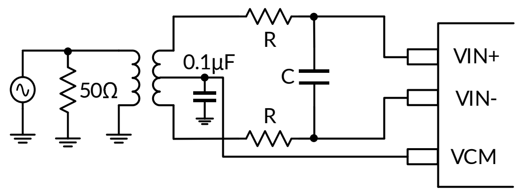


Figure 5. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.
At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the RS1522. For applications above ~10 MHz where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 6).
In any configuration, the value of Shunt Capacitor C is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 1 displays the suggested values to set the RC network. However, these values are dependent on the input signal and should be used only as a starting guide.

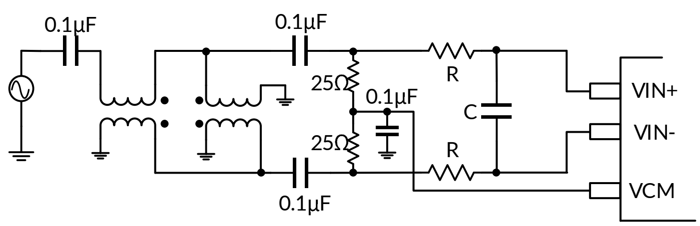


Figure 6. Differential Double Balun Input Configuration

Table 1. Example RC Network

Frequency Range /MHz	R Series /Ω	C Differential /pF
0-70	33	22
70-200	125	-

10.2 Clock Input Considerations

For optimum performance, clock the RS1522 sample clock inputs, CLK+ and CLK−, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally (see Figure 7) and require no external bias.

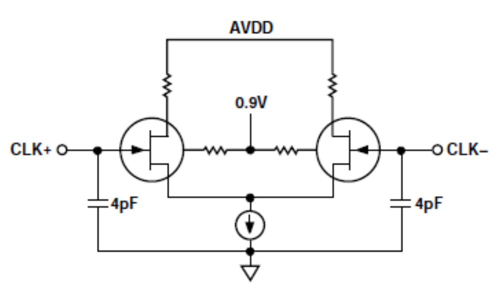


Figure 7. Equivalent Clock Input Circuit

The RS1522 has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern.
Figure 8 and Figure 9 show two preferred methods for clocking the RS1522 (at clock rates up to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun. The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200MHz. The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the RS1522 to approximately 0.8 V pp differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the RS1522 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

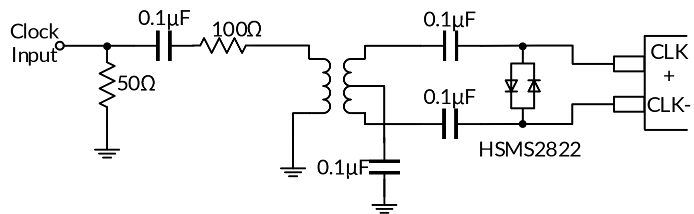


Figure 8. Transformer-Coupled Differential Clock (Up to 200 MHz)

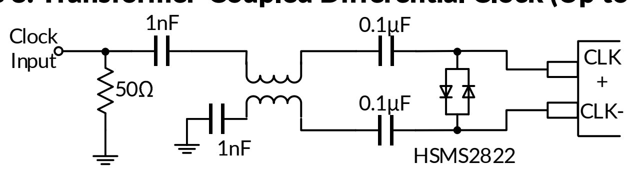


Figure 9. Balun-Coupled Differential Clock (Up to 625 MHz)

10.3 Reference Configuration

A comparator within the RS1522 detects the potential at the SENSE pin and configures the reference into four possible modes, which are summarized in Table 2. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider, setting VREF to 1.0 V.
If a resistor divider is connected external to the chip, as shown in Figure 10, the switch again sets to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output, defined as follows:

$$VREF = 0.5 \times \left(1 + \frac{R2}{R1} \right)$$

The input range of the ADC always equals twice the voltage at the reference pin (VREF) for either an internal or an external reference.

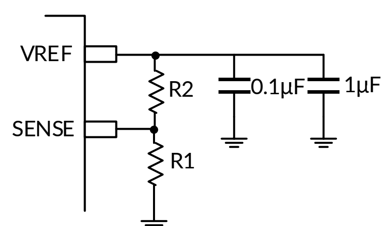


Figure 10. Programmable Reference Mode

Table 2. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (Vpp)
External Reference	AVDD	N/A	2 × external reference
Internal Fixed Reference	VREF	0.5	1.0
Internal Fixed Reference	0.2V to VREF	0.5×(1+R2/R1)	2 × VREF
Internal Fixed Reference	AGND to 0.2V	1.0	2.0

10.4 Digital Outputs

The RS1522 output drivers can be configured to interface with 1.8 V to 3.3 V CMOS logic families. Output data can also be multiplexed onto a single output bus to reduce the total number of traces required. The CMOS output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies and may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches. The output data format can be selected to be either offset binary or twos complement by setting the SCLK/DFS pin when operating in the external pin mode (see Table 3). The data format can be selected for offset binary, twos complement, gray code or random code when using the SPI control.

Table 3. SCLK, SDIO External Pin Mode

Voltage at Pin	SCLK/DFS	SDIO/DCS
AGND	Offset binary (default)	DCS disabled (default)
DRVDD	Twos complement	DCS enabled

Table 4. Output Data Format

Input (V)	Condition	Offset Binary	Twos Complement	OR
VIN+ - VIN-	< -VREF – 0.5LSB	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ - VIN-	= -VREF	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ - VIN-	= 0	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ - VIN-	= +VREF – 1LSB	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ - VIN-	> +VREF – 0.5LSB	11 1111 1111 1111	01 1111 1111 1111	1

11 SERIAL PORT INTERFACE (SPI)

The RS1522 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section.

11.1 Configuration Using The SPI

Three pins define the SPI of this ADC: the SCLK, the SDIO, and the CSB (see Table 5). The SCLK (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) is an active-low control that enables or disables the read and write cycles.

Table 5. Serial Port Interface Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.
SDIO	Serial Data Input/Output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame
CSB	Chip Select Bar. An active-low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing can be found in Figure 11.
Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in high impedance mode. This mode turns on any SPI pin secondary functions. During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits, as shown in Figure 11. All data is composed of 8-bit words.
The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame. In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

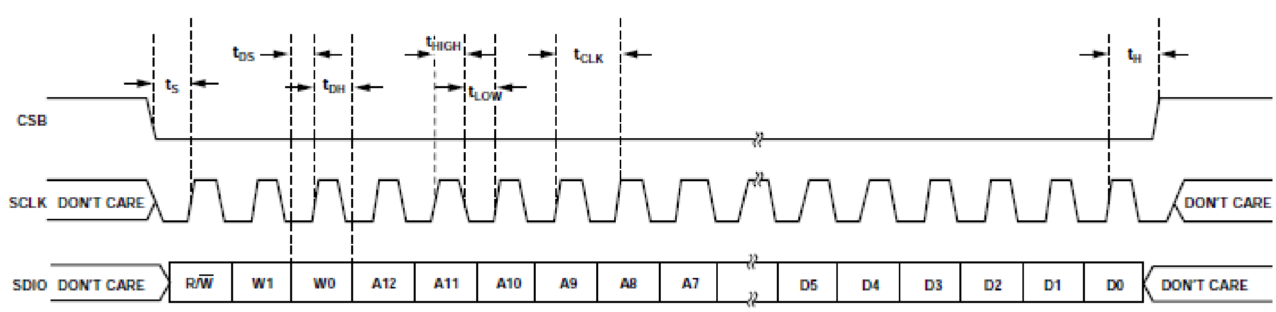


Figure 11. Serial Port Interface Timing Diagram

11.2 Configuration Without The SPI

In applications that do not interface to the SPI control registers, the SDIO/DCS pin, the SCLK/DFS pin, the OEB pin, and the PDWN pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer, output data format, output enable, and power-down feature control. In this mode, connect the CSB chip select to DRVDD, which disables the serial port interface.

Table 6. Mode Selection

Pin	External Voltage	Configuration
SDIO/DCS	DRVDD	Duty cycle stabilizer enabled
	AGND (default)	Duty cycle stabilizer disabled
SCLK/DFS	DRVDD	Twos complement enabled
	AGND (default)	Offset binary enabled
OEB	DRVDD	Outputs in high impedance
	AGND (default)	Outputs enabled
PDWN	DRVDD	Chip in power-down or standby
	AGND (default)	Normal operation

12 MEMORY MAP REGISTER TABLE:

Writes to the addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and then the bit auto clears.

Table 7. REGISTER TABLE

Addr. A7-0 HEX	Register Name	Def. Value	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Notes/ Comments
Chip configuration registers											
0x00	SPI port configuration	18	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	The nibbles are mirrored.
0x01	Chip ID	23	8-bit chip ID (RS1522=0x23)								Read only
0x02	Chip grade			Speed grade ID 000 =20M, 001=40M 010 =65M							Unique speed grade ID used to differentiate devices; read only
Device Index and Transfer Registers											
0x05	Channel index	03	0	0	0	0	0	0	Channel B	Channel A	Channel Selection
0xFF	Transfer	00	0	0	0	0	0	0	0	Transfer	Transfer control
Program registers											
0x08	Modes	80	External power-down enable (local)	External Pin function when high 00 = full power-down 01 = standby 10 = output disabled 11 = output enabled		0	0	0	00= chip run 01= full power-down 10= standby 11= chip run		Determines various generic modes of chip operation.
0x09	Globe Clock	00	0	0	0	0	0	0	0	DCS	
0x0B	Clock divider	00	0	0	0	0	0	000=1, 001=2, 010=3, 011=4, 100=5, 101=6, 110=7, 111=8			Clock division
0x0E	BIST enable	00	0	0	0	0	0	0	0	BIST enable	
0x10	Offset adjust	00	8-bit device offset adjustment, Bits[7:0] (local) Offset adjust in LSBs from +127 to −128 (twos complement format)								
0x14	Output mode	00	0=3.3V 1=1.8V	0	Output mux enable	Output enable	Output Lower Power	Output invert	00=offset binary 01=twos complement 10=gray code 11=random code		Configures the outputs and the format of the data.
0x15	Output adjust	22	DCO3V3_ drive<1:0>		DCO1V8_ drive<1:0>		Data3V3_ drive<1:0>		Data1V8_ drive<1:0>		Determines CMOS output drive strength properties.
16	Output phase	00	DCO output polarity 0 = normal 1 = inv	0	0	0	0	Input clock phase adjust, Bits[2:0] (Value is number of input clock cycles of phase delay) 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles			On devices that use global clock divide, deter mines which phase of the

								011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles 111 = 7 input clock cycles			divider output is used to supply the output clock; internal latching is unaffected.
17	DCO output delay	00	0	0	0		DCO delay, Bits[2:0] 000 = 0.56 ns 001 = 1.12 ns 010 = 1.68 ns 011 = 2.24 ns 100 = 2.80 ns 101 = 3.36 ns 110 = 3.92 ns 111 = 4.48 ns				DCO output delay control
18	VREF select	c0	11=2Vpp (default) 10=1.75Vpp 01=1.5Vpp 00=1.25Vpp		0	0	0	0	0	0	Reference voltage selection, affecting the full range
100	Sync control	00	0	0	0	0	0	Clock divider next sync only	Clock divider sync enable	Master sync enable	

13 SYNC CONTROL

Bit 2—Clock Divider Next Sync Only:

If the master sync enable bit (Address 0x100, Bit 0) and the clock divider sync enable bit (Address 0x100, Bit 1) are high, Bit 2 allows the clock divider to sync to the first sync pulse it receives and to ignore the rest. The clock divider sync enable bit (Address 0x100, Bit 1) resets after it syncs.

Bit 1—Clock Divider Sync Enable:

Bit 1 gates the sync pulse to the clock divider. The sync signal is enabled when Bit 1 and Bit 0 are high and the device is operating in continuous sync mode as long as Bit 2 of the sync control is low.

Bit 0—Master Sync Enable:

Bit 0 must be high to enable any of the sync functions.

14 APPLICATIONS INFORMATION

14.1 Design Guidelines

Before starting the design and layout of the RS1522 as a system, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

14.2 Power and Ground Recommendations

When connecting power to the RS1522, it is strongly recommended that two separate supplies be used. Use one 1.8 V supply for analog (AVDD); use a separate 1.8 V to 3.3 V supply for the digital output supply (DRVDD). If a common 1.8 V AVDD and DRVDD supply must be used, the AVDD and DRVDD domains must be isolated with a ferrite bead or filter choke and separate decoupling capacitors. Several different decoupling capacitors can be used to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length. A single PCB ground plane should be sufficient when using the RS1522. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved. When powering down the RS1522, power off AVDD and DRVDD simultaneously, or DRVDD must be removed before AVDD.

14.3 CMOS Drivers Control

The CMOS output drivers of RS1522 are controlled by **register** 0x14<7> and 0x15. The stronger drive, the more power. In lower sampling rate such as lower than 20MSps, setting 0x14<3>=1 could reduce the drive and achieve lower power consumptions of the output drivers.
The timing between DCO and digital outputs of the RS1522 should always be paid attention. This is the key to acquire the right digital outputs.

14.4 Exposed Paddle Thermal Heat Sink Recommendations

The exposed paddle (Pin 0) is the only ground connection for the RS1522; therefore, it must be connected to analog ground (AGND) on the customer's PCB. To achieve the best electrical and thermal performance, mate an exposed (no solder mask) continuous copper plane on the PCB to the RS1522 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. Fill or plug these vias with nonconductive epoxy. Data Sheet To maximize the coverage and adhesion between the ADC and the PCB, a silkscreen should be overlaid to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB.

14.5 VCM

The VCM pin should be decoupled to ground with a 0.1µF capacitor, as shown in Figures 5 and 6.

14.6 RBIAS

The RS1522 requires that a 10 kΩ resistor be placed between the RBIAS pin and ground. This resistor sets the master current reference of the ADC core and should have at least a 1% tolerance.

14.7 Reference Decoupling

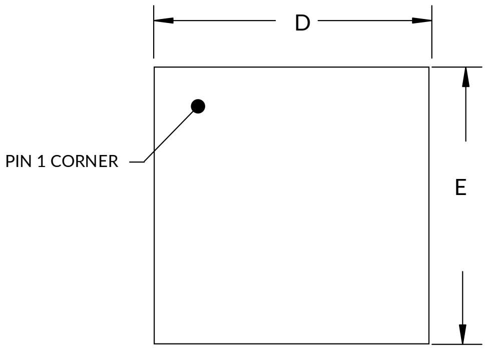
Externally decouple the VREF pin to ground with a low ESR, 1.0µF capacitor in parallel with a low ESR, 0.1µF ceramic capacitor.

14.8 SPI Port

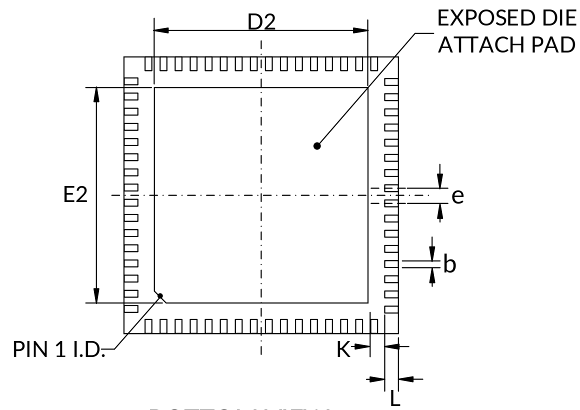
The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the RS1522 to keep these signals from transitioning at the converter inputs during critical sampling periods.

15 PACKAGE OUTLINE DIMENSIONS

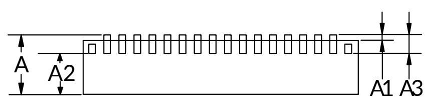
QFN9X9-64 (4)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.800	0.900	0.032	0.035
A1	0.000	0.050	0.000	0.002
A2	0.650		0.026	
A3	0.203 REF (2)		0.008 REF (2)	
b	0.200	0.300	0.008	0.012
D (1)	9.000 BSC (3)		0.354 BSC (3)	
E (1)	9.000 BSC (3)		0.354 BSC (3)	
e	0.500 BSC (3)		0.020 BSC (3)	
D2	7.100	7.300	0.280	0.287
E2	7.100	7.300	0.280	0.287
L	0.300	0.500	0.012	0.020
K	0.500 REF (2)		0.020 REF (2)	

NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
4. This drawing is subject to change without notice.

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