1A, Low Noise, Ultra High PSRR, Low-Dropout Linear Regulator

1 FEATURES

- **Input Voltage Range: 2.2V to 6V**
- **Output Voltage Range:**
  - **Fixed Option: 0.8V, 1.0V, 1.2V, 1.8V, 2.5V, 3V, 3.3V and 5.0V**
  - **Adjustable Option: 0.8V to 5.5V**
- **Up to 1A Load Current**
- **High PSRR: 66dB at 1kHz, 33dB at 1MHz**
- **Excellent Noise Immunity**
- **Very Low Dropout: 175mV Typical at 1A**
- **−40°C to 125°C Operating Junction Temperature Range**
- **Fast Response Over Load and Line Transient**
- **Stable with a 4.7μF Output Ceramic Capacitor**
- **Accurate Output Voltage ±3% over Line Regulation, Load Regulation, and Operating Temperature Range**
- **Enable Control**
- **Over-Current Protection**
- **Over-Temperature Protection**

2 APPLICATIONS

- **Telecom/Networking Cards**
- **Motherboards/Peripheral Cards**
- **Industrial Applications**
- **Wireless Infrastructures**
- **Set-Top Boxes**
- **Medical Equipments**
- **Notebook Computers**
- **Battery Powered Systems**

3 DESCRIPTIONS

The RS3242 is a high performance positive low dropout (LDO) regulator designed for applications requiring very low dropout voltage and ultra-high Power Supply Ripple Rejection (PSRR) at up to 1A. The input voltage range is from 2.2V to 6V and the output voltage is programmable as low as 0.8V. A P-MOSFET switch provides excellent transient response with just a 4.7μF ceramic output capacitor. The external enable control effectively reduces power dissipation while shutdown and further output noise immunity is achieved through bypass capacitor on NR pin.

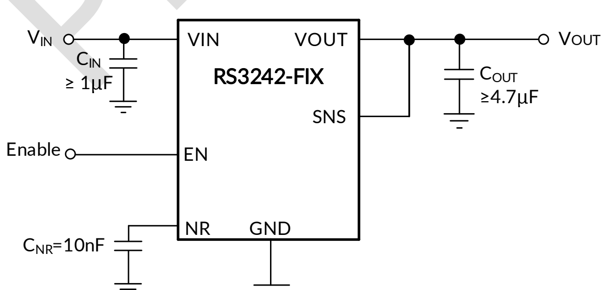
The device is available in the DFN3X3-8 package and is specified from −40°C to 125°C.

Device Information (1)

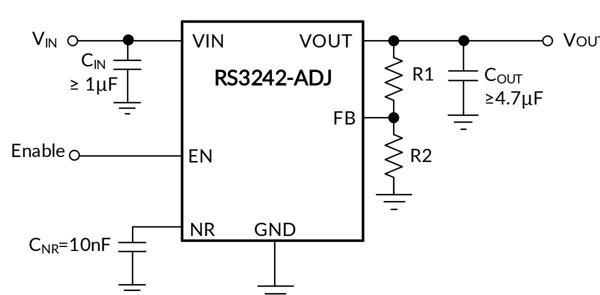
PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS3242	DFN3X3-8	3.00mm×3.00mm

(1) For all available packages, see the orderable addendum at the next page of the data sheet.

4 TYPICAL APPLICATION



Fixed Voltage Typical Application Circuit



Adjustable Voltage Typical Application Circuit

5 FUNCTIONAL BLOCK DIAGRAM

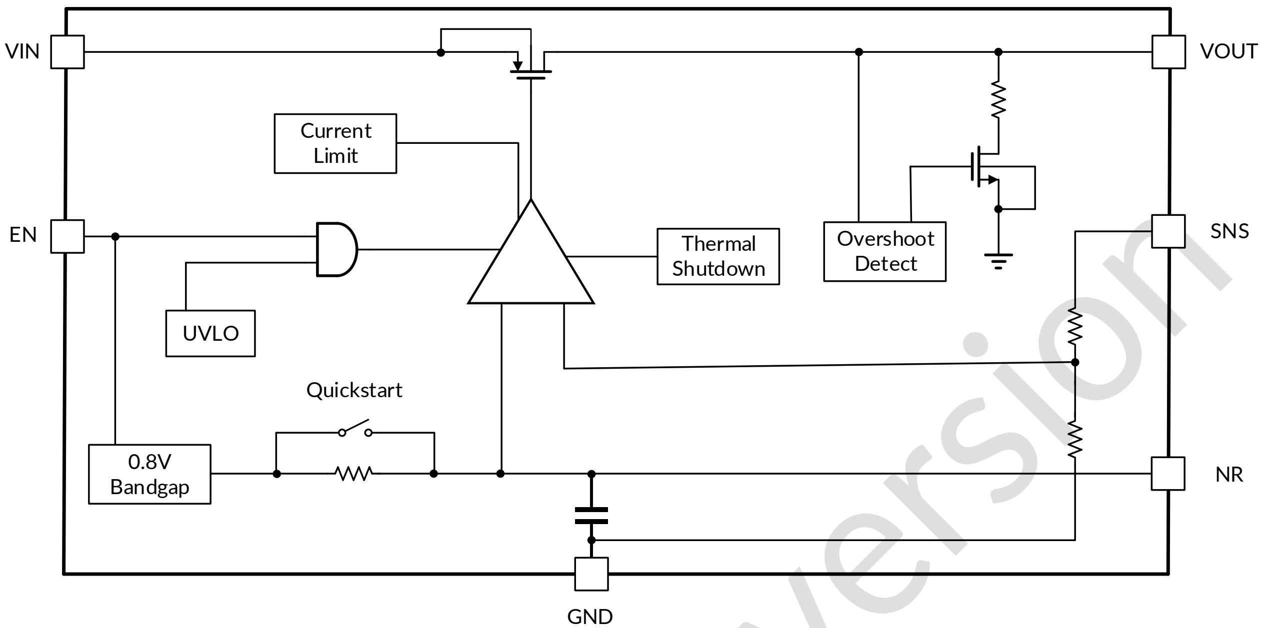


Figure 1. Fixed Voltage Version

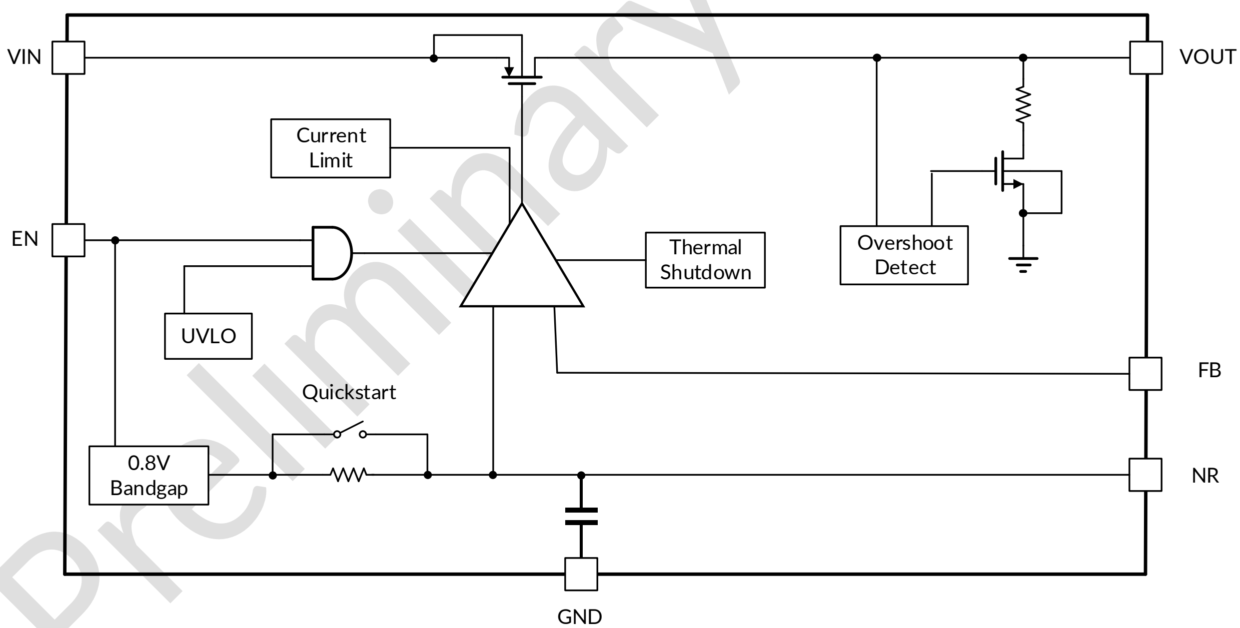


Figure 2. Adjustable Voltage Version

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6 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2024/12/17	Preliminary version completed
A.0.1	2025/07/18	1. Update PACKAGE/ORDERING INFORMATION 2. Modify PIN CONFIGURATION AND FUNCTIONS 3. Update KEY PARAMETER LIST OF TAPE AND REEL
A.0.2	2025/09/28	Change DFN3X3-8 PACKAGE OUTLINE DIMENSIONS
A.0.3	2026/03/31	1. Update FEATURES and TYPICAL APPLICATION on Page 1 2. Add Fixed Voltage Version FUNCTIONAL BLOCK DIAGRAM on Page 2 3. Update Parameter values in SPECIFICATIONS on Page 7 to 9 4. Update Figure 3 and Figure 16 in Typical Characteristics on Page 10 and 12 5. Update FEATURE DESCRIPTION

7 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	V_{OUT}(V)	V_{OUT} Accuracy	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS3242	RS3242-0.8XDC8	0.8	±3%	DFN3X3-8	RS3242A	MSL3	Tape and Reel, 5000
	RS3242-1.0XDC8	1.0	±3%	DFN3X3-8	RS3242B	MSL3	Tape and Reel, 5000
	RS3242-1.2XDC8	1.2	±3%	DFN3X3-8	RS3242C	MSL3	Tape and Reel, 5000
	RS3242-1.8XDC8	1.8	±3%	DFN3X3-8	RS3242D	MSL3	Tape and Reel, 5000
	RS3242-2.5XDC8	2.5	±3%	DFN3X3-8	RS3242E	MSL3	Tape and Reel, 5000
	RS3242-3.0XDC8	3.0	±3%	DFN3X3-8	RS3242F	MSL3	Tape and Reel, 5000
	RS3242-3.3XDC8	3.3	±3%	DFN3X3-8	RS3242G	MSL3	Tape and Reel, 5000
	RS3242-5.0XDC8	5.0	±3%	DFN3X3-8	RS3242H	MSL3	Tape and Reel, 5000
	RS3242-ADJ8XDC8	ADJ	±3%	DFN3X3-8	RS3242K	MSL3	Tape and Reel, 5000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

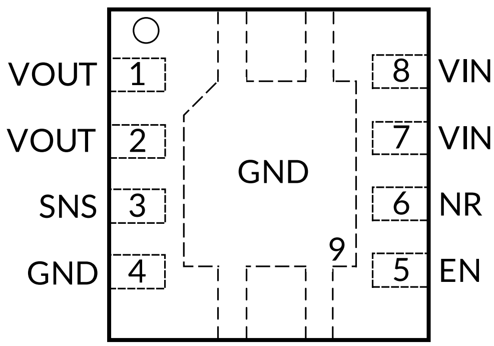
(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

8 PIN CONFIGURATION AND FUNCTIONS

RS3242-Fixed Output

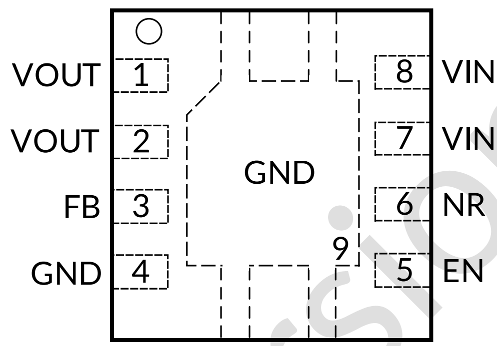
TOP VIEW



DFN3X3-8

RS3242-ADJ

TOP VIEW



DFN3X3-8

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 2	VOUT	Output of the regulator. Decouple this pin to GND with at least 4.7μF for stability.
3	FB	Feedback voltage input. This pin is used to set the desired output voltage via an external resistive divider. The feedback reference voltage is 0.8V typically.
	SNS	Output Voltage Sense Input Pin (fixed voltage version only). Connect this pin to the load side of the output trace only in the fixed voltage version
4, 9 (Exposed Pad)	GND	System ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	EN	Enable control input. Connecting this pin to logic high enables the regulator or driving this pin low puts it into shutdown mode. EN can be connected to IN if not used. (EN pin is not allowed to be left floating.)
6	NR	Noise reduction input. Decouple this pin to GND with an external capacitor can not only reduce output noise to very low levels but also slow down the VOUT rise like a soft-start behavior.
7, 8	VIN	Supply input. A minimum of 1μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection.

9 SPECIFICATIONS

9.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{IN}	Input Voltage		-0.3	7	V
V_{EN}	Enable Input Voltage		-0.3	7	V
I_{OUT}	Current		Internally limited		A
$θ_{JA}$	Package Thermal Impedance (2)	DFN3X3-8		53	°C/W
T_J	Junction Temperature (3)		-40	150	°C
T_{stg}	Storage Temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) $θ_{JA}$ is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. $θ_{JC}$ is measured at the exposed pad of the package.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{θJA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{θJA}$. All numbers apply for packages soldered directly onto a PCB.

9.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), ANSI/ESDA/JEDEC JS001-2024	±2000	V
		Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1000	V

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input Voltage Range on V_{IN}	2.2	6	V
V_{OUT}	Output Voltage	0.8	5.5	V
I_{OUT}	Output Current Range on I_{OUT}	0	1000	mA
C_{OUT}	Output Capacitor	4.7	100	µF
C_{NR}	Noise Reduction Capacitor	1	100	nF
T_J	Junction Temperature	-40	125	°C

9.4 Electrical Characteristics

Over operating temperature range (−40°C ≤ T_J ≤ 125°C), V_{IN}=V_{OUT}(nom)+0.5V or 2.2V, V_{OUT} = 0.8V and 5.5V, I_{OUT} = 1mA, V_{EN} = 2.2V, C_{NR} = 10nF, C_{OUT} = 4.7µF, (unless otherwise noted); typical values are at T_J=25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY AND CURRENTS						
Input Voltage (1)	V_{IN}		2.2		6	V
Under Voltage Lockout	UVLO	V_{IN} rising		2.1		V
Hysteresis	V_{HYS}	V_{IN} falling		200		mV
Quiescent Current	I_Q	V_{EN} = 1.2V, I_{OUT} = 0mA		125		µA
Ground Pin Current	I_{GND}	V_{EN} = 1.2V, I_{OUT} = 1A, V_{OUT}=3.3V		1		mA
Shutdown Current	I_{SD}	V_{EN} = 0V, V_{IN}=6V		0.01	1	µA
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT}		0.8		5.5	V
Feedback Voltage	V_{FB}	Adjustable Version, T_J=25°C, I_{OUT}=1mA		0.8		V
Feedback Pin Current	I_{FB}	Adjustable Version, V_{FB}=0.9V		0.001	0.05	µA
DC Output Accuracy (1)	ΔV_{OUT}	V_{IN} = $V_{OUT(nom)}$+0.5V to 5V, I_{OUT} =1mA to 500mA		±2		%
		V_{IN} = $V_{OUT(nom)}$+0.5V to 6V, I_{OUT} =1mA to 1A		±3		%
Line Regulation (1)	$\Delta V_{OUT(\Delta VIN)}$	V_{IN} = V_{OUT} + 0.5V to 6V, I_{OUT} = 1mA		0.2		%/V
Load Regulation (1)	$\Delta V_{OUT(\Delta IOUT)}$	V_{IN} =V_{OUT} +0.5V, I_{OUT} = 1mA to 1A		20		mV
Output Voltage Temperature Coefficient (4)	$\frac{\Delta V_{OUT}}{\Delta T_A \times V_{OUT}}$	T_J = -40°C ~+85°C, I_{OUT} = 1mA		80		ppm/°C
		T_J = -40°C ~+125°C, I_{OUT} = 1mA		70		ppm/°C
Maximum Output Current (5)	I_{OUTMAX}		1			A
DROPOUT VOLTAGE						
Dropout Voltage (6)	V_{DO}	I_{OUT} = 1A; Adjustable Only, V_{IN}=2.2V, FB=GND		320		mV
		I_{OUT} = 1A; V_{OUT} = 3.3V		230		mV
		I_{OUT} = 1A; V_{OUT} = 5.0V		175		mV
POWER SUPPLY REJECTION RATIO AND NOISE						
Power Supply Rejection Ratio (7)	PSRR	V_{IN} = 4.3V, V_{OUT} = 3.3V, C_{NR} = 10nF, I_{OUT} = 750mA; f = 100Hz		65		dB
		f = 1KHz		66		dB
		f = 10KHz		49		dB
		f = 100KHz		40		dB
		f = 1MHz		33		dB
Output Noise Voltage (7)	V_N	BW= 10Hz to 100kHz, V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 100mA; C_{NR} = 1nF		70		µV_{RMS}
		C_{NR} = 10nF		37		µV_{RMS}
		C_{NR} = 100nF		30		µV_{RMS}
ENABLE AND STARTUP TIME						
EN Input Logic High Voltage	V_{IH}	V_{IN} = 2.2V to 6V, EN rising	1.2			V
EN Input Logic Low Voltage	V_{IL}	V_{IN} = 2.2V to 6V, EN falling			0.4	V
EN Input Leakage Current	I_{EN}	V_{IN}=6V, V_{EN}=0V			1	µA
		V_{IN}=6V, V_{EN}=6V		0.03	1	µA
Output discharge FET Rdson	R_{DIS}	V_{IN}=5V, V_{EN}<V_{IL} (output disable)		300		Ω
Startup Time	t_{STR}	V_{OUT} = 3.3V, I_{OUT}=10mA, C_{OUT} = 4.7µF; C_{NR} = 1nF		95		µs
		C_{NR} = 10nF		910		µs

PROTECTIONS						
Over Current Limit	I_{LMT}	V_{OUT} = 0.85 x V_{OUT}		1300		mA
Thermal Shutdown Threshold (7)	T_{SD}	Shutdown, temperature increasing		155		°C
		Reset, temperature decreasing		135		°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.2V, whichever is greater.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) Output voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.
(5) Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when V_{IN} < V_{OUT} + V_{DROP}.
(6) The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 2% below the value of V_{OUT} for V_{IN} = V_{OUT}nom+ 0.5V (1).
(7) Guaranteed by design and characterization, not a FT item.

9.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

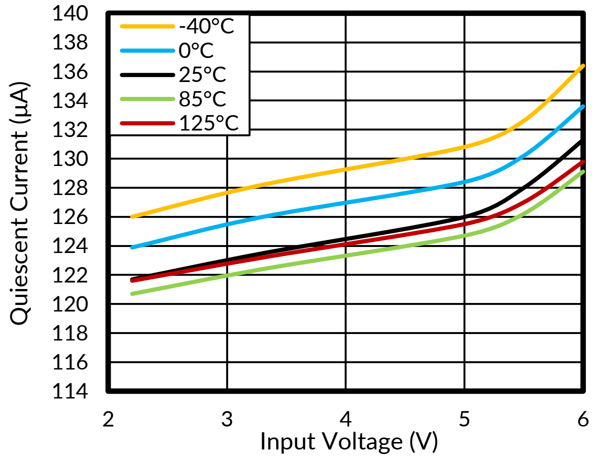


Figure 3. Quiescent Current vs Input Voltage

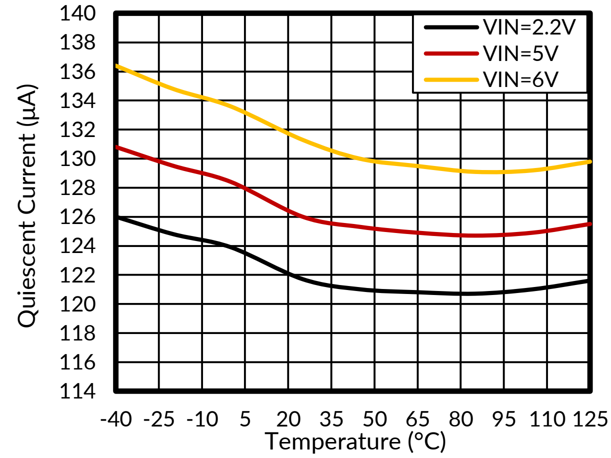


Figure 4. Quiescent Current vs Temperature

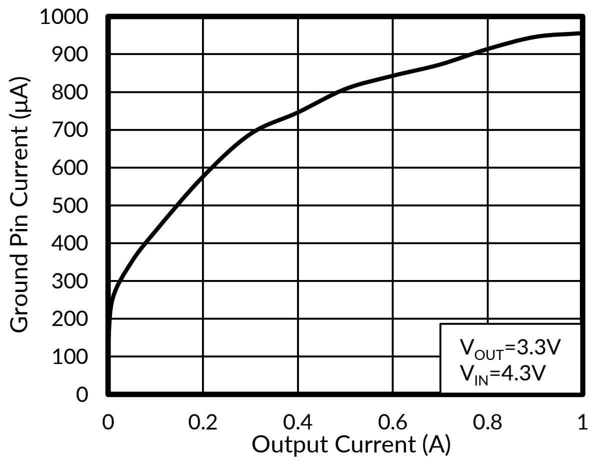


Figure 5. Ground Pin Current vs Output Current

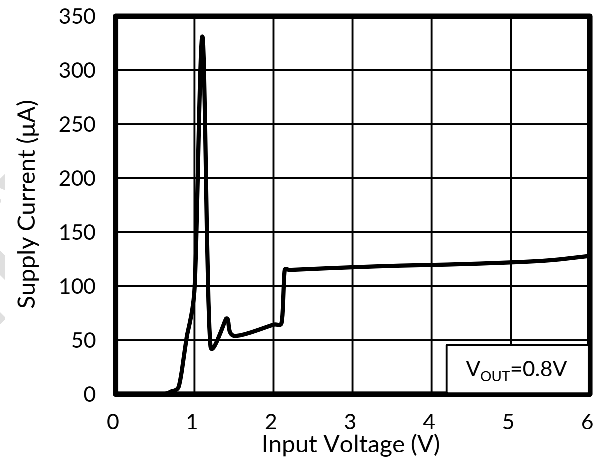


Figure 6. Supply Current vs Input Voltage

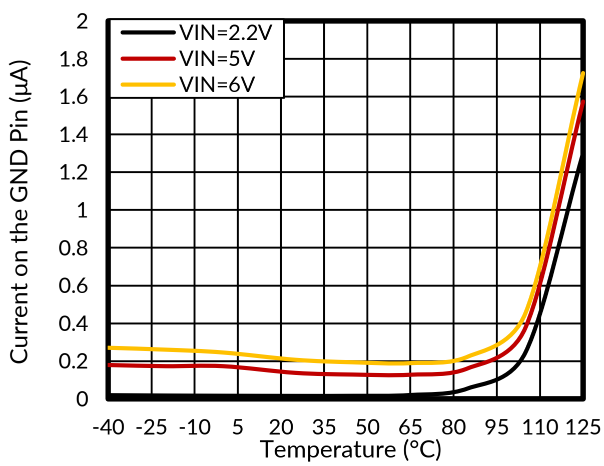


Figure 7. Shutdown Current vs Temperature

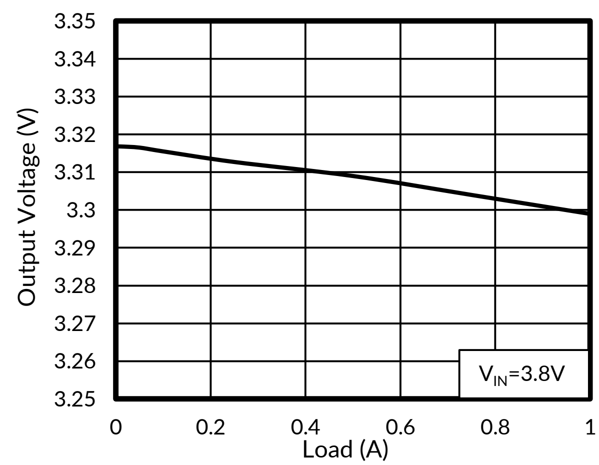


Figure 8. Load Regulation

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

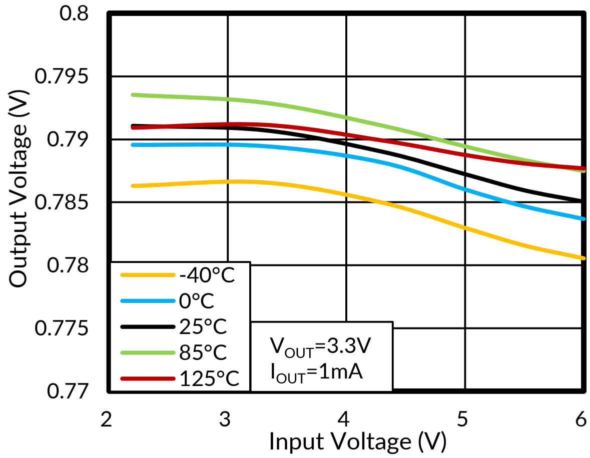


Figure 9. Line Regulation

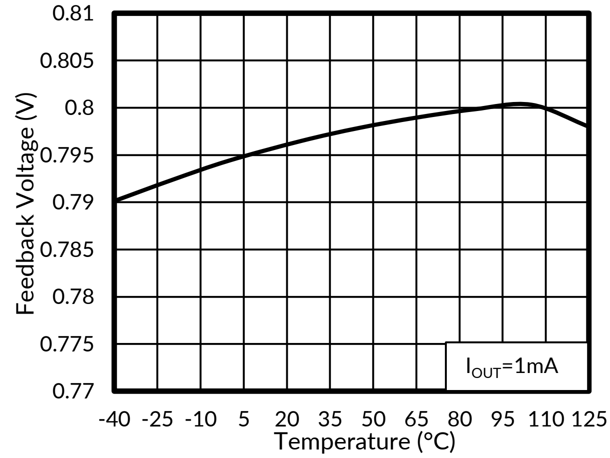


Figure 10. Feedback Voltage vs Junction Temperature

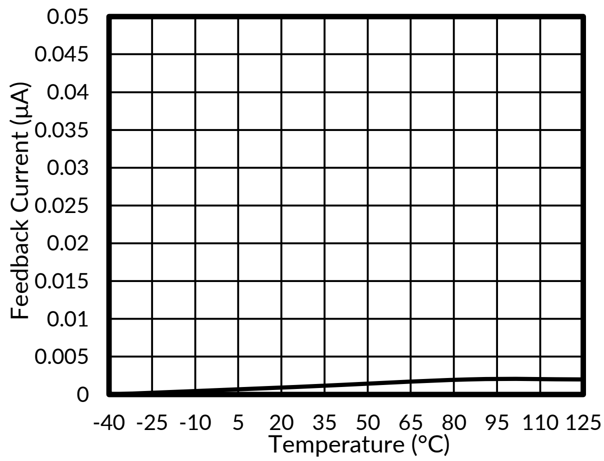


Figure 11. Feedback Pin Current vs Junction Temperature

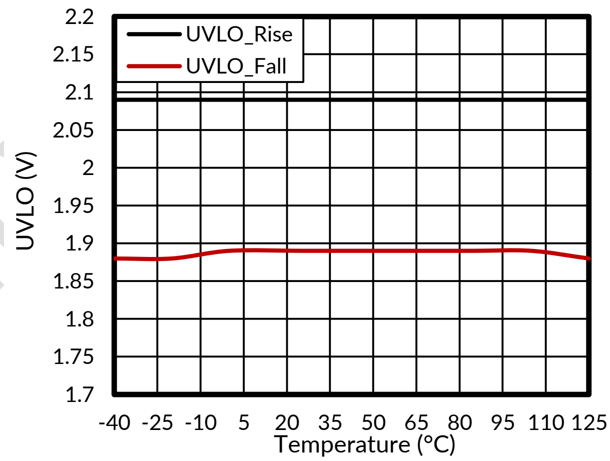


Figure 12. UVLO vs Junction Temperature

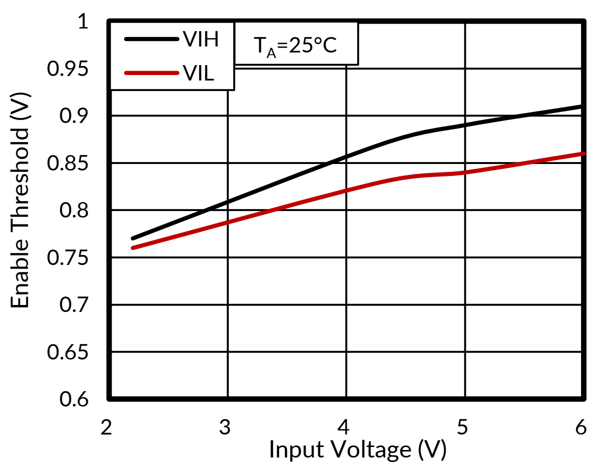


Figure 13. Enable Threshold vs Input Voltage

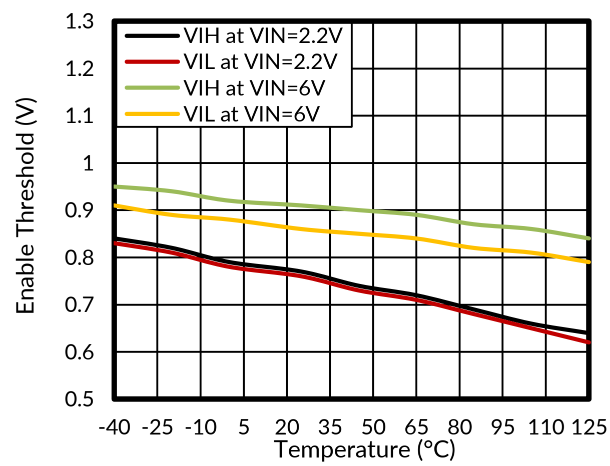


Figure 14. Enable Threshold vs Junction Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

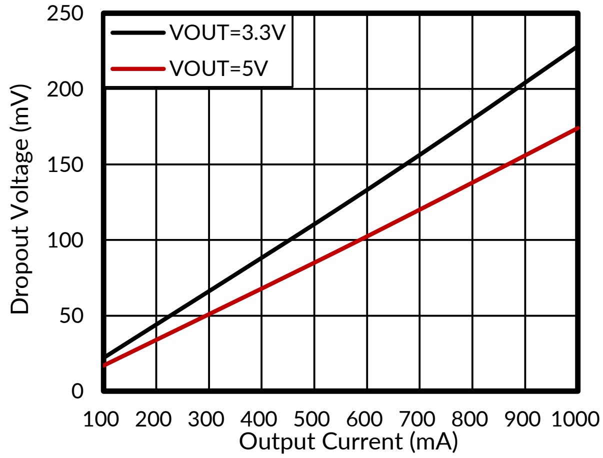


Figure 15. Dropout Voltage vs Output Current

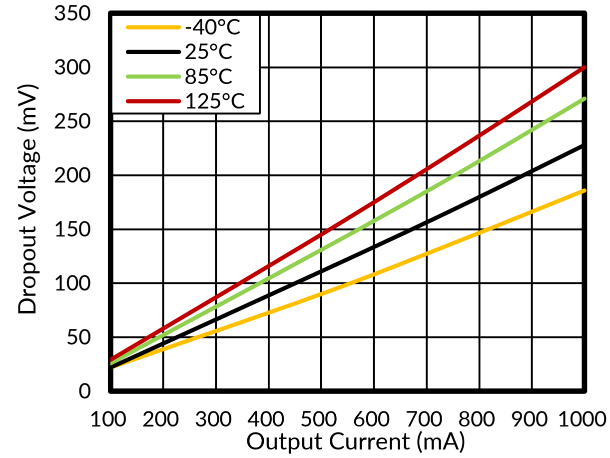


Figure 16. Dropout Voltage vs Output Current

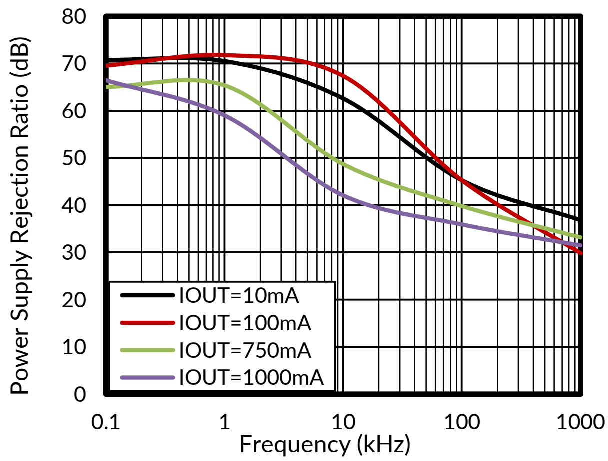


Figure 17. Power Supply Rejection Ratio vs Frequency

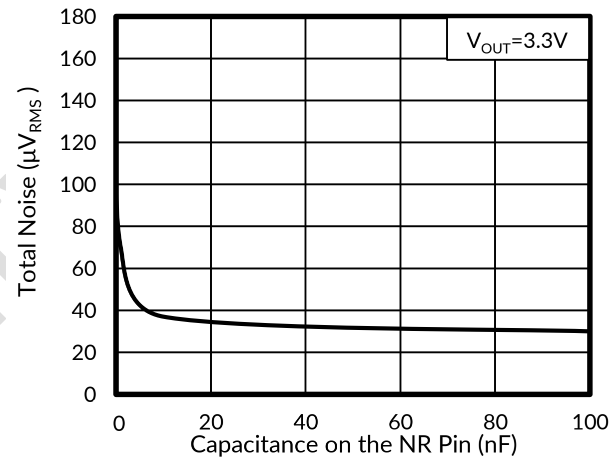


Figure 18. RMS Noise vs C_{NR}

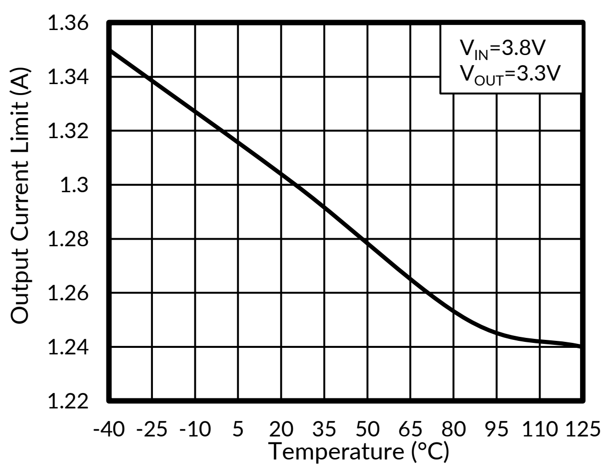


Figure 19. Output Current Limit vs Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

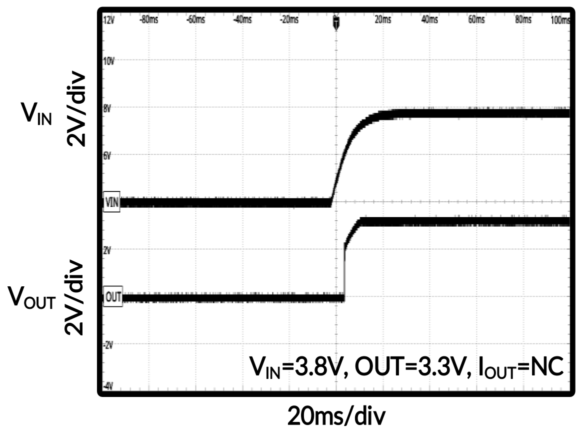


Figure 20. Power On

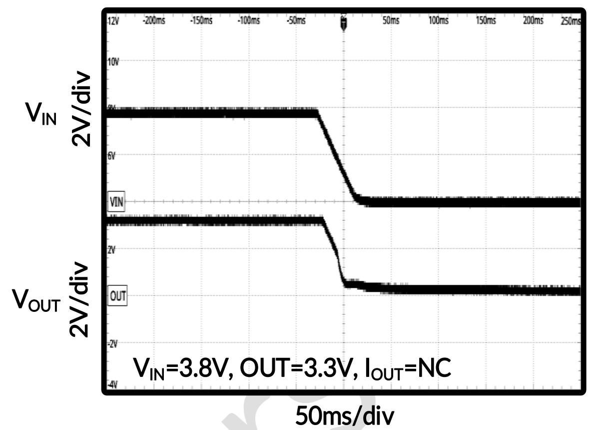


Figure 21. Power Off

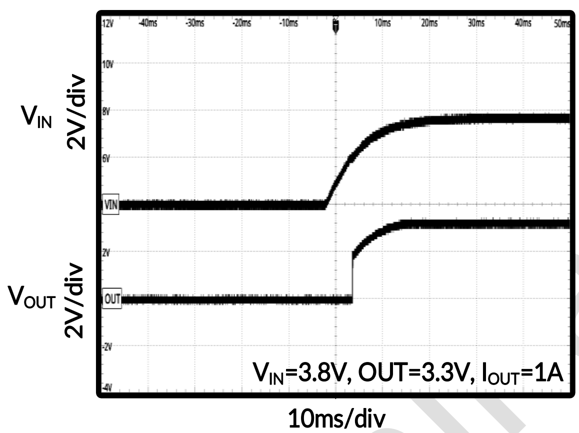


Figure 22. Power On

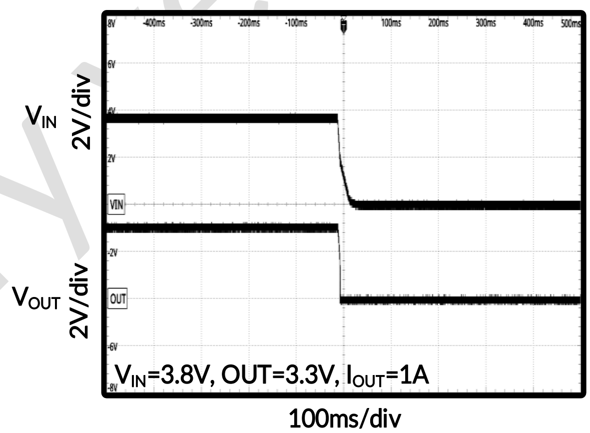


Figure 23. Power Off

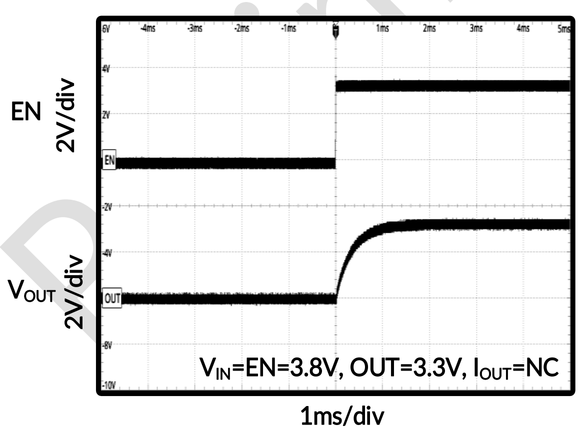


Figure 24. Turn On

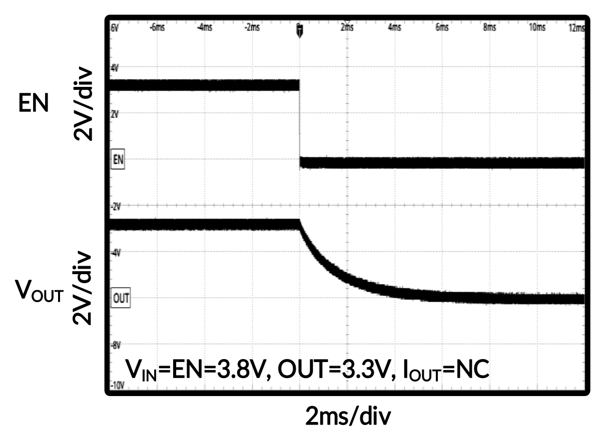
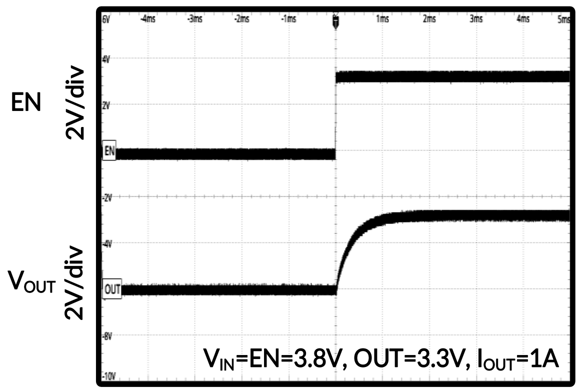


Figure 25. Turn Off

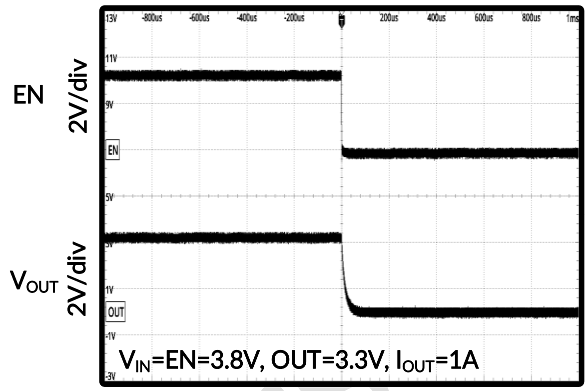
Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.



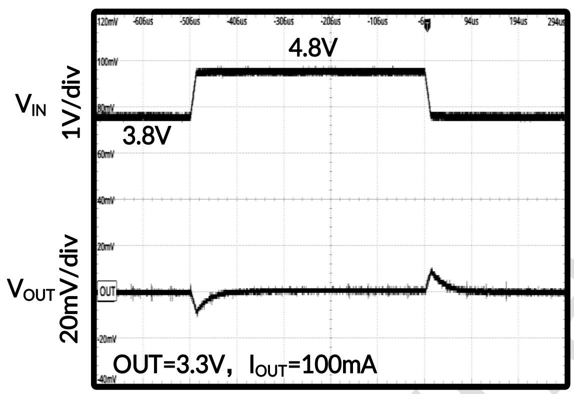
1ms/div

Figure 26. Turn On



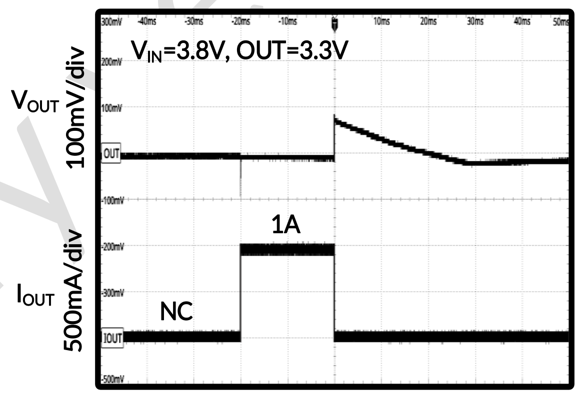
200µs/div

Figure 27. Turn Off



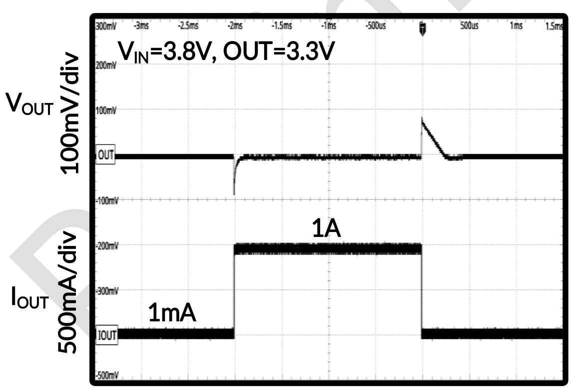
100µs/div

Figure 28. Line Transient Response



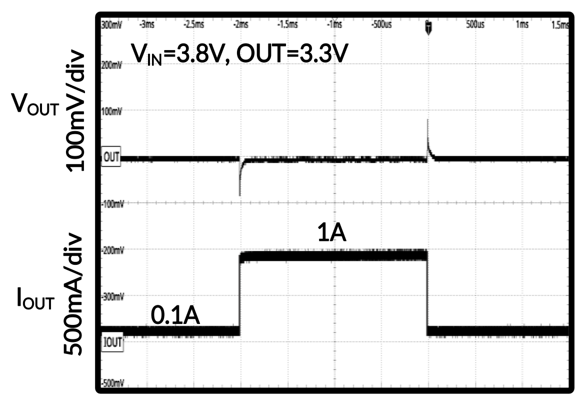
10ms/div

Figure 29. Load Transient Response



500µs/div

Figure 30. Load Transient Response



500µs/div

Figure 31. Load Transient Response

10 FEATURE DESCRIPTION

10.1 Overview

The RS3242 is a high performance positive low dropout (LDO) regulator designed for applications requiring very low dropout voltage and ultra-high Power Supply Ripple Rejection (PSRR) at up to 1A. The input voltage range is from 2.2V to 6V and the output voltage is programmable as low as 0.8V. A P-MOSFET switch provides excellent transient response with just a 4.7μF ceramic output capacitor. The external enable control effectively reduces power dissipation while shutdown and further output noise immunity is achieved through bypass capacitor on NR pin.

10.2 Undervoltage Lockout (UVLO)

The RS3242 family of devices uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

10.3 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, the EN pin can be connected to the VIN pin.

10.4 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 155°C which allows the device to cool. When the junction temperature cools to approximately 135°C, the output circuitry enables.

Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as aresult of overheating.

The thermal shutdown circuitry of the RS3242 has been designed to protect against temporary thermal overload conditions. The T_{SD} circuitry was not intended to replace proper heat-sinking. Continuously running the RS3242 device into thermal shutdown may degrade device reliability.

10.5 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO threshold minus V_{HYS}, or has not yet exceeded the UVLO threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold. When disenabled, the pull-down device behaves like a 300Ω resistor to ground.
- The device junction temperature is greater than the thermal shutdown temperature.

10.6 Internal Current-Limit

The RS3242 internal current-limit helps protect the regulator during fault conditions. During current-limit, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in current-limit for extended periods of time.
The RS3242 family of devices has a built-in body diode that conducts current when the voltage at the VOUT pin exceeds the voltage at the VIN pin. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting can be appropriate.

10.7 Startup and Noise Reduction Capacitor

The RS3242 family of devices uses a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}. This architecture allows the combination of very-low output noise and fast startup times. The NR pin is high impedance so a low-leakage C_{NR} capacitor must be used. Most ceramic capacitors are appropriate in this configuration. A high-quality, C0G-type (NP0) dielectric ceramic capacitor is recommended for C_{NR} when used in environments where abrupt changes in temperature can occur.

For better performance, a 10nF C0G-type (NP0) dielectric ceramic capacitor is strongly recommended for most applications.

10.8 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, connecting a minimum of 1µF low-equivalent series resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher value capacitor can be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the power source.

The RS3242 family of devices is designed to be stable with standard ceramic output capacitors of values 4.7µF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature.

10.9 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (1)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the Electrical Characteristics table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \le V_{OUT} / (I_{FB} \times 100) \quad (2)$$

11 POWER SUPPLY RECOMMENDATIONS

The device is designed to operate from an input voltage supply range between 2.2V and 6V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

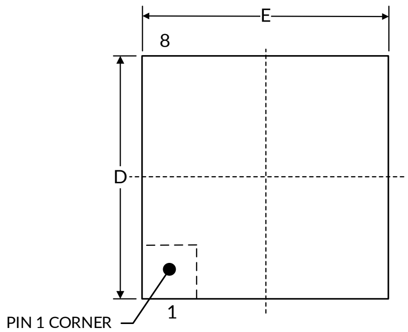
12 LAYOUT

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

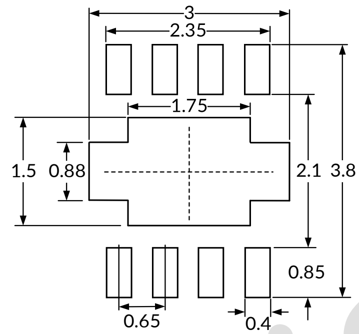
To improve ac performance (such as PSRR, output noise, and transient response), designing the board with separate ground planes for V_{IN} and V_{OUT} is recommended, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

13 PACKAGE OUTLINE DIMENSIONS

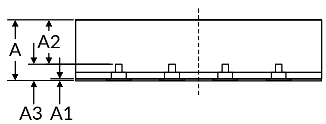
DFN3X3-8 (4)



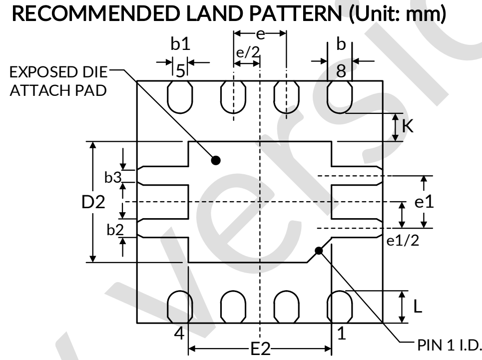
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



BOTTOM VIEW

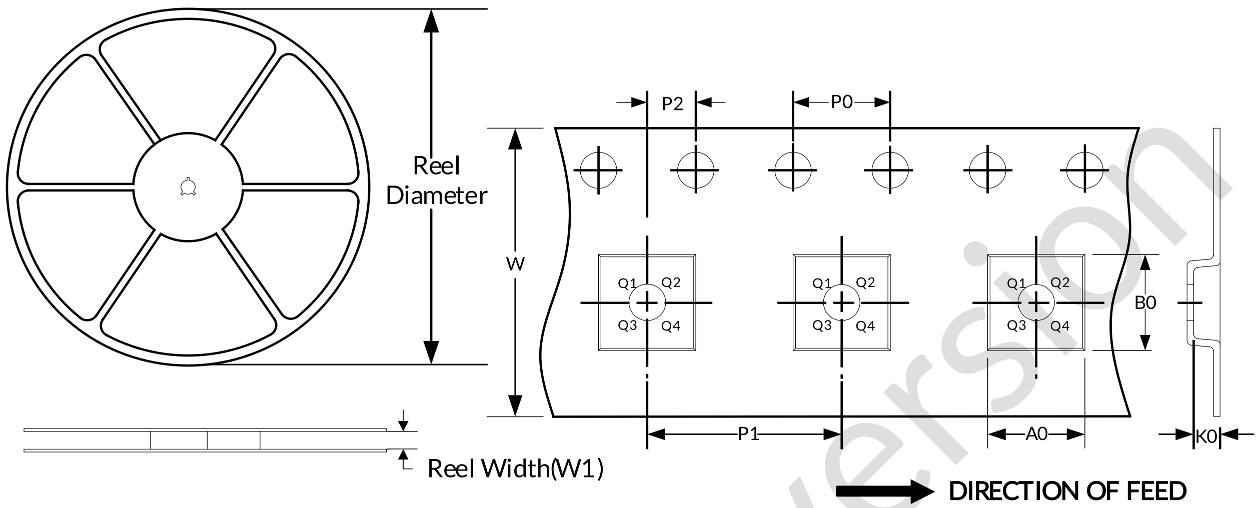
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.032
A1	0.000	0.050	0.000	0.002
A2	0.550 NOM		0.022 NOM	
A3	0.203 REF (2)		0.008 REF (2)	
b	0.250	0.350	0.010	0.014
b1	0.180 REF (2)		0.007 REF (2)	
b2	0.180	0.280	0.007	0.011
b3	0.150 REF (2)		0.006 REF (2)	
D (1)	3.000 BSC (3)		0.118 BSC (3)	
E (1)	3.000 BSC (3)		0.118 BSC (3)	
e	0.650 BSC (3)		0.026 BSC (3)	
e1	0.650 BSC (3)		0.026 BSC (3)	
D2	1.400	1.600	0.055	0.063
E2	1.650	1.850	0.065	0.073
L	0.300	0.500	0.012	0.020
K	0.350 REF (2)		0.014 REF (2)	

NOTE:
1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
4. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
DFN3X3-8	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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