16-Bit, 8-Channel, 250KSPS PulSAR ADCs

1 FEATURES

- **16-Bit Resolution with No Missing Codes**
- **8-Channel Multiplexer with Choice of Inputs**
- **Unipolar Single-Ended**
- **Differential (Gnd Sense)**
- **Pseudobipolar**
- **Throughput: 250 kSPS**
- **INL: ±1.5LSB Typical, ±3LSB Maximum (±23 ppm or FSR)**
- **Dynamic Range: 91.6dB**
- **Analog Input Range: 0 V to V_{REF} with V_{REF} Up to VDD**
- **Multiple Reference Types**
  - **Internal Selectable 2.5 V or 4.096 V**
  - **External Buffered (Up to 4.096 V)**
  - **External (Up to VDD)**
- **Internal Temperature Sensor (TEMP)**
- **Channel Sequencer, Selectable 1-Pole Filter, Busy Indicator**
- **No Pipeline Delay, SAR Architecture**
- **Single-Supply 2.3 V to 5.5 V Operation with 1.8 V to 5.5 V Logic Interface**
- **Serial Interface Compatible with SPI, MICROWIRE, QSPI, and DSP**
- **Power Dissipation**
  - **3.5 mW at 2.5 V/200 kSPS**
  - **14.6 mW at 5 V/250 kSPS**
- **Standby Current: 50 nA**
- **Low Cost Grade Available**

2 APPLICATIONS

- **Multichannel System Monitoring**
- **Battery-Powered Equipment**
- **Medical Instruments: ECG/EKG**
- **Mobile Communications: GPS**
- **Power Line Monitoring**
- **Data Acquisition**
- **Seismic Data Acquisition Systems**
- **Instrumentation**
- **Process Control**

3 DESCRIPTIONS

The RS1438 is 8-channel, 16-bit, charge redistribution successive approximation register (SAR) analog-to-digital converters (ADCs) that operate from a single power supply, VDD.

The RS1438 contains all components for using in a multichannel, low power data acquisition system, including a true 16-bit SAR ADC with no missing codes; a 8-channel low crosstalk multiplexer that is useful for configuring the inputs as single-ended (with or without ground sense), differential, or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and a buffer; a temperature sensor; a selectable one-pole filter; and a sequencer that is useful when channels are continuously scanned in order.

The RS1438 uses a simple serial port interface (SPI) for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level. Power dissipation scales with throughput.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1438	QFN4X4-20	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

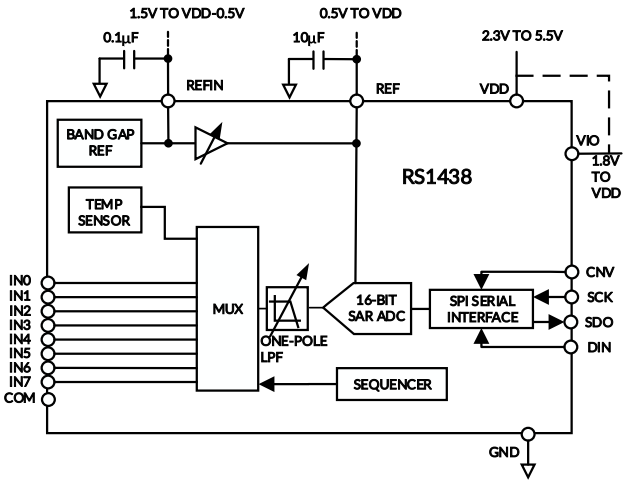

Figure 1. Functional Block Diagram

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2024/12/10	Preliminary version completed
A.0.1	2025/08/11	1. Update PACKAGE OPTION 2. Add KEY PARAMETER LIST OF TAPE AND REEL

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS1438	RS1438XTQR20	-40°C ~+125°C	QFN4X4-20	RS1438	MSL1	Tape and Reel, 3000

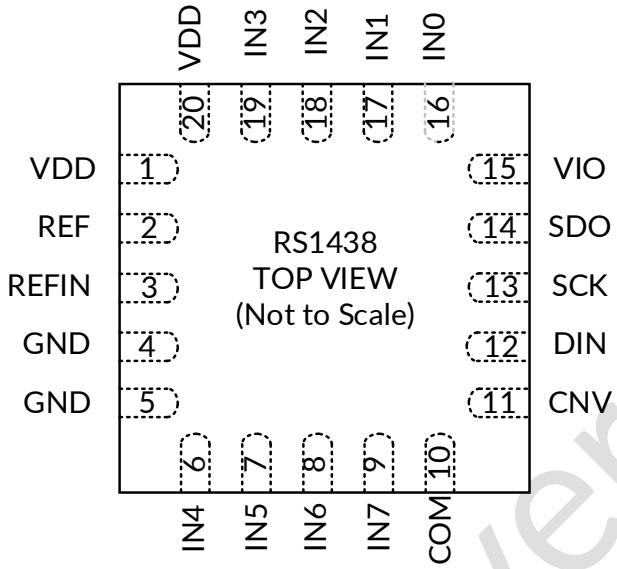
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 PIN CONFIGURATION AND FUNCTIONS



QFN4X4-20

PIN FUNCTIONS

PIN. NO	NAME	TYPE	DESCRIPTION
1, 20	VDD	P	Power Supply. Nominally 2.5 V to 5.5 V when using an external reference and decoupled with 10 µF and 100 nF capacitors. When using the internal reference for a 2.5 V output, the minimum must be 3.0 V. When using the internal reference for 4.096V output, the minimum must be 4.5 V
2	REF	AI/O	Reference Input/Output. See the Voltage Reference Output/Input section. When the internal reference is enabled, this pin produces a selectable system reference of 2.5 V or 4.096 V. When the internal reference is disabled and the buffer is enabled, REF produces a buffered version of the voltage present on the REFIN pin (VDD − 0.5 V, maximum), which is useful when using low cost, low power references. For improved drift performance, connect a precision reference to REF (0.5 V to VDD). For any reference method, this pin needs decoupling with an external 10 µF capacitor connected as close to REF as possible. See the Reference Decoupling section.
3	REFIN	AI/O	Internal Reference Output/Reference Buffer Input. See the Voltage Reference Output/Input section. When using the internal reference, the internal unbuffered reference voltage is present and requires decoupling with a 0.1 µF capacitor. When using the internal reference buffer, apply a source between 0.5 V and (VDD − 0.5 V) that is buffered to the REF pin, as described in the REF pin description.
4, 5	GND	P	Power Supply Ground.
6	IN4	AI	Analog Input Channel 4.
7	IN5	AI	Analog Input Channel 5.
8	IN6	AI	Analog Input Channel 6.
9	IN7	AI	Analog Input Channel 7.
10	COM	AI	Common Channel Input. All input channels, IN[7:0], can be referenced to a commonmode point of 0 V or V_{REF}/2 V.

PIN. NO	NAME	TYPE	DESCRIPTION
11	CNV	DI	Conversion Input. On the rising edge, CNV initiates the conversion. During conversion, if CNV is held low, the busy indictor is enabled.
12	DIN	DI	Data Input. Use this input for writing to the 14-bit configuration register. The configuration register can be written to during and after conversion.
13	SCK	DI	Serial Data Clock Input. This input is used to clock out the data on SDO and clock in data on DIN in an MSB first fashion.
14	SDO	DO	Serial Data Output. The conversion result is output on this pin, synchronized to SCK. In unipolar modes, conversion results are straight binary. In bipolar modes, conversion results are twos complement.
15	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
16	IN0	AI	Analog Input Channel 0.
17	IN1	AI	Analog Input Channel 1.
18	IN2	AI	Analog Input Channel 2.
19	IN3	AI	Analog Input Channel 3.
21	EPAD	NC	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the system ground plane.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	UNIT
ANALOG INPUTS				
INx, COM		GND-0.3	VDD+0.3	V
REF, REFIN		GND-0.3	VDD+0.3	V
SUPPLY VOLTAGES				
VDD, VIO to GND		-0.3	7	V
VIO to VDD		-0.3	VDD + 0.3	V
DIN, CNV, SCK to GND		-0.3	VIO + 0.3	V
SDO to GND		-0.3	VIO + 0.3	V
Package thermal impedance (2)	QFN4X4-20		55	°C/W
Storage temperature Range		-65	+150	°C
Junction Temperature (3)			+150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The package thermal impedance is calculated in accordance with JESD-51.
(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1500	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Specifications

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, reference voltage (V_{REF}) = VDD, all specifications, T_A = -40 to +125°C, unless others noted.

PARAMETER	TEST CONDITIONS/ COMMENTS	MIN	TYP	MAX	UNIT
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	Unipolar mode	0		$+V_{REF}$	V
	Bipolar mode	$-V_{REF}/2$		$+V_{REF}/2$	V
Absolute Input Voltage	Positive input, unipolar and bipolar modes	-0.1		$V_{REF}+0.1$	V
	Negative or COM input, unipolar mode	-0.1		+0.1	V
	Negative or COM input, bipolar mode	$V_{REF}/2-0.1$	$V_{REF}/2$	$V_{REF}/2+0.1$	V
Analog Input CMRR (1)	Input frequency (f_{IN}) = 10 kHz		75		dB
Leakage Current at 25°C Input Impedance (2)	Acquisition phase		1		nA
THROUGHPUT					
Conversion Rate					
Full Bandwidth (3)	VDD = 4.5 V to 5.5 V	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	kSPS
¼ Bandwidth (3)	VDD = 4.5 V to 5.5 V	0		62.5	kSPS
	VDD = 2.3 V to 4.5 V	0		50	kSPS
Transient Response	Full-scale step, full bandwidth			1.8	µs
	Full-scale step, ¼ bandwidth			14.5	µs
ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error			±1.5		LSB (4)
Differential Linearity Error			±0.4		LSB
Transition Noise	REF = VDD = 5 V		0.6		LSB
Gain Error (5)			±5		LSB
Gain Error Match			0.5		LSB
Gain Error Temperature Drift			±0.1		ppm/°C
Offset Error (5)	VDD = 4.5 V to 5.5 V		±5		LSB
	VDD = 2.3 V to 4.5 V		±5		LSB
Offset Error Match			0.9		LSB
Offset Error Temperature Drift			0.2		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±1		LSB

Specifications(continued)

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, reference voltage (V_{REF}) = VDD, all specifications, T_A = -40 to +125°C, unless others noted.

PARAMETER	TEST CONDITIONS/ COMMENTS	MIN	TYP	MAX	UNIT
AC ACCURACY (6)					
Dynamic Range			91.5		dB (7)
Signal-to-Noise (SNR)	f_{IN} = 2kHz, V_{REF} = 5 V		90.3		dB
	f_{IN} = 2 kHz, V_{REF} = 4.096V, internal REF		89		dB
	f_{IN} = 2kHz, V_{REF} = 2.5 V, internal REF		85.2		dB
SINAD (8)	f_{IN} = 2kHz, V_{REF} = 5 V		90.1		dB
	f_{IN} = 2kHz, V_{REF} = 4.096V, internal REF		88		dB
	f_{IN} = 2kHz, V_{REF} = 2.5 V, internal REF		85		dB
Total Harmonic Distortion (THD)	f_{IN} = 2kHz		-104		dB
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 2kHz		109		dB
Channel to Channel Crosstalk	f_{IN} = 100 kHz on adjacent channel(s)		-112		dB
SAMPLING DYNAMICS					
−3 dB Input Bandwidth	Full Bandwidth		1.7		MHz
	¼ Bandwidth		0.475		MHz
Aperture Delay	VDD = 5 V		2		ns
TEMPERATURE RANGE					
Specified Performance	Minimum temperature (T_{MIN}) to T_{MAX}	-40		125	°C

(1) CMRR means common mode rejection ratio.
(2) See the Analog Inputs section.
(3) The bandwidth is set in the configuration register.
(4) With the 5 V input range, one LSB is 76.3 µV.
(5) See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.
(6) With VDD = 5 V, unless otherwise noted.
(7) All specifications expressed in decibels are referred to a full-scale input range (FSR) and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
(8) See the Terminology section.

Specifications(continued)

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, V_{REF} = VDD, all specifications, T_A = −40°C to +125°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE					
REF Output Voltage	2.5 V at 25°C	2.490	2.500	2.510	V
	4.096 V at 25°C	4.089	4.096	4.101	V
REFIN Output Voltage (1)	2.5 V at 25°C		1.13		V
	4.096 V at 25°C		2.31		V
REF Output Current			±300		µA
Temperature Drift			±15		ppm/°C
Line Regulation	VDD=5V±5%		25		ppm/V
Long-Term Drift	1000 hours		TBD		ppm
Turn-On Settling Time	Reference capacitor (C_{REF})=10µF		100		ms
EXTERNAL REFERENCE					
Voltage Range	REF input	0.5		VDD+0.3	V
	REFIN input (buffered)	1.5		VDD-0.5	V
Current Drain (2)	250 KSPS, REF = 5 V		88		µA
TEMPERATURE SENSOR					
Output Voltage (3)	25°C		267		mV
Temperature Sensitivity			0.88		mV/°C
DIGITAL INPUTS					
Logic Levels					
Input Voltage					
Low (V_{IL})		-0.3		0.3×VIO	V
High (V_{IH})		0.7×VIO		VIO+0.3	V
Input Current					
Low (I_{IL})		-1		+1	µA
High (I_{IH})		-1		+1	µA
DIGITAL OUTPUTS					
Data Format (4)					
Pipeline Delays (5)					
Output Voltage					
Low (V_{OL})	Sink current (I_{SINK})=500µA			0.4	V
High (V_{OH})	Source current (I_{SOURCE}) = -500 µA	VIO-0.3			V

Specifications(continued)

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, V_{REF} = VDD, all specifications, T_A = −40°C to +125°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
POWER SUPPLIES					
VDD (6)	Specified performance	2.3		5.5	V
VIO	Specified performance	1.8		VDD+0.3	V
Standby Current (7,8)	VDD and VIO= 5 V at 25°C		50		nA
Power Dissipation	VDD = 2.5 V, 100 SPS throughput		2.1		µW
	VDD= 2.5 V, 200 kSPS throughput		3.5		mW
	VDD= 5 V, 250 kSPS throughput		12	18	mW
	VDD = 5 V, 250 kSPS throughput with internal reference		14.6	20	mW
Energy per Conversion	VDD=5V		50		nJ
TEMPERATURE RANGE (9)					
Specified Performance	T_{MIN} to T_{MAX}	-40		125	°C

(1) This is the output from the internal band gap.
(2) This is an average current and scales with throughput.
(3) The output voltage is internal and present on a dedicated multiplexer input.
(4) Unipolar mode is serial 16-bit straight binary. Bipolar mode is serial, 16-bit twos complement.
(5) Conversion results available immediately after completed conversion.
(6) The minimum VDD supply must be 3 V when the 2.5 V internal reference is enabled, and 4.5 V when the 4.096 V internal reference is enabled. See Figure 22 for more information.
(7) With all digital inputs forced to VIO or GND as required.
(8) During acquisition phase.
(9) Contact an Analog Devices, Inc., sales representative for the extended temperature range.

7.4 Timing Specifications

VDD = 4.5 V to 5.5 V, VIO = 1.8 V to VDD, all specifications, T_A = −40°C to +125°C, unless otherwise noted. See Figure 2 and Figure 3 for load conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CONVERSION TIME					
CNV Rising Edge to Data Available	t_{CONV}			2.2	µs
ACQUISITION TIME	t_{ACQ}	1.8			µs
TIME BETWEEN CONVERSION	t_{CYC}	4			µs
DATA WRITE/READ DURING CONVERSION	t_{DATA}			1.2	µs
SCK					
Period	t_{SCK}	t_{DSDO}+2			ns
Low Time	t_{SCKL}	15			ns
High Time	t_{SCKH}	15			ns
Falling Edge to Data Remains Valid	t_{HSDO}	10			ns
Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 2.7 V				20	ns
VIO Above 2.3 V				23	ns
VIO Above 1.8 V				31	ns
CNV					
Pulse Width	t_{CNVH}	5			ns
Low to SDO DI 5 MSB Valid	t_{EN}				
VIO Above 2.7 V				13	ns
VIO Above 2.3 V				15	ns
VIO Above 1.8 V				18	ns
High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			15	ns
Low to SCK Rising Edge	t_{CLSCK}	5			ns
DIN					
Valid Setup Time from SCK Rising Edge	t_{SDIN}	5			ns
Valid Hold Time from SCK Rising Edge	t_{HDIN}	5			ns

Timing Specifications(continued)

VDD = 2.3 V to 4.5 V, VIO = 1.8 V to VDD, all specifications, T_A = −40°C to +125°C, unless otherwise noted. See Figure 2 and Figure 3 for load conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CONVERSION TIME					
CNV Rising Edge to Data Available	t_{CONV}			3.2	µs
ACQUISITION TIME	t_{ACQ}	1.8			µs
TIME BETWEEN CONVERSIONS	t_{CYC}	5			µs
DATA WRITE/READ DURING CONVERSION	t_{DATA}			1.2	µs
SCK					
Period	t_{SCK}	t_{DSDO}+2			ns
Low Time	t_{SCKL}	20			ns
High Time	t_{SCKH}	20			ns
Falling Edge to Data Remains Valid	t_{HSDO}	5			ns
Falling Edge to Data Valid Delay	t_{DSD0}				
VIO Above 3V, T_A ≤ 125°C				24	ns
VIO Above 2.7V, T_A ≤ 125°C				30	ns
VIO Above 2.3V, T_A ≤ 125°C				30	ns
VIO Above 1.8V, T_A≤125°C				36	ns
CNV					
Pulse Width	t_{CNVH}	5			ns
Low to SDO D15 MSB Valid	t_{EN}				
VIO Above 3V, T_A≤125°C				37	ns
VIO Above 2.7V, T_A≤ 125°C				43	ns
VIO Above 2.3V, T_A ≤ 125°C				52	ns
VIO Above 1.8V, T_A ≤ 125°C				60	ns
High or Last SCK Falling Edge to SDO High Impedance	t_{DIS}			50	ns
Low to SCK Rising Edge	t_{CLSCK}	5			ns
DIN					
Valid Setup Time from SCK Rising Edge	t_{SDIN}	5			ns
Valid Hold Time from SCK Rising Edge	t_{HDIN}	5			ns

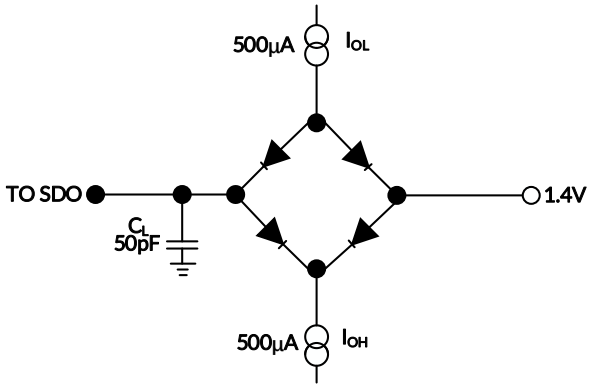
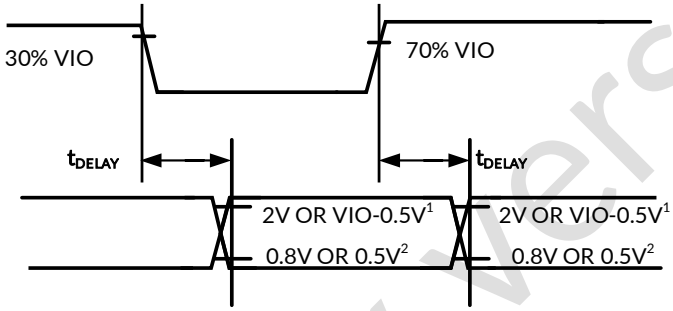


Figure 2. Load Circuit for Digital Interface Timing



2V IF VIO ABOVE 2.5V,VIO-0.5V IF VIO BELOW 2.5V.
0.8V IF VIO ABOVE 2.5V,0.5V IF VIO BELOW 2.5V.

Figure 3. Voltage Levels for Timing

7.5 Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

VDD = 2.5 V to 5.5 V, V_{REF} = 2.5 V to 5 V, VIO = 2.3 V to VDD, unless otherwise noted.

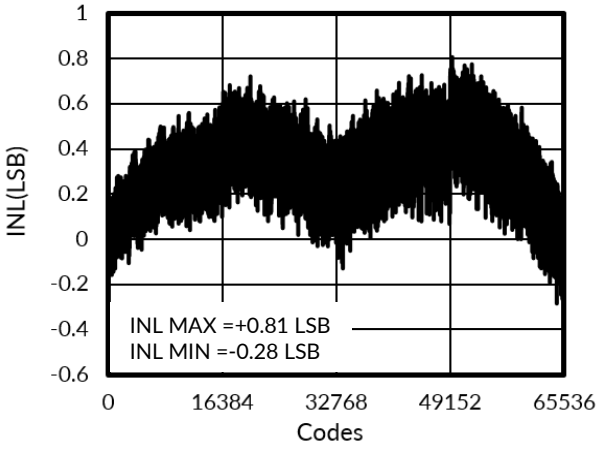


Figure 4. Integral Nonlinearity vs Code, V_{REF}=VDD=5V

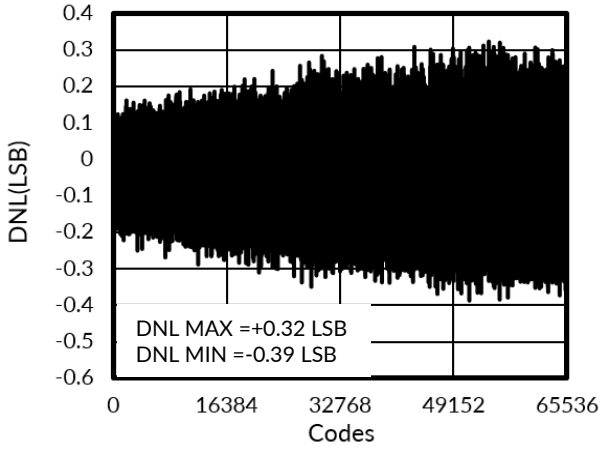


Figure 5. Differential Nonlinearity vs Code, V_{REF}=VDD=5V

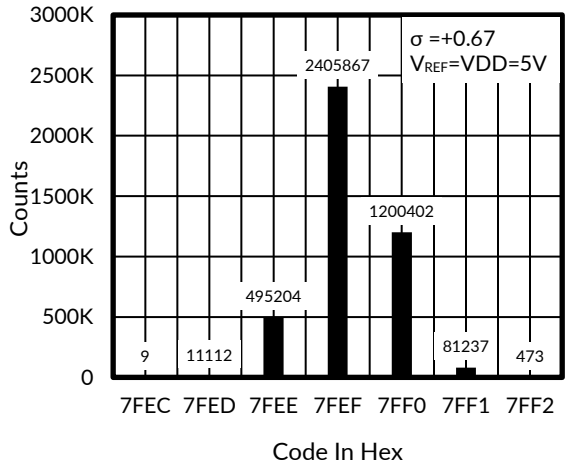


Figure 6. Histogram of a DC Input at Code Center

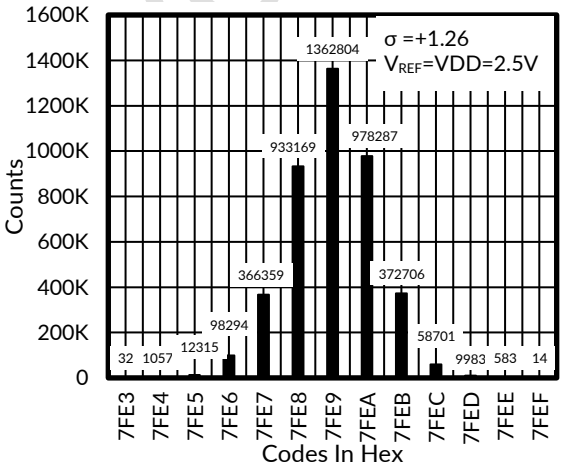


Figure 7. Histogram of a DC Input at Code Center

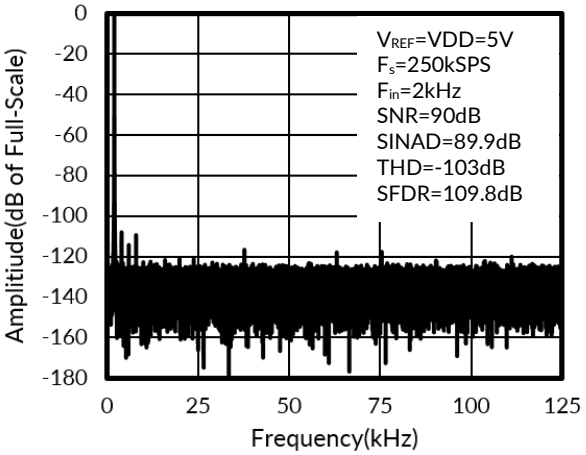


Figure 8. 2kHz Fast Fourier Transform (FFT), V_{REF} = VDD = 5 V

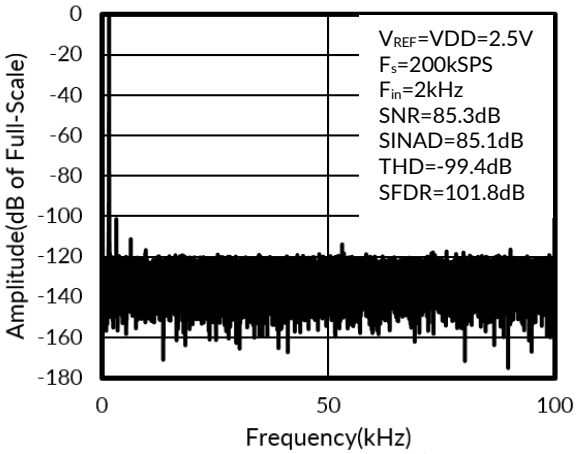


Figure 9. 2kHz FFT, V_{REF} = VDD = 2.5 V

Typical Performance Characteristics(continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

VDD = 2.5 V to 5.5 V, V_{REF} = 2.5 V to 5 V, VIO = 2.3 V to VDD, unless otherwise noted.

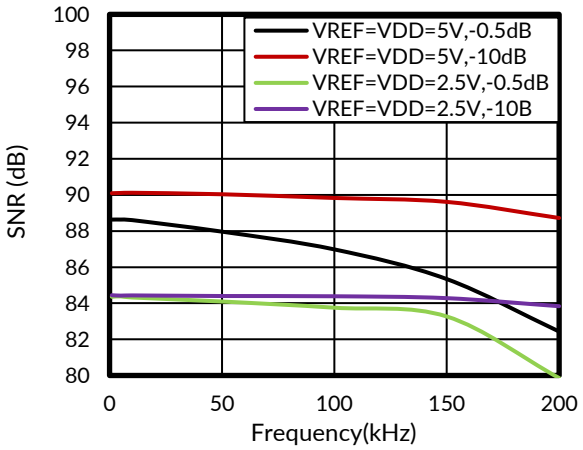


Figure 10. SNR vs Input Frequency

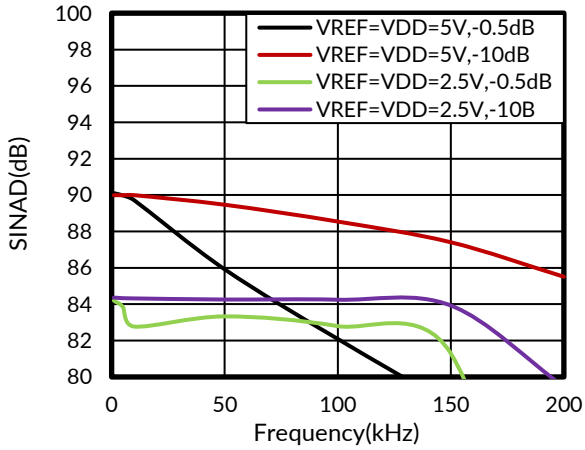


Figure 11. SINAD vs Input Frequency

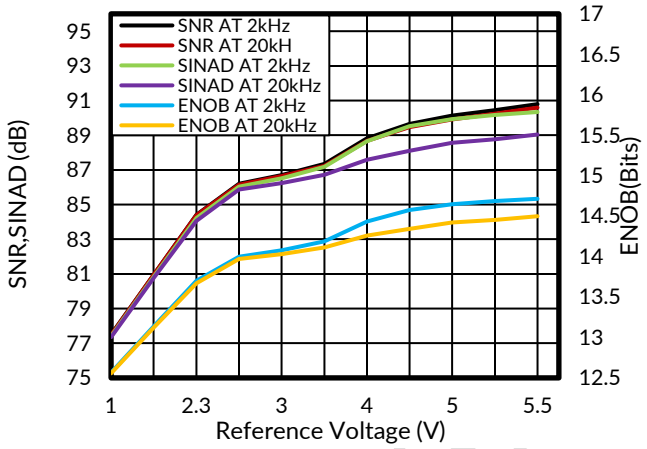


Figure 12. SNR, SINAD, and Effective Number of Bits (ENOB) vs Reference Voltage

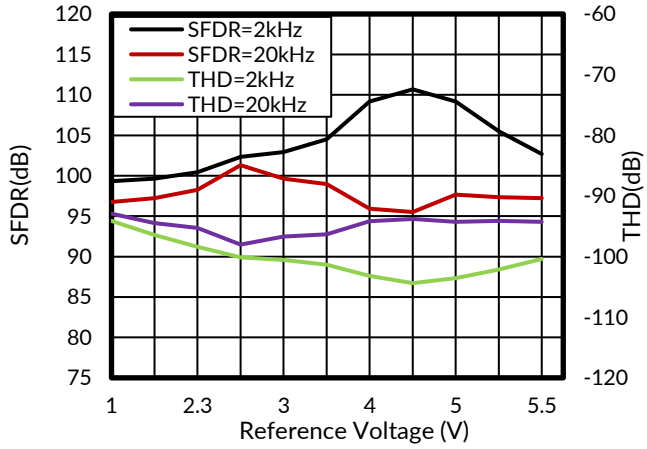


Figure 13. Spurious-Free Dynamic Range (SFDR) and THD vs Reference Voltage

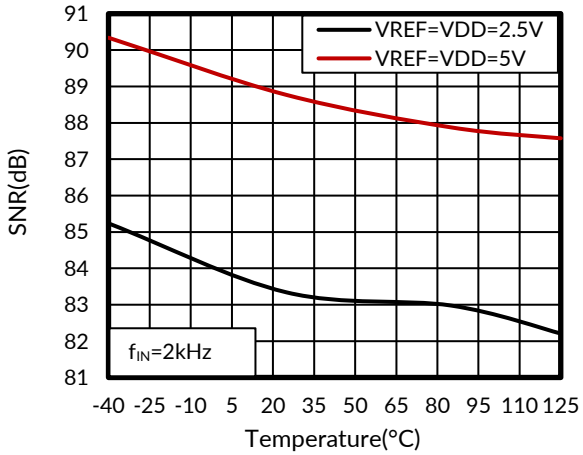


Figure 14. SNR vs Temperature

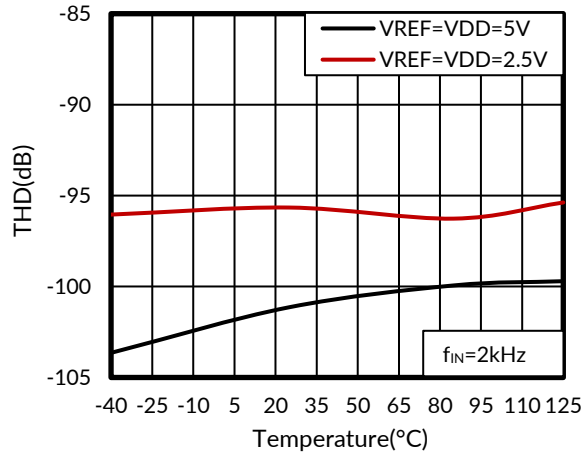


Figure 15. THD vs Temperature

Typical Performance Characteristics(continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
VDD = 2.5 V to 5.5 V, VREF = 2.5 V to 5 V, VIO = 2.3 V to VDD, unless otherwise noted.

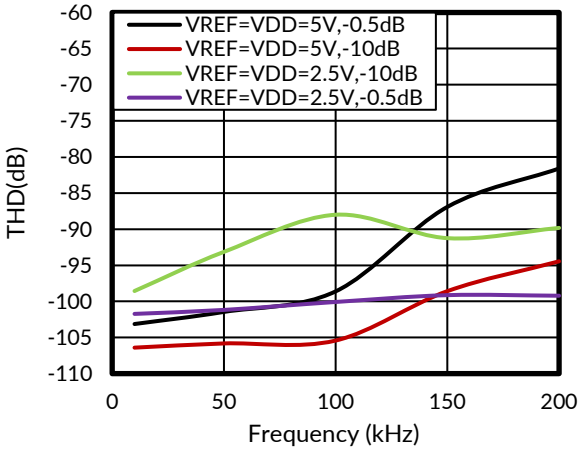


Figure 16. THD vs Frequency

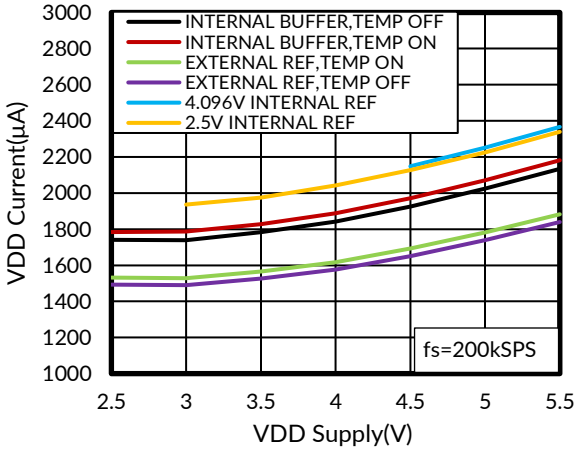


Figure 17. Operating Currents vs Supply

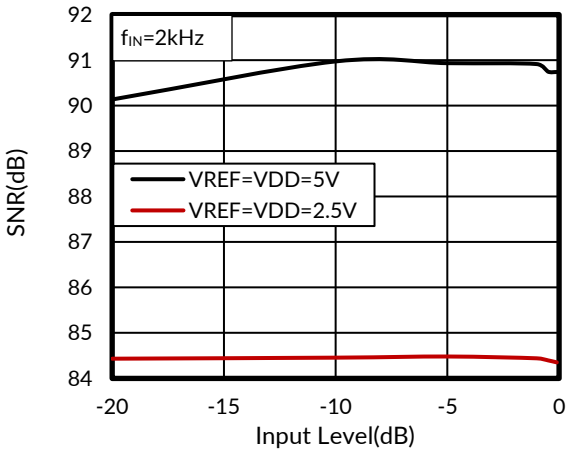


Figure 18. SNR vs Input Level

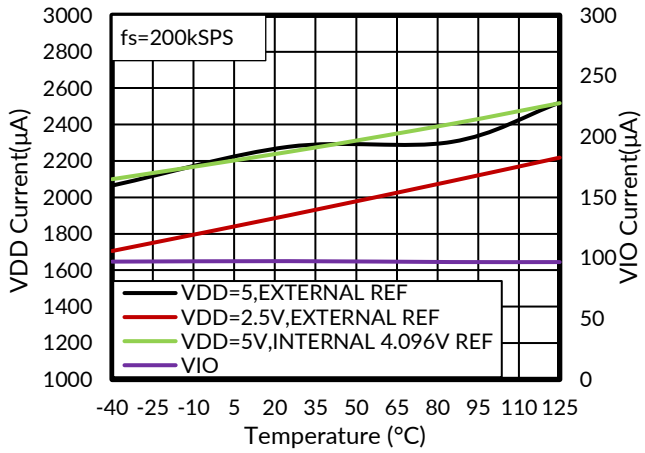


Figure 19. Operating Currents vs Temperature

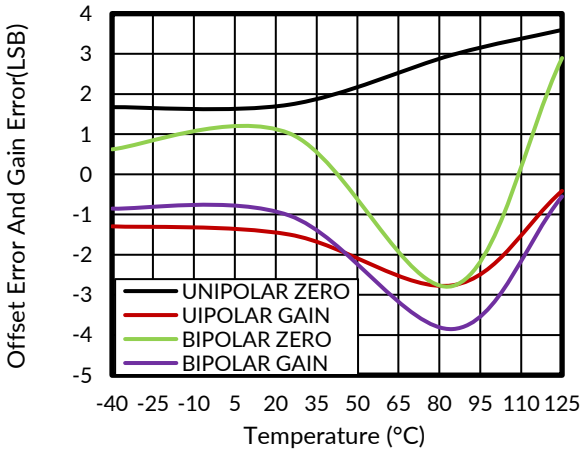


Figure 20. Offset and Gain Error vs Temperature

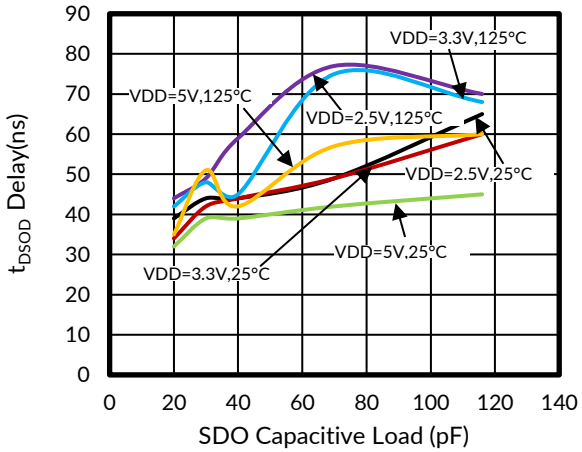


Figure 21. t_{DSDO} Delay vs SDO Capactiance Load and Supply

8 TERMINOLOGY

Least Significant Bit (LSB)
The LSB is the smallest increment represented by a converter. For an ADC with N bits of resolution, the LSB expressed in volts is

$$LSB(V) = V_{REF}/2^N$$

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 23).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error
The first transition must occur at a level ½ LSB above analog ground. The offset error is the deviation of the actual transition from that point.

Gain Error
The last transition (from 111...10 to 111...11) must occur for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation in LSB (or percentage of full-scale range) of the actual level of the last transition from the ideal level after the offset error is adjusted out. Closely related is the full-scale error (also in LSB or percentage of full-scale range), which includes the effects of the offset error.

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and the point at which the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the formula

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is a measure of the level of crosstalk between any two adjacent channels. It is measured by applying a dc to the channel under test and applying a full-scale, 100 kHz sine wave signal to the adjacent channel(s). The crosstalk is the amount of signal that leaks into the test channel, and is expressed in decibels.

Reference Voltage Temperature Coefficient

Reference voltage temperature coefficient is derived from the typical shift of output voltage at 25°C on a sample of parts at the maximum and minimum reference output voltage (V_{REF}) measured at T_{MIN}, T (25°C), and T_{MAX}. It is expressed in ppm/°C as

$$TCV_{REF}(ppm/°C) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°C) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:

V_{REF} (Max) = maximum V_{REF} at T_{MIN}, T (25°C), or T_{MAX}.
V_{REF} (Min) = minimum V_{REF} at T_{MIN}, T (25°C), or T_{MAX}.
V_{REF} (25°C) = V_{REF} at 25°C.
T_{MAX} = 125°C.
T_{MIN} = −40°C.

9 THEORY OF OPERATION

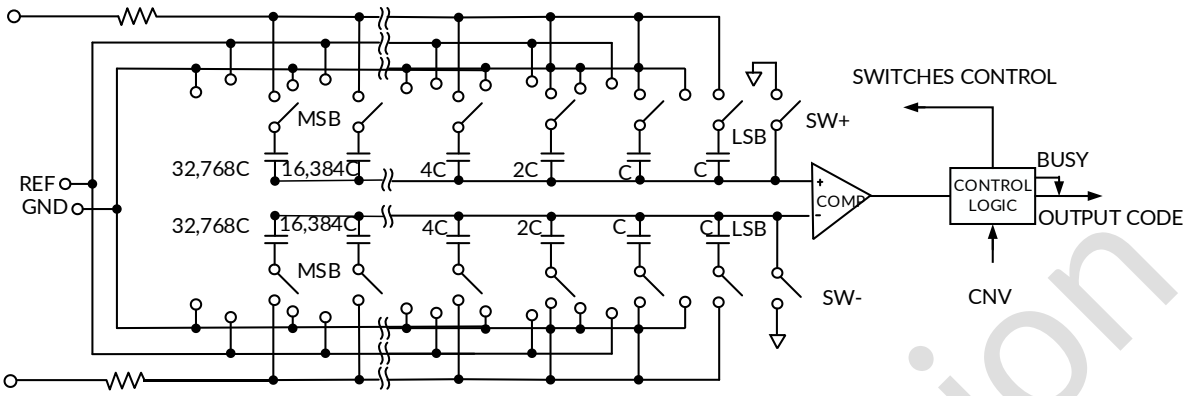


Figure 22. DC Simplified Schematic

9.1 Overview

The RS1438 is 8-channel, 16-bit, charge redistribution SAR ADC. The device is capable of converting 250,000 samples per second (250 kSPS) and power down between conversions. For example, when operating with an external reference at 1 kSPS, they consume 17 µW typically, ideal for battery-powered applications.

The RS1438 contains all of the components for use in a multichannel, low power data acquisition system, including the following:

- 16-bit SAR ADC with no missing codes
- 8-channel, low crosstalk multiplexer
- Internal low drift reference and buffer
- Temperature sensor
- Selectable one-pole filter
- Channel sequencer

These components are configured through an SPI-compatible, 14-bit register. Conversion results, also SPI compatible, can be read after or during conversions with the option for reading back the configuration associated with the conversion.

The RS1438 provides the user with an on-chip track- and-hold and do not exhibit pipeline delay or latency.

The RS1438 is specified from 2.3V to 5.5V and can be interfaced to any 1.8V to 5V digital logic family. It is housed in a 20-lead, 4 mm × 4 mm QFN4 that combines space savings and allows flexible configurations. It is pin-for-pin compatible with the 16-bit RS1438.

9.2 Converter Operation

The RS1438 is successive approximation ADCs based on a charge redistribution DAC. Figure 22 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs.

The capacitor arrays are used as sampling capacitors and acquire the analog signal on the INx+ and INx− (or COM) inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− open first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the INx+ and INx− (or COM) inputs captured at the end of the acquisition phase applies to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$…$V_{REF}/32,768$). The control

logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the device returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the RS1438 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

9.3 Transfer Functions

With the inputs configured for unipolar range (single-ended, COM with ground sense, or paired differentially with INx− as ground sense), the data output is straight binary.

With the inputs configured for bipolar range (COM = $V_{REF}/2$ or paired differentially with INx− = $V_{REF}/2$), the data outputs are twos complement.

The ideal transfer characteristic for the RS1438 is shown in Figure 23 and for both unipolar and bipolar ranges with the internal 4.096 V reference.

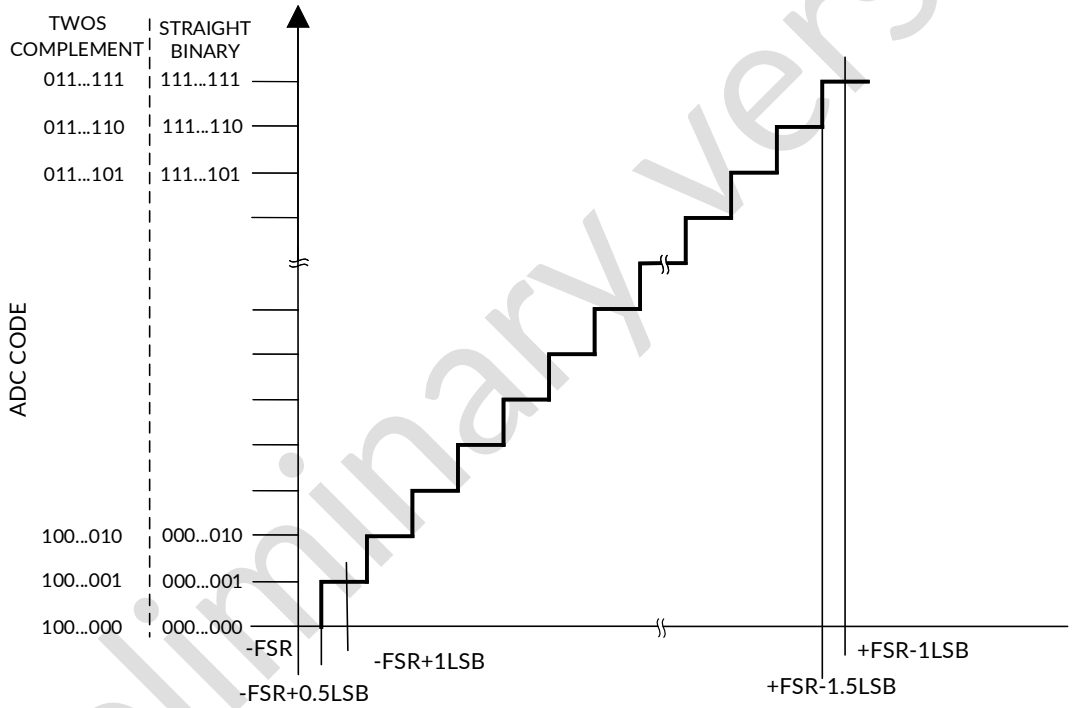


Figure 23. ADC Ideal Transfer Function

Table 1. Output Codes and Ideal Input Voltages

Description	Unipolar Analog Input (1) V_{REF} = 4.096 V	Digital Output Code (Straight Binary Hex)	Bipolar Analog Input (2) V_{REF} = 4.096 V	Digital Output Code (Twos Complement Hex)
FSR − 1 LSB	4.095938V	0xFFFF (3)	2.047938V	0x7FFF
Midscale + 1 LSB	2.048063V	0x8001	62.5µV	0x0001
Midscale	2.048V	0x8000	0V	0x0000
Midscale − 1 LSB	2.047938V	0x7FFF	-62.5µV	0xFFFF
-FSR + 1 LSB	62.5µV	0x0001	-2.047938V	0x8001
-FSR	0V	0x0000[4]	-2.048V	0x8000 (4)

(1) With COM or INx_- = 0 V or all INx referenced to GND.
(2) With COM or INx_- = $V_{REF}/2$.
(3) This is also the code for an overranged analog input ((INx_+) − (INx_-), or COM, above V_{REF} − GND).
(4) This is also the code for an underranged analog input ((INx_+) − (INx_-), or COM, below GND).

9.4 Typical Connection Diagrams

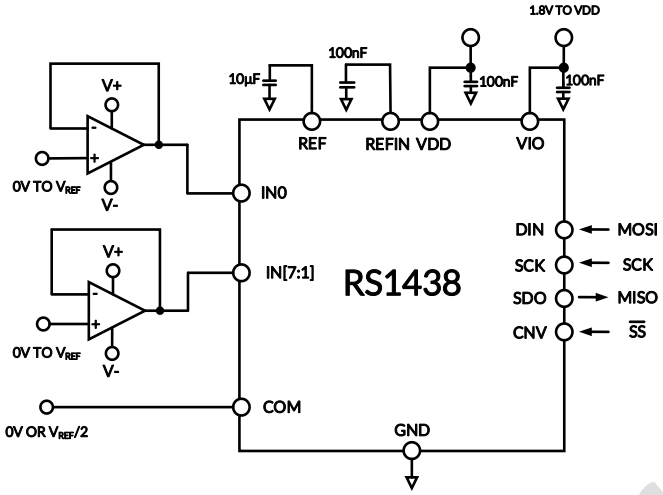


Figure 24. Typical Application Diagram with Multiple Supplies

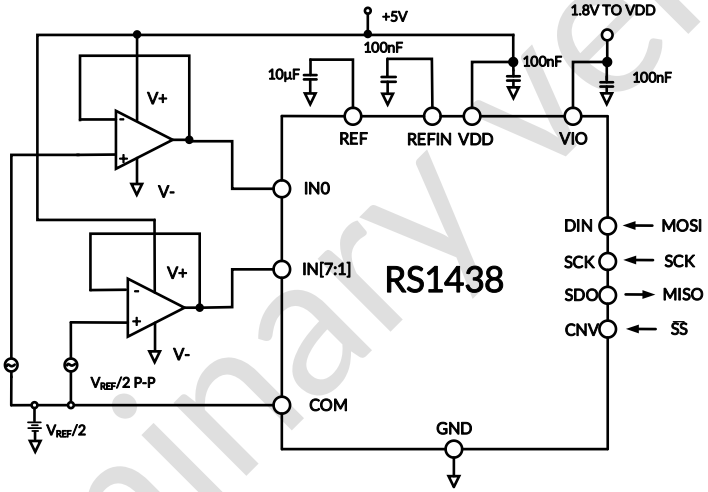


Figure 25. Typical Application Diagram Using Bipolar Input

9.4.1 Unipolar or Bipolar

Figure 24 shows an example of the recommended connection diagram for the RS1438 when multiple supplies are available.

9.4.2 Bipolar Single Supply

Figure 25 shows an example of a system with a bipolar input using single supplies with the internal reference (optional different VIO supply). This circuit is also useful when the amplifier/signal conditioning circuit is remotely located with some common mode present. Note that for any input configuration, the INx inputs are unipolar and are always referenced to GND (no negative voltages even in bipolar range). For this circuit, a rail-to-rail input/output amplifier can be used. However, take the offset voltage vs. input common-mode range into consideration (1 LSB = 62.5 µV with V_{REF} = 4.096 V). Note that the conversion results are in twos complement format when using the bipolar input configuration.

9.5 Analog Inputs

9.5.1 Input Structure

Figure 26 shows an equivalent circuit of the input structure of the RS1438. The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN[7:0] and COM. Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 0.3V because this causes the diodes to become forward biased and to start conducting current.

These diodes can handle a maximum forward-biased current of 130 mA. For instance, these conditions may eventually occur when the input buffer supplies are different from VDD. In such a case, for example, an input buffer with a short circuit, the current limitation can be used to protect the device.

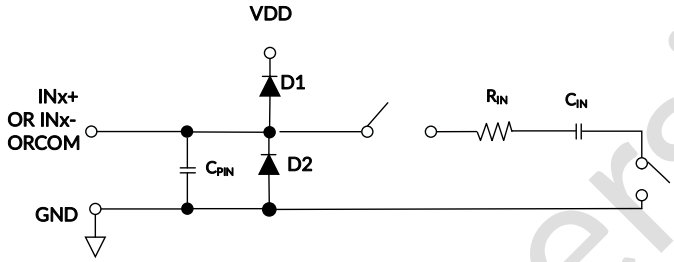


Figure 26. Equivalent Analog Input Circuit

This analog input structure allows the sampling of the true differential signal between INx+ and COM or INx+ and INx−. (COM or INx− = GND ± 0.1 V or V_{REF} ± 0.1 V). By using these differential inputs, signals common to both inputs are rejected, as shown in Figure 27.

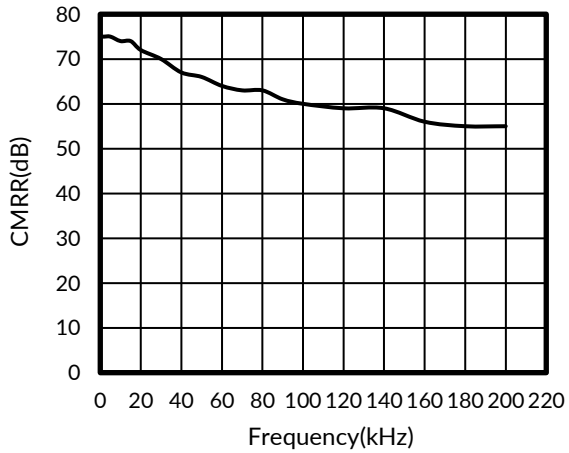


Figure 27. Analog Input CMRR vs Frequency

During the acquisition phase, the impedance of the analog inputs can be modeled as a parallel combination of the capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 2.2 kΩ and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 27 pF and is mainly the ADC sampling capacitor.

9.5.2 Selectable Low-Pass Filter

During the conversion phase, when the switches are opened, the input impedance is limited to C_{PIN}. While the RS1438 is acquiring, R_{IN} and C_{IN} make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise from the driving circuitry. The low-pass filter can be programmed for the full bandwidth or ¼ of the bandwidth with CFG[6], as shown in Table 3. This setting changes R_{IN} to 19kΩ. Note that the converter throughput must also be reduced by ¼ when using the filter. If the maximum throughput is used with the bandwidth (BW) set to ¼, the converter acquisition time, t_{ACQ}, is violated, resulting in increased THD.

9.5.3 Input Configurations

Figure 28 shows the different methods for configuring the analog inputs with the configuration register, CFG[12:10]. Refer to the Configuration Register, CFG section for more details. The analog inputs can be configured as shown in the following figures:

- Figure 28 (A), single-ended referenced to system ground, CFG[12:10] = 111_2. In this configuration, all inputs (IN[7:0]) have a range of GND to V_{REF}.

- Figure 28 (B), bipolar differential with a common reference point, COM = $V_{REF}/2$, CFG[12:10] = 010_2. Unipolar differential with COM connected to a ground sense; CFG[12:10] = 110_2. In this configuration, all inputs IN[7:0] have a range of GND to V_{REF}.

- Figure 28 (C), bipolar differential pairs with the negative input channel referenced to $V_{REF}/2$, CFG[12:10] = $00X_2$. Unipolar differential pairs with the negative input channel referenced to a ground sense, CFG[12:10] = $10X_2$. In these configurations, the positive input channels have the range of GND to V_{REF}. The negative input channels are a sense referred to $V_{REF}/2$ for bipolar pairs, or GND for unipolar pairs. The positive channel is configured with CFG[9:7]. If CFG[9:7] is even, then IN0, IN2, IN4, and IN6 are used. If CFG[9:7] is odd, then IN1, IN3, IN5, and IN7 are used, as indicated by the channels with parentheses in Figure 28 (C). For example, for IN0/IN1 pairs with the positive channel on IN0, CFG[9:7] = 000_2. For IN4/IN5 pairs with the positive channel on IN5, CFG[9:7] = 101_2. Note that for the sequencer, detailed in the Channel Sequencer section, the positive channels are always IN0, IN2, IN4, and IN6.

- Figure 28 (D), inputs configured in any of the preceding combinations (showing that the RS1438 can be configured dynamically)

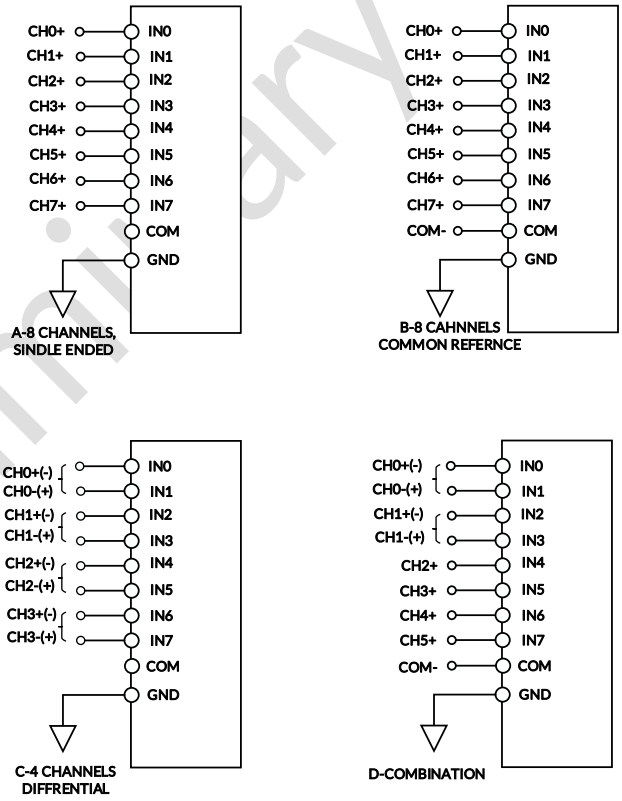


Figure 28. Multiplexed Analog Input Configurations

9.5.4 Sequencer

The RS1438 includes a channel sequencer useful for scanning channels in a repeated fashion. Refer to the Channel Sequencer section for further details on the sequencer operation.

9.5.5 Source Resistance

When the source impedance of the driving circuit is low, the RS1438 can be driven directly. Large source impedances significantly affect the ac performance, especially THD. The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

9.6 Driver Amplifier Choice

Although the RS1438 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the RS1438. Note that the RS1438 has a noise much lower than most other 16-bit ADCs and, therefore, can be driven by a noisier amplifier to meet a given system noise specification. The noise from the amplifier is filtered by the RS1438 analog input circuit low-pass filter made by R_{IN} and C_{IN}, or by an external filter, if one is used. Because the typical noise of the RS1438 is 35 µV rms (with V_{REF} = 5 V), the SNR degradation due to the amplifier is

$$SNR_{LOSS}=20(\log\frac{35}{\sqrt{35^2+\frac{\pi}{2}f_{-3dB}(Ne_N)^2}})$$

  where:
  f_{-3dB} is the input bandwidth in megahertz of the RS1438 (1.7 MHz in full BW or 425 kHz in ¼ BW), or the cut off frequency of an input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_N is the equivalent input noise voltage of the op amp, in nV/√Hz.

- For ac applications, the driver must have a THD performance commensurate with the RS1438. Figure 16 shows THD vs frequency for the RS1438.

- For multichannel, multiplexed applications on each input or input pair, the driver amplifier and the RS1438 analog input circuit must settle a full-scale step onto the capacitor array at a 16-bit level (0.0015%). In amplifier data sheets, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at a 16-bit level and must be verified prior to driver selection.

9.7 Voltage Reference Output/Input

The RS1438 allows the choice of a very low temperature drift internal voltage reference, an external reference, or an external buffered reference.

The internal reference of the RS1438 provide excellent performance and can be used in almost all applications. There are six possible choices of voltage reference schemes, briefly described in Table 3, with more details in each of the following sections.

9.7.1 Internal Reference/Temperature Sensor

The precision internal reference, suitable for most applications, can be set for either a 2.5V or a 4.096 V output, as detailed in Table 3. With the internal reference enabled, the band gap voltage is also present on the REFIN pin, which requires an external 0.1 µF capacitor.

Enabling the reference also enables the internal temperature sensor, which measures the internal temperature of the RS1438, and is therefore useful for performing a system calibration. For applications requiring the use of the temperature sensor, the internal reference must be active (internal buffer can be disabled in this case). Note that, when using the temperature sensor, the output is straight binary referenced from the RS1438 GND pin.

The internal reference is temperature compensated to within 10 mV. The reference is trimmed to provide a typical drift of ±10 ppm/°C. Connect the RS1438 as shown in Figure 29 for either a 2.5 V or 4.096 V internal reference.

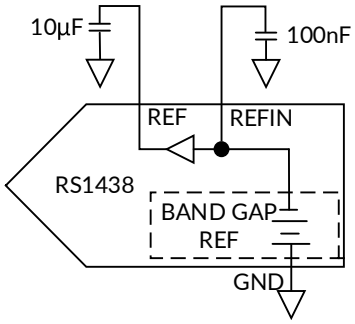


Figure 29. 2.5 V or 4.096 V Internal Reference Connection

9.7.2 External Reference and Internal Buffer

For improved drift performance, an external reference can be used with the internal buffer, as shown in Figure 30. The external source is connected to REFIN, the input to the on-chip unity-gain buffer, and the output is produced on the REF pin. An external reference can be used with the internal buffer with or without the temperature sensor enabled. Refer to Table 3 for register details. With the buffer enabled, the gain is unity and is limited to an input/output of VDD = −0.2 V. However, the maximum voltage allowable must be ≤VDD − 0.5 V.

The internal reference buffer is useful in multiconverter applications because a buffer is typically required in these applications. In addition, a low power reference can be used because the internal buffer provides the necessary performance to drive the SAR architecture of the RS1438

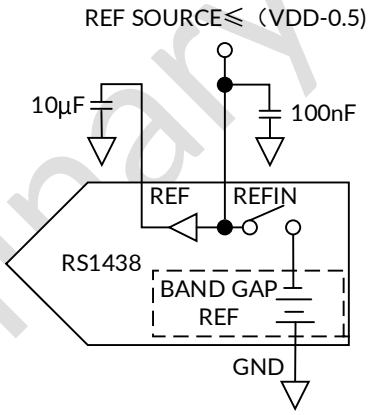


Figure 30. External Reference Using Internal Buffer

9.7.3 External Reference

In any of the six voltage reference schemes, an external reference can be connected directly on the REF pin as shown in Figure 31 because the output impedance of REF is >5 kΩ. To reduce power consumption, power down the reference and buffer. Refer to Table 3 for register details.

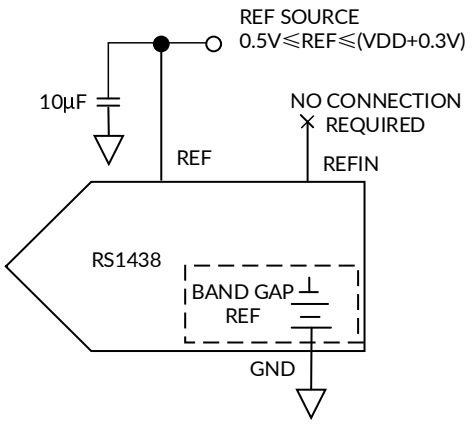


Figure 31. Extend Reference

Note that the best SNR is achieved with a 5 V external reference as the internal reference is limited to 4.096 V. The SNR degradation is as follows:

$$SNR_{LOSS}=20\log\frac{4.096}{5}$$

9.7.4 Reference Decoupling

Whether using an internal or external reference, the RS1438 voltage reference output/input, REF, has a dynamic input impedance and must be driven by a low impedance source with efficient decoupling between the REF and GND pins. This decoupling depends on the choice of the voltage reference but usually consists of a low ESR capacitor connected to REF and GND with minimum parasitic inductance.

The placement of the reference decoupling capacitor is also important to the performance of the RS1438, as explained in the Layout section. Mount the decoupling capacitor with a thick PCB trace on the same side as the ADC at the REF pin. The GND must also connect to the reference decoupling capacitor with the shortest distance and to the analog ground plane with several vias. If desired, smaller reference decoupling capacitor values down to 2.2 µF can be used with a minimal impact on performance, especially on DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

For applications that use multiple RS1438 devices or other PulSAR devices, it is more effective to use the internal reference buffer to buffer the external reference voltage, thus reducing SAR conversion crosstalk.

The voltage reference temperature coefficient directly impacts full scale; therefore, in applications where full-scale accuracy matters, care must be taken with the temperature coefficient. For instance, a ±10 ppm/°C temperature coefficient of the reference changes full scale by ±1 LSB/°C

9.8 Power Supply

The RS1438 use two power supply pins: an analog and digital core supply (VDD), and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between 1.8 V and VDD. To reduce the supplies needed, the VIO and VDD pins can be tied together. The RS1438 are independent of power supply sequencing between VIO and VDD. Additionally, they are very insensitive to power supply variations over a wide frequency range, as shown in Figure 32.

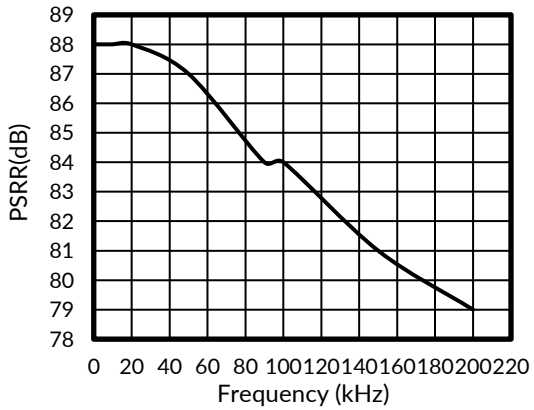


Figure 32. Power Supply Rejection Ratio (PSRR) vs Frequency

The RS1438 powers down automatically at the end of each conversion phase. Therefore, the operating currents and power scale linearly with the sampling rate. This makes the device ideal for low sampling rates (even of a few hertz), and low battery-powered applications.

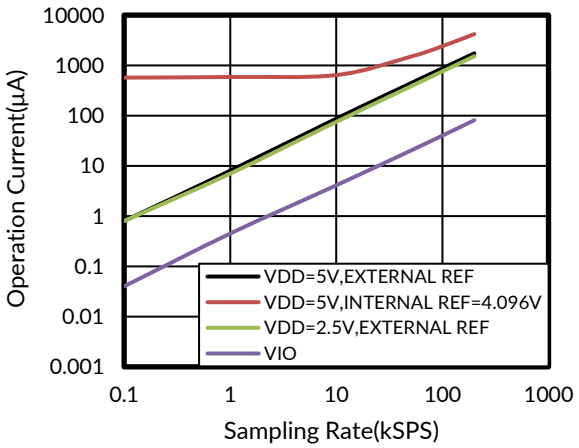


Figure 33. Operating Currents vs Sampling Rate

9.9 Supplying The ADC from The Reference

For simplified applications, the RS1438, with their low operating current, can be supplied directly using an external reference circuit like the one shown in Figure 34. The reference line can be driven by the following:

- The system power supply directly.
- A reference voltage with enough current output capability.
- A reference buffer.

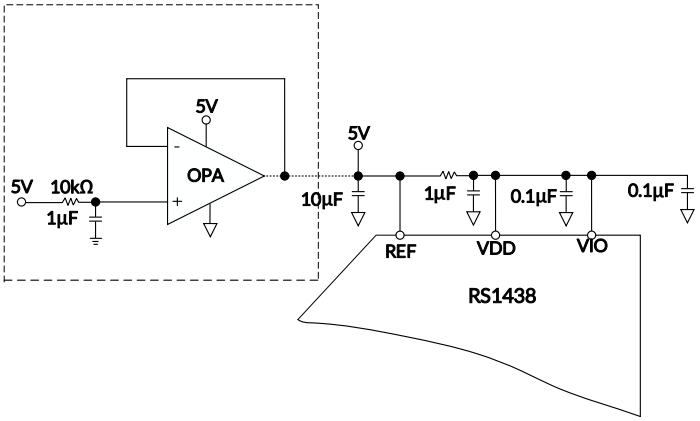


Figure 34. Example of an Application Circuit

10 DIGITAL INTERFACE

The RS1438 use a simple 4-wire interface and are compatible with SPI, MICROWIRE™, QSPI™, digital hosts, and DSPs .

The interface uses the CNV, DIN, SCK, and SDO signals and allows CNV, which initiates the conversion, to be independent of the readback timing. This is useful in low jitter sampling or simultaneous sampling applications.

A 14-bit register, CFG[13:0], is used to configure the ADC for the channel to be converted, the reference selection, and other components, which are detailed in the Configuration Register, CFG section.

When CNV is low, reading/writing can occur during conversion, acquisition, and spanning conversion (acquisition plus conversion). The CFG word is updated on the first 14 SCK rising edges, and conversion results are output on the first 15 (or 16, if busy mode is selected) SCK falling edges. If the CFG readback is enabled, an additional 14 SCK falling edges are required to output the CFG word associated with the conversion results with the CFG MSB following the LSB of the conversion result.

A discontinuous SCK is recommended because the device is selected with CNV low, and SCK activity begins to write a new configuration word and clock out data.

The timing diagrams indicate digital activity (SCK, CNV, DIN, and SDO) during the conversion. However, due to the possibility of performance degradation, digital activity occurs only prior to the safe data reading/writing time, t_{DATA}, because the RS1438 provide error correction circuitry that can correct for an incorrect bit during this time. From t_{DATA} to t_{CONV}, there is no error correction, and conversion results may be corrupted. Configure the RS1438 and initiate the busy indicator (if desired) prior to t_{DATA}. It is also possible to corrupt the sample by having SCK or DIN transitions near the sampling instant. Therefore, it is recommended to keep the digital pins quiet for approximately 20 ns before and 10 ns after the rising edge of CNV, using a discontinuous SCK whenever possible to avoid any potential performance degradation.

10.1 Reading/Writing During Conversion, Fast Hosts

When reading/writing during conversion (n), conversion results are for the previous (n − 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion. After the CNV is brought high to initiate conversion, it must be brought low again to allow reading/writing during conversion. Reading/writing must only occur up to t_{DATA} and, because this time is limited, the host must use a fast SCK. The SCK frequency required is calculated by

$$f_{SCK} \geq \frac{\text{Number\_SCK\_Edges}}{t_{DATA}}$$

The time between t_{DATA} and t_{CONV} is a safe time when digital activity must not occur, or sensitive bit decisions may be corrupt.

10.2 Reading/Writing After Conversion, Any Speed Hosts

When reading/writing after conversion, or during acquisition (n), conversion results are for the previous (n − 1) conversion, and writing is for the (n + 1) acquisition.

For the maximum throughput, the only time restriction is that the reading/writing take place during the t_{ACQ} (minimum) time. For slow throughputs, the time restriction is dictated by the throughput required by the user, and the host is free to run at any speed. Thus for slow hosts, data access must take place during the acquisition phase.

10.3 Reading/Writing Spanning Conversion, Any Speed Host

When reading/writing spanning conversion, the data access starts at the current acquisition (n) and spans into the conversion (n). Conversion results are for the previous (n − 1) conversion, and writing the CFG register is for the next (n + 1) acquisition and conversion.

Similar to reading/writing during conversion, reading/writing must only occur up to t_{DATA}. For the maximum throughput, the only time restriction is that reading/writing take place during the t_{ACQ} + t_{DATA} time.

For slow throughputs, the time restriction is dictated by the required throughput, and the host is free to run at any speed. Similar to reading/writing during acquisition, for slow hosts, the data access must take place during the acquisition phase with additional time into the conversion.

Data access spanning conversion requires the CNV to be driven high to initiate a new conversion, and data access is not allowed when CNV is high. Therefore, the host must perform two bursts of data access when using this method.

10.4 Configuration Register, CFG

The RS1438 use a 14-bit configuration register (CFG[13:0]), as detailed in Table 3, to configure the inputs, the channel to be converted, the one-pole filter bandwidth, the reference, and the channel sequencer. The CFG register is latched (MSB first) on DIN with 14 SCK rising edges. The CFG update is edge dependent, allowing for asynchronous or synchronous hosts.

The register can be written to during conversion, during acquisition, or spanning acquisition/conversion, and is updated at the end of conversion, t_{CONV} (maximum). There is always a one deep delay when writing the CFG register.

At power-up, the CFG register is undefined and two dummy conversions are required to update the register. To preload the CFG register with a factory setting, hold DIN high for two conversions (CFG[13:0] = 0x3FFF). This sets the RS1438 for the following:

- IN[7:0] unipolar referenced to GND, sequenced in order.
- Full bandwidth for a one-pole filter.
- Internal reference/temperature sensor disabled, buffer enabled.
- Enables the internal sequencer.
- No readback of the CFG register.

Table 3 summarizes the configuration register bit details. See the Theory of Operation section for more details.

Table 2. Configuration Register Bit Names

13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFG	INCC	INCC	INCC	INx	INx	INx	BW	REF	RED	REF	SEQ	SEQ	RB

Table 3. Configuration Register Description

<table>
<tr><th>Bits</th><th>Name</th><th colspan="4">Description</th></tr>
<tr><td>[13]</td><td>CFG</td><td colspan="4">Configuration update.
0 = keep current configuration settings.
1 = overwrite contents of register.</td></tr>
<tr><td rowspan="8">[12:10]</td><td rowspan="8">INCC</td><td colspan="4">Input channel configuration. Selection of pseudo bipolar, pseudo differential, pairs, single-ended, or temperature sensor. Refer to the Input Configurations section.</td></tr>
<tr><td>Bit 12</td><td>Bit 11</td><td>Bit 10</td><td>Function</td></tr>
<tr><td>0</td><td>0</td><td>X</td><td>Bipolar differential pairs; INx− referenced to VREF/2 ± 0.1 V.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bipolar; INx referenced to COM = VREF/2 ± 0.1 V.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Temperature sensor.</td></tr>
<tr><td>1</td><td>0</td><td>X</td><td>Unipolar differential pairs; INx− referenced to GND ± 0.1 V.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Unipolar, INx referenced to COM = GND ± 0.1 V.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Unipolar, INx referenced to GND.</td></tr>
<tr><td rowspan="4">[9:7]</td><td rowspan="4">INx</td><td colspan="4">Input channel selection in binary fashion</td></tr>
<tr><td>Bit 9</td><td>Bit8</td><td>Bit 7</td><td>Channel</td></tr>
<tr><td>0
0
...
1</td><td>0
0
...
1</td><td>0
1
...
1</td><td>IN0
IN1
...
IN7</td></tr>
<tr><td>[6]</td><td>BW</td><td colspan="4">Select bandwidth for low-pass filter. Refer to the Selectable Low-Pass Filter section.
0= ¼ of BW, uses an additional series resistor to further bandwidth limit the noise. Maximum throughput must be reduced to ¼.
1 = full BW.</td></tr>
<tr><td rowspan="11">[5:3]</td><td rowspan="11">REF</td><td colspan="4">Reference/buffer selection. Selection of internal, external, external buffered, and enabling of the on-chip temperature sensor. Refer to the Voltage Reference Output/Input section.</td></tr>
<tr><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Function</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal reference and temperature sensor enabled. REF = 2.5 V buffered output.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Internal reference and temperature sensor enabled. REF = 4.096 V buffered output.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Use external reference. Temperature sensor enabled. Internal buffer disabled.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Use external reference. Internal buffer and temperature sensor enabled.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Do not use.</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Do not use.</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Use external reference. Internal reference, internal buffer, and temperature sensor disabled.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Use external reference. Internal buffer enabled. Internal reference and temperature sensor disabled.</td></tr>
<tr><td rowspan="6">[2:1]</td><td rowspan="6">SEQ</td><td colspan="4">Channel sequencer. Allows for scanning channels in an IN0 to IN[7:0] fashion. Refer to the Channel Sequencer section</td></tr>
<tr><td>Bit 2</td><td>Bit 1</td><td colspan="2">Function</td></tr>
<tr><td>0
0
1
1</td><td>0
1
0
1</td><td colspan="2">Disable sequencer.
Update configuration during sequence.
Scan IN0 to IN[7:0] (set in CFG[9:7]), then temperature.
Scan IN0 to IN[7:0] (set in CFG[9:7]).</td></tr>
<tr><td>[0]</td><td>RB</td><td colspan="4">Read back the CFG register.
0 = read back current configuration at end of data.
1 = do not read back contents of configuration</td></tr>
</table>

10.5 General Timing Without A Busy Indicator

Figure 35 details the timing for all three modes: read/write during conversion (RDC), read/write after conversion (RAC), and read/write spanning conversion (RSC). Note that the gating item for both CFG and data readback is at the end of conversion (EOC). At EOC, if CNV is high, the busy indicator is disabled.

As detailed in the Digital Interface section, the data access must occur up to safe data reading/writing time, t_{DATA}. If the full CFG word is not written to prior to EOC, it is discarded and the current configuration remains. If the conversion result is not read out fully prior to EOC, it is lost as the ADC updates SDO with the MSB of the current conversion. For detailed timing, refer to Figure 38 and Figure 39, which depict reading/writing spanning conversion with all timing details, including setup, hold, and SCK.

When CNV is brought low after EOC, SDO is driven from high impedance to the MSB. Falling SCK edges clock out bits starting with MSB − 1.

The SCK can idle high or low depending on the clock polarity (CPOL) and clock phase (CPHA) settings if SPI is used. A simple solution is to use CPOL = CPHA = 0 as shown in Figure 35 with SCK idling low.

From power-up, in any read/write mode, the first three conversion results are undefined because a valid CFG does not take place until the second EOC; therefore, two dummy conversions are required. If the state machine writes the CFG during the power-up state (RDC shown), the CFG register must be rewritten at the next phase. The first valid data occurs in phase (n + 1) when the CFG register is written during phase (n − 1).

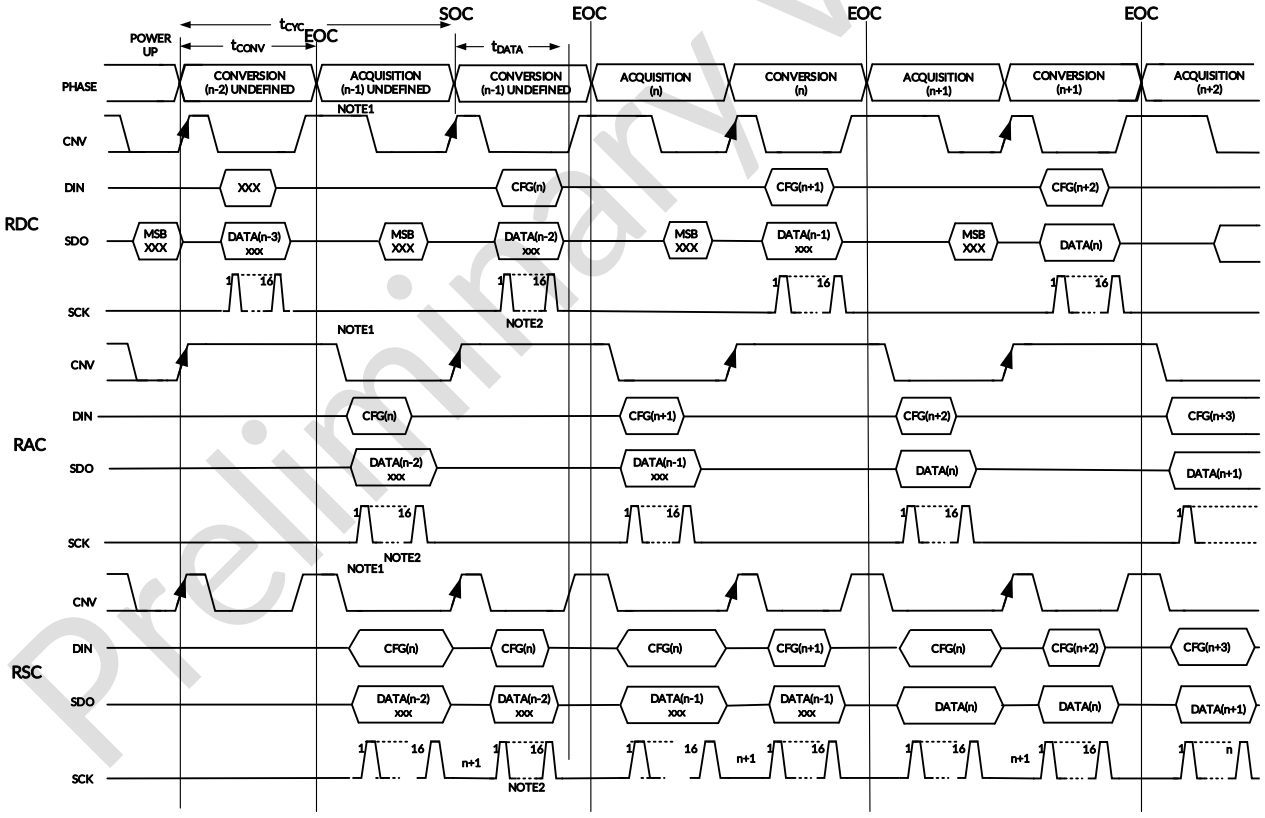


Figure 35. General Interface Timing for the RS1438 Without a Busy Indicato

NOTES
1. CNV MUST BE HIGH PRIOR TO THE END OF CONVERSION (EOC) TO AVOID THE BUSY INDICATOR.
2. A TOTAL OF 16 SCK FALLING EDGES ARE REQUIRED TO RETURN SDO TO HIGH-Z. IF CFG READBACK IS ENABLED, A TOTAL OF 30 SCK FALLING EDGES IS REQUIRED TO RETURN SDO TO HIGH-Z.

10.6 General Timing With A Busy Indicator

Figure 36 details the timing for all three modes: RDC, RAC, and RSC. Note that the gating item for both CFG and data readback is at EOC. The data access must occur up to safe data reading/writing time, t_{DATA}. If the full CFG word is not written to prior to EOC, it is discarded and the current configuration remains.

At the EOC, if CNV is low, the busy indicator enables. In addition, to generate the busy indicator properly, the host must assert a minimum of 17 SCK falling edges to return SDO to high impedance because the last bit on SDO remains active. Unlike the case detailed in the Read/Write Spanning Conversion Without a Busy Indicator section, if the conversion result is not read out fully prior to EOC, the last bit clocked out remains. If this bit is low, the busy signal indicator cannot be generated because the busy generation requires either a high impedance or a remaining bit high-to-low transition. A good example of this occurs when an SPI host sends 16 SCKs because these are usually limited to 8-bit or 16-bit bursts. Therefore, the LSB remains. Because the transition noise of the RS1438 is 4 LSBs peak-to-peak (or greater), the LSB is low 50% of the time. For this interface, the SPI host needs to burst 24 SCKs, or a QSPI interface can be used and programmed for 17 SCKs. The SCK can idle high or low depending on the CPOL and CPHA settings if SPI is used. A simple solution is to use CPOL = CPHA = 1 (not shown) with SCK idling high.

From power-up, in any read/write mode, the first three conversion results are undefined because a valid CFG does not take place until the second EOC. Thus, two dummy conversions are required. Also, if the state machine writes the CFG during the power-up state (RDC shown), the CFG register needs to be rewritten again at the next phase. The first valid data occurs in phase (n + 1) when the CFG register is written during phase (n − 1).

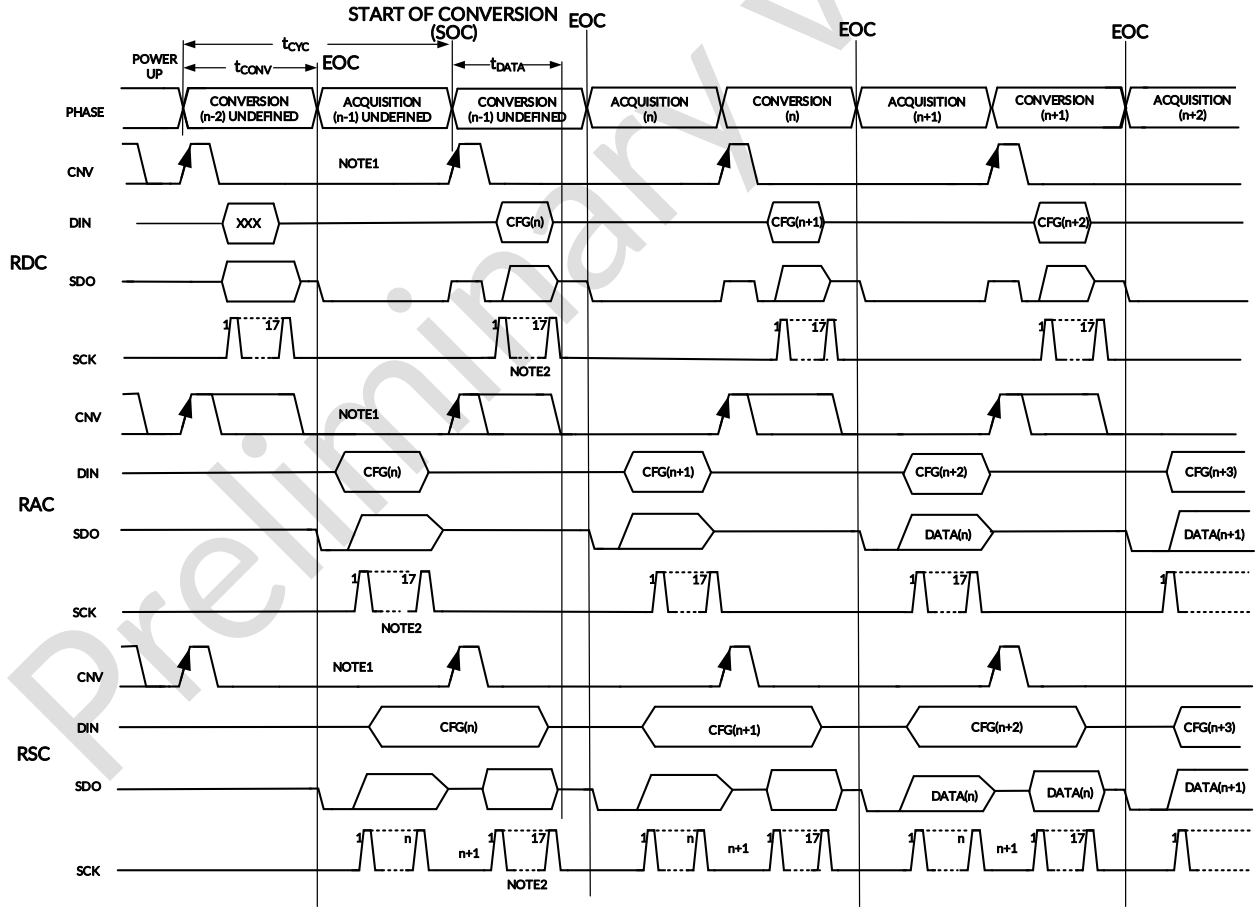


Figure 36. General Interface Timing for the RS1438 With a Busy Indicator

NOTES
1. CNV MUST BE LOW PRIOR TO THE END OF CONVERSION (EOC) TO GENERATE THE BUSY INDICATOR.
2. A TOTAL OF 17 SCK FALLING EDGES ARE REQUIRED TO RETURN SDO TO HIGH-Z. IF CFG READBACK IS ENABLED, A TOTAL OF 31 SCK FALLING EDGES IS REQUIRED TO RETURN SDO TO HIGH-Z.

10.7 Channel Sequencer

The RS1438 includes a channel sequencer useful for scanning channels in a repeated fashion. Channels are scanned as singles or pairs, with or without the temperature sensor, after the last channel is sequenced.

The sequencer starts with IN0 and finishes with IN[7:0] set in CFG[9:7]. For paired channels, the channels are paired depending on the last channel set in CFG[9:7]. Note that in sequencer mode, the channels are always paired with the positive input on the even channels (IN0, IN2, IN4, and IN6), and with the negative input on the odd channels (IN1, IN3, IN5, and IN7). For example, setting CFG[9:7] = 110 or 111 scans all pairs with the positive inputs dedicated to IN0, IN2, IN4, and IN6.

CFG[2:1] are used to enable the sequencer. After the CFG register is updated, DIN must be held low while reading data out for Bit 13, or the CFG register begins updating again.

Note that while operating in a sequence, some bits of the CFG register can be changed. However, if changing CFG[11] (paired or single channel) or CFG[9:7] (last channel in sequence), the sequence reinitializes and converts IN0 (or IN0/IN1 pairs) after the CFG register is updated.

Figure 37 details the timing for all three modes without a busy indicator. Refer to the Read/Write Spanning Conversion Without a Busy Indicator section and the Read/Write Spanning Conversion Without a Busy Indicator section for more details. The sequencer can also be used with the busy indicator and details for these timings can be found in the General Timing with a Busy Indicator section and the Read/Write Spanning Conversion with a Busy Indicator section.

For sequencer operation, the CFG register must be set during the (n − 1) phase after power-up. On phase (n), the sequencer setting takes place and acquires IN0. The first valid conversion result is available at phase (n + 1). After the last channel set in CFG[9:7] is converted, the internal temperature sensor data is output (if enabled), followed by acquisition of IN0.

10.7.1 Examples

With all channels configured for unipolar mode to GND, including the internal temperature sensor, the sequence scans in the following order:

IN0, IN1, IN2, IN3, IN4, IN5, IN6, IN7, TEMP, IN0, IN1, IN2…

For paired channels with the internal temperature sensor enabled, the sequencer scans in the following order:

IN0, IN2, IN4, IN6, TEMP, IN0…

Note that IN1, IN3, IN5, and IN7 are referenced to a GND sense or $V_{REF}/2$, as detailed in the Input Configurations section.

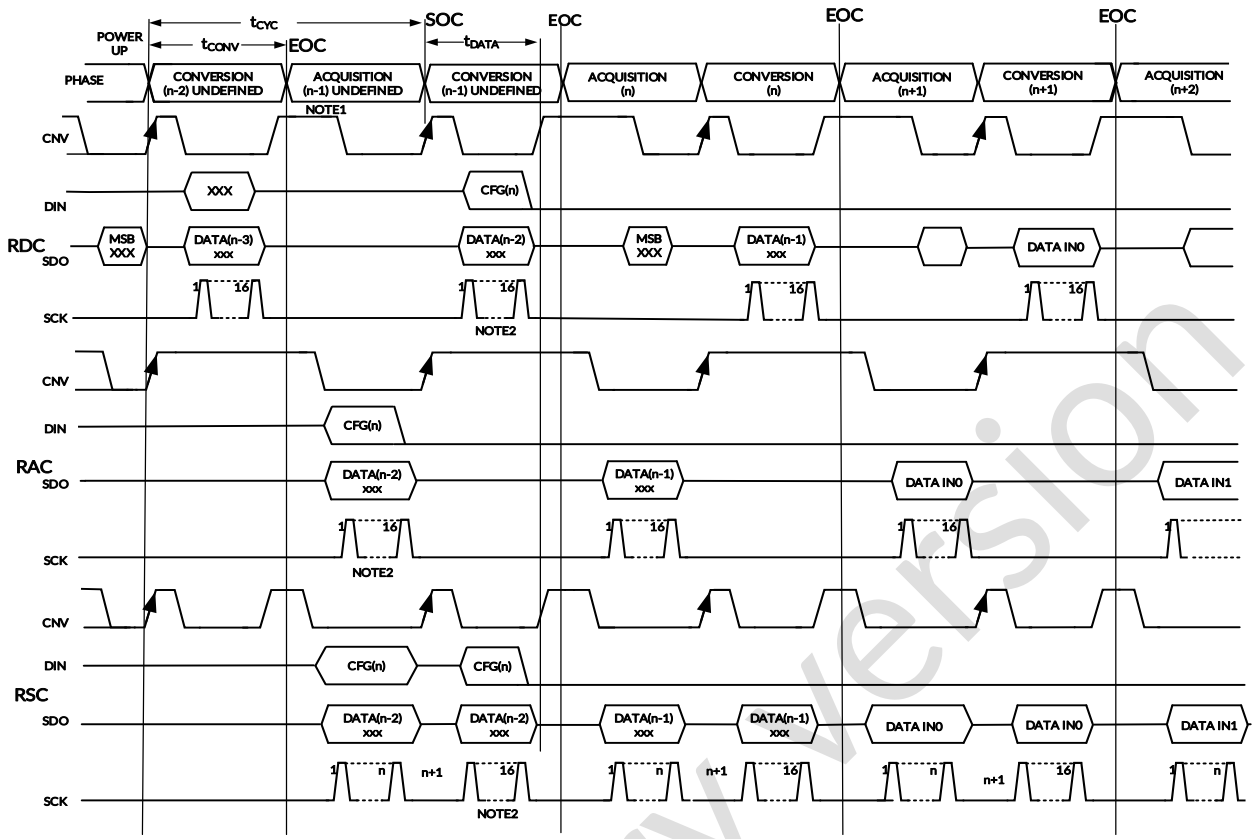


Figure 37. General Channel Sequencer Timing Without a Busy Indicator

NOTES
1. CNV MUST BE HIGH PRIOR TO THE END OF CONVERSION (EOC) TO AVOID THE BUSY INDICATOR.
2. A TOTAL OF 16 SCK FALLING EDGES ARE REQUIRED TO RETURN SDO TO HIGH-Z. IF CFG READBACK IS ENABLED, A TOTAL OF 30 SCK FALLING EDGES IS REQUIRED TO RETURN SDO TO HIGH-Z.

10.8 Read/Write Spanning Conversion Without A Busy Indicator

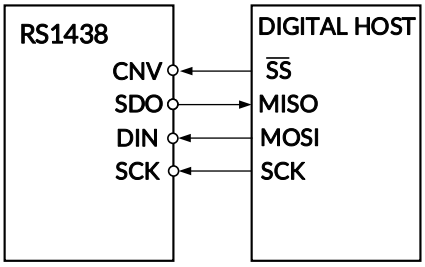
This mode is used when the RS1438 are connected to any host using an SPI, serial port, or FPGA. The connection diagram is shown in Figure 38, and the corresponding timing is given in Figure 39. For the SPI, the host must use CPHA = CPOL = 0. Reading/writing spanning conversion is shown, which covers all three modes detailed in the Digital Interface section. For this mode, the host must generate the data transfer based on the conversion time. For an interrupt driven transfer that uses a busy indicator, refer to the Read/Write Spanning Conversion with a Busy Indicator section.

A rising edge on CNV initiates a conversion, forces SDO to high impedance, and ignores data present on DIN. After a conversion initiates, it continues until completion, irrespective of the state of CNV. CNV must be returned high before the safe data transfer time (t_{DATA}), and held high beyond the conversion time (t_{CONV}) to avoid generation of the busy signal indicator.

After the conversion is complete, the RS1438 enters the acquisition phase and power-down. When the host brings CNV low after t_{CONV} (maximum), the MSB enables on SDO. The host also must enable the MSB of the CFG register at this time (if necessary) to begin the CFG update. While CNV is low, both a CFG update and a data readback take place. The first 14 SCK rising edges are used to update the CFG, and the first 15 SCK falling edges clock out the conversion results starting with MSB − 1. The restriction for both configuring and reading is that they both must occur before the t_{DATA} time of the next conversion elapses. All 14 bits of CFG[13:0] must be written or they are ignored. In addition, if the 16-bit conversion result is not read back before t_{DATA} elapses, it is lost.

The SDO data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th (or 30th) SCK falling edge, or when CNV goes high (whichever occurs first), SDO returns to high impedance.

If CFG readback is enabled, the CFG register associated with the conversion result is read back MSB first following the LSB of the conversion result. A total of 30 SCK falling edges is required to return SDO to high impedance if this is enabled.



FOR SPI USE CPHA=0,CPOL=0.

Figure 38. Connection Diagram for the RS1438 Without a Busy Indicator

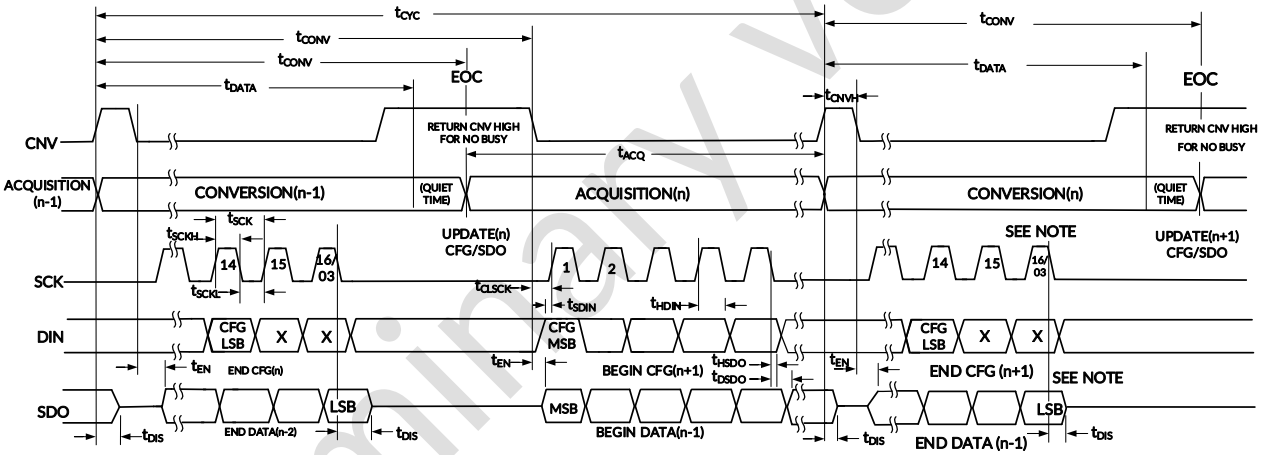


Figure 39. Serial Interface Timing for the RS1438 Without a Busy Indicator

NOTES
1. THE LSB IS FOR CONVERSION RESULTS OR THE CONFIGURATION REGISTER CFG (n – 1) IF
   15 SCK FALLING EDGES = LSB OF CONVERSION RESULTS.
   29 SCK FALLING EDGES = LSB OF CONFIGURATION REGISTER.
   ON THE 16TH OR 30TH SCK FALLING EDGE, SDO IS DRIVEN TO HIGH IMPENDANCE.

10.9 Read/Write Spanning Conversion With A Busy Indicator

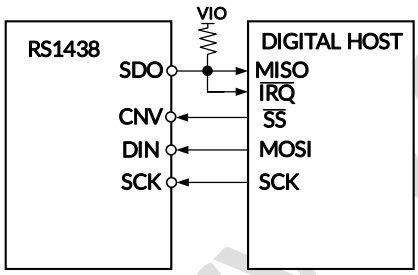
This mode is used when the RS1438 is connected to any host using an SPI, serial port, or FPGA with an interrupt input. The connection diagram is shown in Figure 40 and the corresponding timing is given in Figure 41. For the SPI, the host must use CPHA = CPOL = 1. Reading/writing spanning conversion is shown, which covers all three modes detailed in the Digital Interface section.

A rising edge on CNV initiates a conversion, ignores data present on DIN, and forces SDO to high impedance. After the conversion initiates, it continues until completion, irrespective of the state of CNV. CNV must be returned low before the safe data transfer time (t_{DATA}), and then held low beyond the conversion time (t_{CONV}) to generate the busy signal indicator. When the conversion is complete, SDO transitions from high impedance to low (data ready), and with a pull-up to VIO, SDO can be used to interrupt the host to begin data transfer.

After the conversion is complete, the RS1438 enters the acquisition phase and power-down. The host must enable the MSB of the CFG register at this time (if necessary) to begin the CFG update. While CNV is low, both a CFG update and a data readback take place. The first 14 SCK rising edges are used to update the CFG register, and the first 16 SCK falling edges clock out the conversion results starting with the MSB. The restriction for both configuring and reading is that they both occur before the t_{DATA} time elapses for the next conversion. All 14 bits of CFG[13:0] must be written or they are ignored. If the 16-bit conversion result is not read back before t_{DATA} elapses, it is lost.

The SDO data is valid on both SCK edges. Although the rising edge can capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17th (or 31st) SCK falling edge, SDO returns to high impedance. If the optional SCK falling edge is not used, the busy feature cannot be detected, as described in the General Timing with a Busy Indicator section.

If CFG readback is enabled, the CFG register associated with the conversion result is read back MSB first following the LSB of the conversion result. A total of 31 SCK falling edges is required to return SDO to high impedance if this is enabled.



FOR SPI USE CPHA=1,CPOL=1.

Figure 40. Connection Diagram for the RS1438 with a Busy Indicator

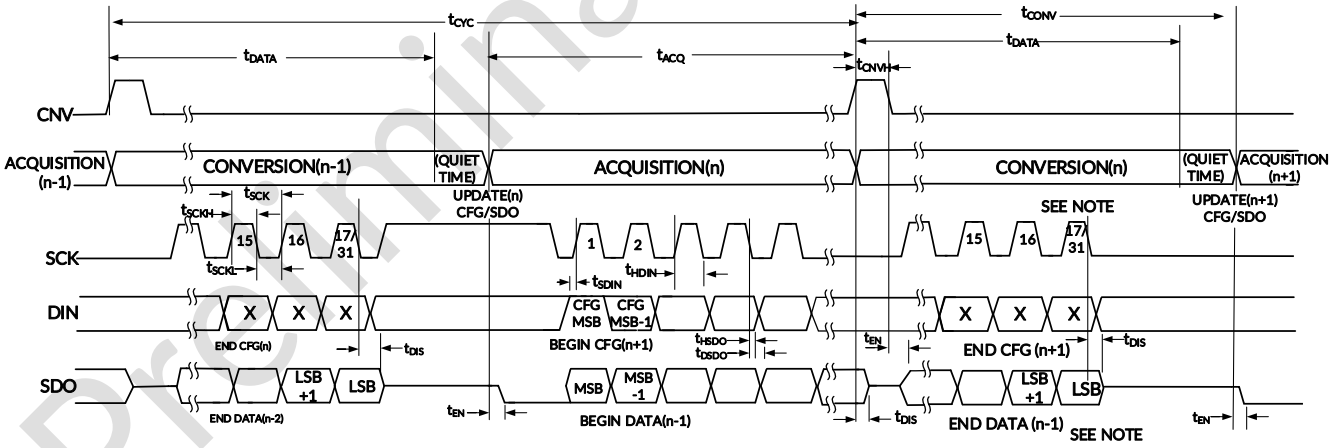


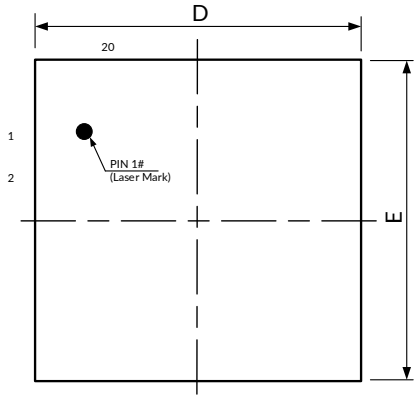
Figure 41. Serial Interface Timing for the RS1438 with a Busy Indicator

NOTES:

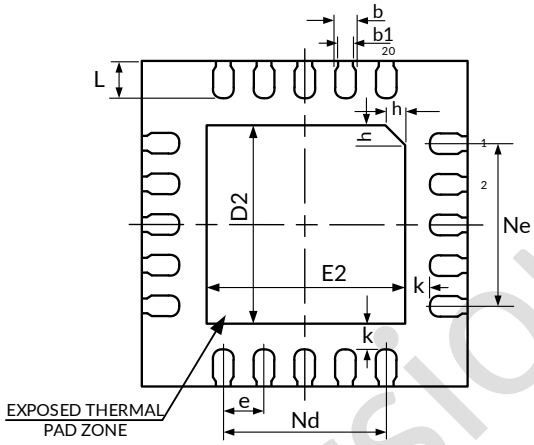
1. THE LSB IS FOR CONVERSION RESULTS OR THE CONFIGURATION REGISTER CFG (n – 1) IF
   16 SCK FALLING EDGES = LSB OF CONVERSION RESULTS.
   30 SCK FALLING EDGES = LSB OF CONFIGURATION REGISTER.
   ON THE 17TH OR 31st SCK FALLING EDGE, SDO IS DRIVEN TO HIGH IMPENDANCE.
   OTHERWISE, THE LSB REMAINS ACTIVE UNTIL THE BUSY INDICATOR IS DRIVEN LOW.

11 PACKAGE OUTLINE DIMENSIONS

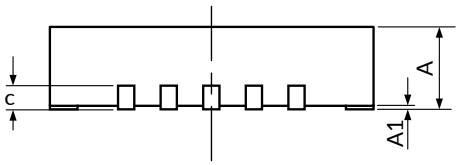
QFN4X4-20 (4)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.032
A1	0.000	0.050	0.000	0.002
b	0.200	0.300	0.008	0.012
b1	0.180 REF (2)		0.008 REF (2)	
c	0.203 REF (2)		0.008 REF (2)	
D (1)	3.900	4.100	0.154	0.161
D2	2.600	2.800	0.102	0.110
e	0.500 BSC (3)		0.020 BSC (3)	
Nd	2.000 BSC (3)		0.079 BSC (3)	
E (1)	3.900	4.100	0.154	0.161
E2	2.600	2.800	0.102	0.110
Ne	2.000 BSC (3)		0.079 BSC (3)	
L	0.350	0.450	0.014	0.018
K	0.250 REF (2)		0.010 REF (2)	
h	0.300	0.400	0.012	0.016

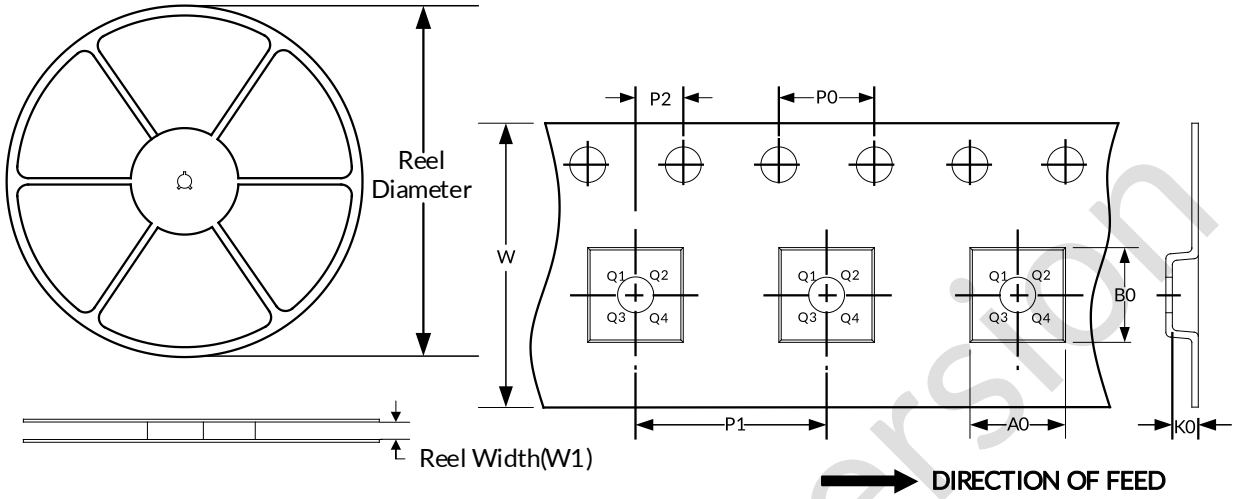
NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
4. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
QFN4X4-20	13”	12.4	4.4	4.3	1.3	4.0	8.0	2.0	12.0	Q2

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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