RS1328 12-Bit Micro-Power OCTAL Digital-to-Analog Converter With Rail-to-Rail Outputs

1 FEATURES

- **Ensured Monotonicity**
- **Low Power Operation**
- **Rail-to-Rail Voltage Output**
- **Daisy-Chain Capability**
- **Power-on Reset to 0 V**
- **Simultaneous Output Updating**
- **Individual Channel Power-Down Capability**
- **Wide Power Supply Range (2.7 V to 5.5 V)**
- **Dual Reference Voltages With Range of 0.5 V to V_A**
- **Operating Temperature Range of −40°C to 125°C**
- **Smallest Package in the Industry**
- **Resolution 12 Bits**
- **INL ±2 LSB (Typical)**
- **DNL +0.3/−0.15 LSB (Typical)**
- **Settling Time 2 µs (Typical)**
- **Zero Code Error 4 mV (Typical)**
- **Full-Scale Error −0.04 %FSR (Typical)**
- **Supply Power**
  2.10mW (3V) / 4.55mW (5V) Typical
- **Power Down 0.3µW (3V) / 1µW (5V) Typical**

2 APPLICATIONS

- **Battery-Powered Instruments**
- **Digital Gain and Offset Adjustment**
- **Programmable Voltage and Current Sources**
- **Programmable Attenuators**
- **Voltage Reference for ADCs**
- **Sensor Supply Voltage**
- **Range Detectors**

3 DESCRIPTIONS

The RS1328 is a full-featured, general-purpose OCTAL 12-bit voltage-output digital-to-analog converter (DAC) that can operate from a single 2.7V to 5.5V supply and consumes 2.10mW at 3V and 4.55mW at 5V. The RS1328 is packaged in a 16 lead TSSOP package. The on-chip output amplifiers allow rail-to-rail output swing, and the 3 wire serial interface operates at clock rates up to 40MHz over the entire supply voltage range. The serial interface is compatible with standard SPI™, QSPI, MICROWIRE, and DSP interfaces. The RS1328 also offers daisy-chain operation, where an unlimited number of RS1328 can be updated simultaneously using a single serial interface.

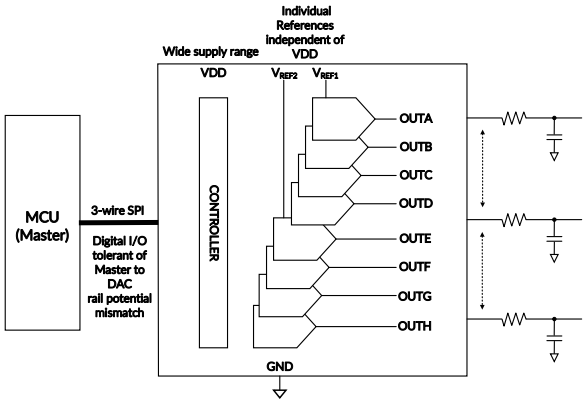
There are two references for the RS1328. One reference input serves channels A through D, while the other reference serves channels E through H. Each reference can be set independently between 0.5 V and V_A, providing the widest possible output dynamic range. The RS1328 has a 16-bit input shift register that controls the mode of operation, the power-down condition, and the register/output value of the DAC channels. All eight DAC outputs can be updated simultaneously or individually.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1328	TSSOP16	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2025/07/09	Preliminary version completed
A.0.1	2025/08/28	Update Electrical Characteristics

5 DESCRIPTION

A power-on reset circuit ensures that the DAC outputs power up to zero volts and remain there until there is a valid write to the device. The power-down feature of the RS1328 allows each DAC to be independently powered with three different termination options. With all the DAC channels powered down, power consumption reduces to less than 0.3μW at 3V and less than 1μW at 5V. The low power consumption and small packages of the RS1328 make it an excellent choice for use in battery-operated equipment. The RS1328 operates over the extended industrial temperature range of −40°C to 125°C.

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS1328	RS1328XTSS16	-40°C ~ 125°C	TSSOP16	RS1328	MSL1	Tape and Reel, 4000

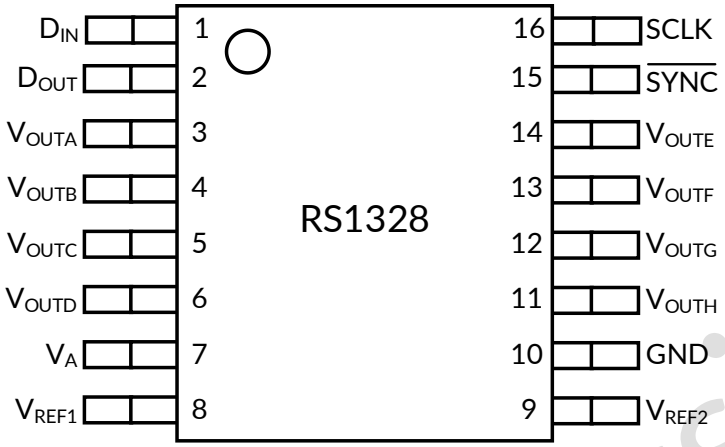
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

7 PIN CONFIGURATION AND FUNCTIONS (TOP VIEW)



TSSOP16

PIN DESCRIPTION

NAME	PIN	TYPE	DESCRIPTION
D_{IN}	1	Digital Input	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
D_{OUT}	2	Digital Output	Serial Data Output. D_{OUT} is utilized in daisy chain operation and is connected directly to a D_{IN} pin on another RS1328. Data is not available at D_{OUT} unless $\overline{SYNC}$ remains low for more than 16 SCLK cycles.
V_{OUTA}	3	Analog Output	Channel A Analog Output Voltage.
V_{OUTB}	4	Analog Output	Channel B Analog Output Voltage.
V_{OUTC}	5	Analog Output	Channel C Analog Output Voltage.
V_{OUTD}	6	Analog Output	Channel D Analog Output Voltage.
V_A	7	Analog Output	Power supply input. Must be decoupled to GND.
V_{REF1}	8	Analog Input	Unbuffered reference voltage shared by Channels A, B, C, and D. Must be decoupled to GND.
V_{REF2}	9	Analog Input	Unbuffered reference voltage shared by Channels E, F, G, and H. Must be decoupled to GND.
GND	10	Ground	Ground reference for all on-chip circuitry.
V_{OUTH}	11	Analog Output	Channel H Analog Output Voltage.
V_{OUTG}	12	Analog Output	Channel G Analog Output Voltage.
V_{OUTF}	13	Analog Output	Channel F Analog Output Voltage.
V_{OUTE}	14	Analog Output	Channel E Analog Output Voltage.
$\overline{SYNC}$	15	Digital Input	Frame Synchronization Input. When this pin goes low, data is written into the DAC's input shift register on the falling edges of SCLK. After the 16th falling edge of SCLK, rising edge of $\overline{SYNC}$ causes the DAC to be updated. If $\overline{SYNC}$ is brought high before the 15th falling edge of SCLK, the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
SCLK	16	Digital Input	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Supply voltage, V_A			6.5	V
Voltage on any input pin		-0.3	6.5	V
Input current at any pin (3)			10	mA
Package input current (3)			30	mA
Power consumption at T_A = 25°C		See (4)		
Package thermal impedance, θ_{JA} (5)	TSSOP16		135	°C/W
Junction temperature			150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.

(3) When the input voltage at any pin exceeds the power supplies (that is, less than GND, or greater than V_A), the current at that pin must be limited to 10 mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.

(4) The absolute maximum junction temperature (T_{JMAX}) for this device is 150°C. The maximum allowable power dissipation is dictated by T_{JMAX}, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (for example, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions must always be avoided.

(5) The package thermal impedance is calculated in accordance with JESD-51.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

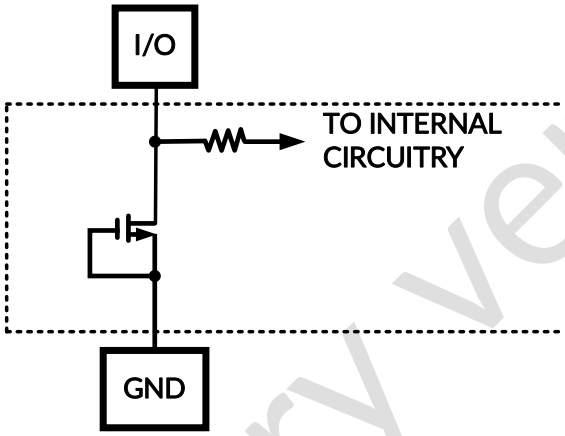
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating Temperature Range	-40	125	°C
Supply voltage, V_A	2.7	5.5	V
Reference Voltage, $V_{REF1,2}$	0.5	V_A	V
Digital Input Voltage (1)	0	5.5	V
Output load	0	1500	pF
SCLK Frequency		40	MHz

(1) The inputs are protected as shown below. Input voltage magnitudes up to 5.5 V, regardless of V_A, will not cause errors in the conversion result. For example, if V_A is 3 V, the digital input pins can be driven with a 5 V logic device.



8.4 Electrical Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF1} = V_{REF2} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are at T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE						
Resolution		$T_{MIN} \le T_A \le T_{MAX}$	12			Bits
Monotonicity		$T_{MIN} \le T_A \le T_{MAX}$	12			Bits
INL	Integral Non-Linearity	T_A = 25°C		±2	±3.5	LSB
		$T_{MIN} \le T_A \le T_{MAX}$		±3		LSB
DNL	Differential Non-Linearity	T_A = 25°C	-0.5	+0.3/-0.15	0.7	LSB
		$T_{MIN} \le T_A \le T_{MAX}$		+0.4/-0.3		LSB
ZE	Zero Code Error	V_A = 2.7 V, I_{OUT} = 0		3	6	mV
		$T_{MIN} \le T_A \le T_{MAX}$		4.5		
		V_A = 5.5 V, I_{OUT} = 0		4	7	mV
		$T_{MIN} \le T_A \le T_{MAX}$		6		
FSE	Full-Scale Error	I_{OUT} = 0		-0.04	±0.12	%FSR
		$T_{MIN} \le T_A \le T_{MAX}$		±0.06		
GE	Gain Error	T_A = 25°C		-0.15	±0.25	%FSR
		$T_{MIN} \le T_A \le T_{MAX}$		-0.2		
ZCED	Zero Code Error Drift			20		µV/°C
TC GE	Gain Error Tempco			-0.6		ppm/°C
OUTPUT CHARACTERISTICS						
	Output Voltage Range	$T_{MIN} \le T_A \le T_{MAX}$	0		$V_{REF1,2}$	V
I_{OZ}	High-Impedance Output Leakage Current (1)	$T_{MIN} \le T_A \le T_{MAX}$		±0.1		µA
ZCO	Zero Code Output	V_A = 3 V, I_{OUT} = 200 µA		9	11	mV
		V_A = 3 V, I_{OUT} = 1 mA		35	45	
		V_A = 5 V, I_{OUT} = 200 µA		6	8	
		V_A = 5 V, I_{OUT}= 1 mA		25	31	
FSO	Full Scale Output	V_A = 3 V, I_{OUT} = 200 µA	2.887	2.988		V
		V_A = 3 V, I_{OUT} = 1 mA	2.942	2.948		
		V_A = 5 V, I_{OUT} = 200 µA	4.990	4.992		
		V_A = 5 V, I_{OUT} = 1 mA	4.961	4.965		
I_{OS}	Output Short-Circuit Current (I_{SOURCE}) (2)	V_A = 3 V, V_{OUT} = 0 V, Input Code = FFFh		-35		mA
		V_A = 5 V, V_{OUT} = 0 V, Input Code = FFFh		-38		
I_{OS}	Output Short-Circuit Current (I_{SINK}) (2)	V_A = 3 V, V_{OUT} = 3 V, Input Code = 000h		57		mA
		V_A = 5 V, V_{OUT} = 5 V, Input Code = 000h		58		
I_O	Continuous Output Current per channel (1)	T_A = 105°C			8	mA
		T_A = 125°C			4.5	mA
C_L	Maximum Load Capacitance	R_L = ∞		1500		pF
		R_L = 2 kΩ		1500		
Z_{OUT}	DC Output Impedance	V_A = 2.7 V, Input Code = 7FFh		0.5	1	Ω
		V_A = 5.5 V, Input Code = 7FFh		0.5	1	Ω

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF1} = V_{REF2} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are at T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
REFERENCE INPUT CHARACTERISTICS							
$V_{REF1,2}$	Input Range Minimum	T_A = 25°C			0.5		V
		$T_{MIN} \le T_A \le T_{MAX}$		2.7			
	Input Range Maximum	$T_{MIN} \le T_A \le T_{MAX}$				V_A	V
	Input Impedance				30		kΩ
LOGIC INPUT CHARACTERISTICS							
I_{IN}	Input Current (1)	$T_{MIN} \le T_A \le T_{MAX}$			±0.1		µA
V_{IL}	Input Low Voltage	V_A = 2.7 V to 3.6 V			0.6		V
		V_A = 2.7 V to 3.6 V, $T_{MIN} \le T_A \le T_{MAX}$				0.6	
		V_A = 4.5 V to 5.5 V			1.1		V
		V_A = 4.5 V to 5.5 V, $T_{MIN} \le T_A \le T_{MAX}$				0.8	
V_{IH}	Input High Voltage	V_A = 2.7 V to 3.6 V			1.5		V
		V_A = 2.7 V to 3.6 V, $T_{MIN} \le T_A \le T_{MAX}$		2.1			
		V_A = 4.5 V to 5.5 V			2.2		V
		V_A = 4.5 V to 5.5 V, $T_{MIN} \le T_A \le T_{MAX}$		2.4			
C_{IN}	Input Pin Capacitance (1)	$T_{MIN} \le T_A \le T_{MAX}$				3	pF
POWER REQUIREMENTS							
V_A	Supply Voltage Minimum	$T_{MIN} \le T_A \le T_{MAX}$		2.7			V
	Supply Voltage Maximum	$T_{MIN} \le T_A \le T_{MAX}$				5.5	V
I_N	Normal Supply Current for supply pin V_A	f_{SCLK} = 30MHz, $f_{\overline{SYNC}}$=176kHz, output unloaded	V_A = 3 V		496		µA
			V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$		553		µA
			V_A = 5 V		573		µA
			V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$		632		µA
	Normal Supply Current for V_{REF1} or V_{REF2}	f_{SCLK} = 30MHz, output unloaded	V_A = 3 V		102		µA
			V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$		102		µA
			V_A = 5 V		170		µA
			V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$		170		µA
I_{ST}	Static Supply Current for supply pin V_A	f_{SCLK} = 0MHz, output unloaded	V_A = 3 V		433	510	µA
			V_A = 5 V		480	615	µA
	Static Supply Current for V_{REF1} or V_{REF2}	f_{SCLK}= 0MHz, output unloaded	V_A = 3 V		102		µA
			V_A = 5 V		170		µA

(1) This parameter is specified by design and/or characterization and is not tested in production.

(2) This parameter does not represent a condition which the DAC can sustain continuously. See the continuous output current specification for the maximum DAC output current per channel.

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF1} = V_{REF2} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are at T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{PD}	Total Power Down Supply Current for all PD Modes (1)	f_{SCLK} = 30MHz, $\overline{SYNC}$= V_A and D_{IN} = 0V, after PD mode loaded	V_A = 3 V		26		µA
			V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$		51		µA
			V_A = 5 V		62		µA
			V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$		98		µA
		f_{SCLK} = 0MHz, $\overline{SYNC}$= V_A and D_{IN} = 0V, after PD mode loaded	V_A = 3 V		0.1	0.3	µA
			V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$		2.5		µA
			V_A = 5 V		0.2	0.5	µA
			V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$		3.6		µA
P_N	Total Power Consumption (output unloaded)	f_{SCLK} =30MHz, $f_{\overline{SYNC}}$=176kHz, output unloaded	V_A = 3 V		2.10		mW
			V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$		2.27		
			V_A = 5 V		4.55		mW
			V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$		4.86		
		f_{SCLK} = 0MHz, output unloaded	V_A = 3 V		1.91		mW
			V_A = 5 V		4.10		mW
P_{PD}	Total Power Consumption in all PD Modes (1)	f_{SCLK} = 30MHz, $\overline{SYNC}$= V_A and D_{IN} = 0V, after PD mode loaded	V_A = 3 V		78		µW
			V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$		153		
			V_A = 5 V		310		µW
			V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$		490		
		f_{SCLK} = 0MHz, $\overline{SYNC}$= V_A and D_{IN} = 0V, after PD mode loaded	V_A = 3 V		0.3	0.9	µW
			V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$		7.35		
			V_A = 5 V		1	2.5	µW
			V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$		18		

8.5 AC and Timing Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF1} = V_{REF2} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are at T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK Frequency	T_A = 25°C			40	MHz
		$T_{MIN} \le T_A \le T_{MAX}$			30	MHz
t_S	Output Voltage Settling Time (1)	400h to C00h code change R_L = 2 kΩ, C_L = 200 pF		2		µs
		$T_{MIN} \le T_A \le T_{MAX}$		3		
SR	Output Slew Rate			1		V/µs
GI	Glitch Impulse	Code change from 800h to 7FFh		40		nV-sec
DF	Digital Feedthrough			0.5		nV-sec
DC	Digital Crosstalk			0.5		nV-sec
CROSS	DAC-to-DAC Crosstalk			1.6		nV-sec
MBW	Multiplying Bandwidth	$V_{REF1,2}$ = 2.5 V ± 2 Vpp		400		kHz
THD+N	Total Harmonic Distortion Plus Noise	$V_{REF1,2}$ = 2.5 V ± 0.5 Vpp 100 Hz < f_{IN} < 20 kHz		-77		dB
ONSD	Output Noise Spectral Density (1)	DAC Code = 800h, 10 kHz		40		nV/√Hz
ON	Output Noise (1)	BW = 30 kHz		14		µV
t_{WU}	Wake-Up Time	V_A = 3 V		5		µsec
		V_A = 5 V		3		µsec
$1/f_{SCLK}$	SCLK Cycle Time	T_A = 25°C	25			ns
		$T_{MIN} \le T_A \le T_{MAX}$	33			ns
t_{CH}	SCLK High time	T_A = 25°C		7		ns
		$T_{MIN} \le T_A \le T_{MAX}$	10			ns
t_{CL}	SCLK Low Time	T_A = 25°C		7		ns
		$T_{MIN} \le T_A \le T_{MAX}$	10			ns
t_{SS}	$\overline{SYNC}$ Set-up Time prior to SCLK Falling Edge.	T_A = 25°C		4		ns
		$T_{MIN} \le T_A \le T_{MAX}$	10			ns
t_{DS}	Data Set-up Time prior to SCLK Falling Edge.	T_A = 25°C		4		ns
		$T_{MIN} \le T_A \le T_{MAX}$	5			ns
t_{DH}	Data Hold Time after SCLK Falling Edge.	T_A = 25°C		4		ns
		$T_{MIN} \le T_A \le T_{MAX}$	5			ns
t_{SH}	$\overline{SYNC}$ Hold Time after the 16th falling edge of SCLK.	T_A = 25°C		5		ns
		$T_{MIN} \le T_A \le T_{MAX}$	6			ns
$t_{\overline{SYNC}}$	$\overline{SYNC}$ High Time	T_A = 25°C		10		ns
		$T_{MIN} \le T_A \le T_{MAX}$	15			ns

(1) This parameter is specified by design and/or characterization and is not tested in production.

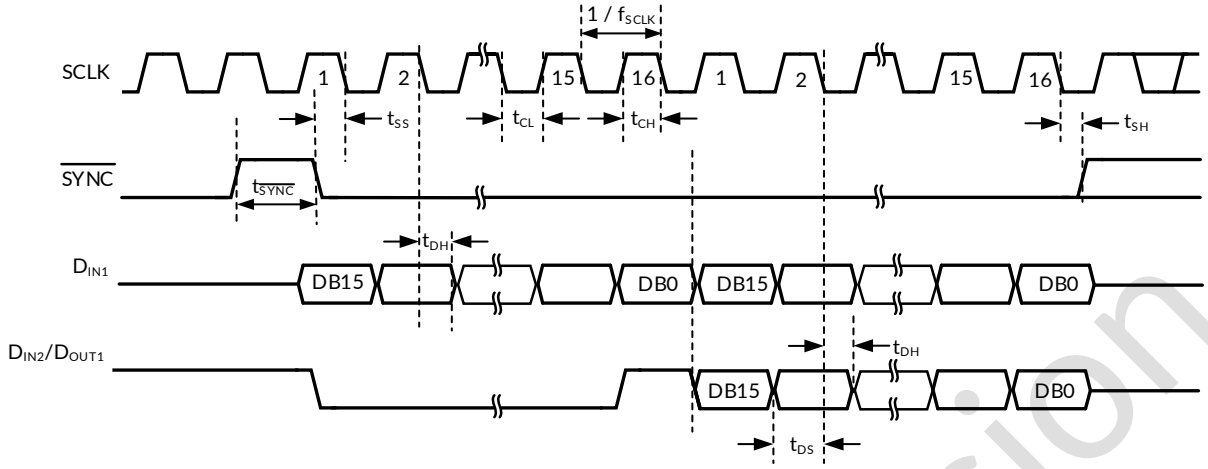


Figure 1. Serial Timing Diagram

8.6 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_A = 2.7 V to 5.5 V, $V_{REF1,2}$ = V_A, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated.

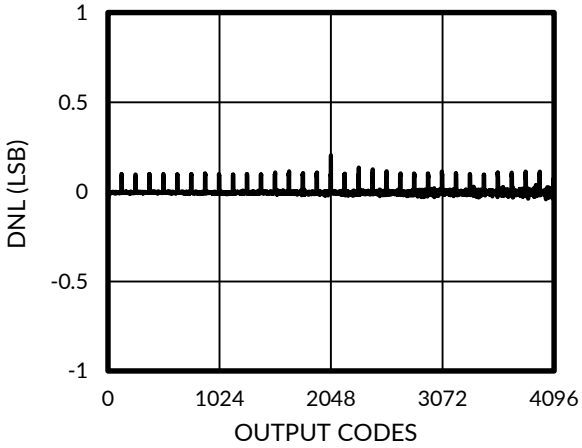


Figure 2. DNL at V_A = 3V

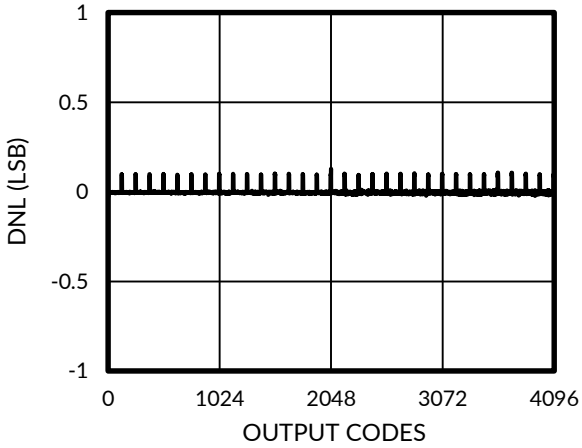


Figure 3. DNL at V_A = 5V

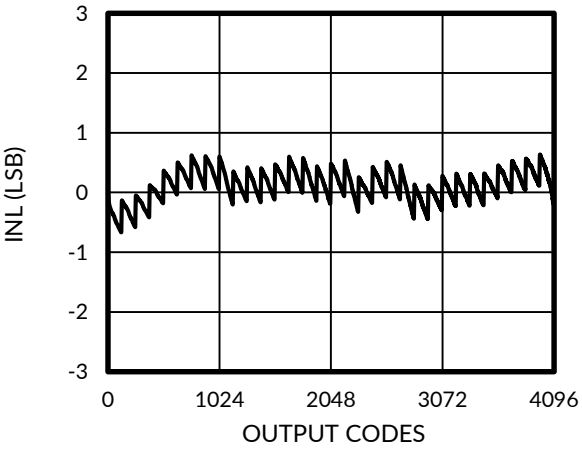


Figure 4. INL at V_A = 3V

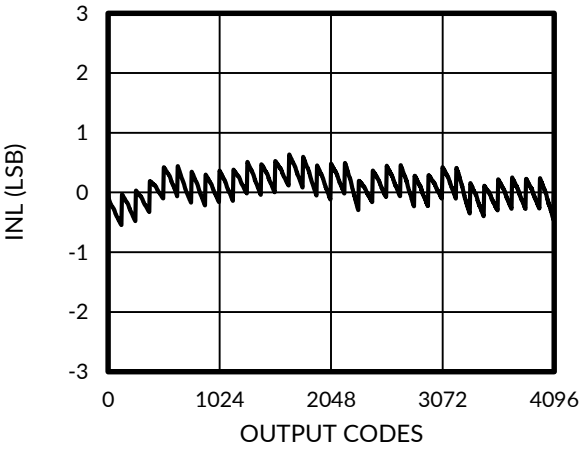


Figure 5. INL at V_A = 5V

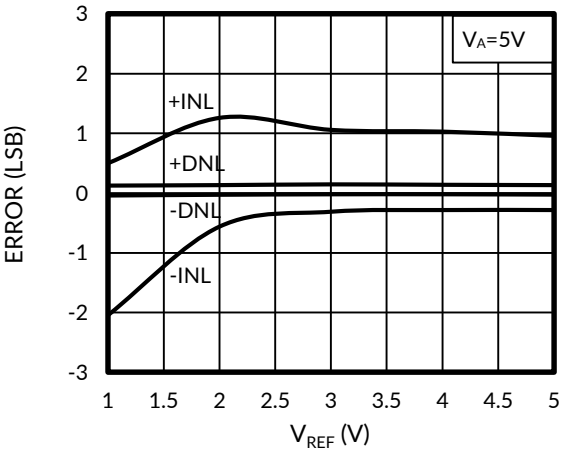


Figure 6. INL/ DNL vs V_{REF}

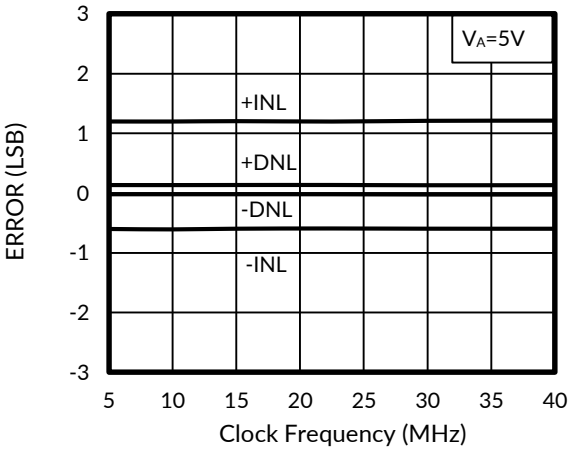


Figure 7. INL / DNL vs F_{SCLK}

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_A = 2.7 V to 5.5 V, $V_{REF1,2}$ = V_A, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated.

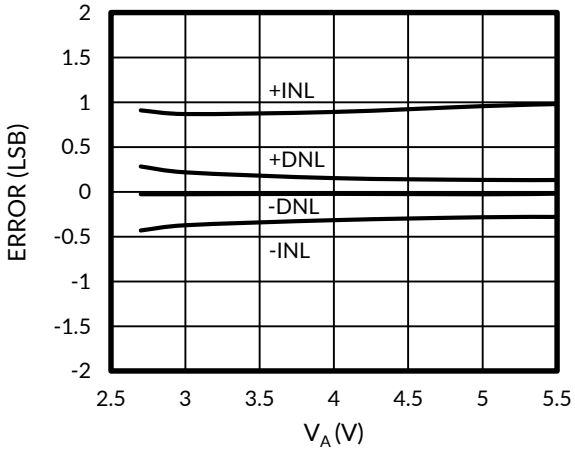


Figure 8. INL / DNL vs V_A

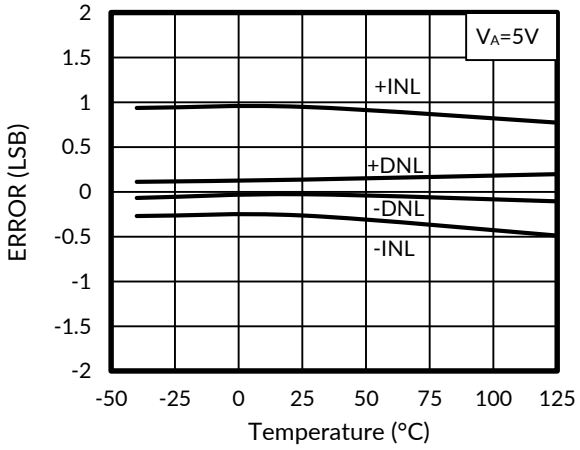


Figure 9. INL / DNL vs Temperature

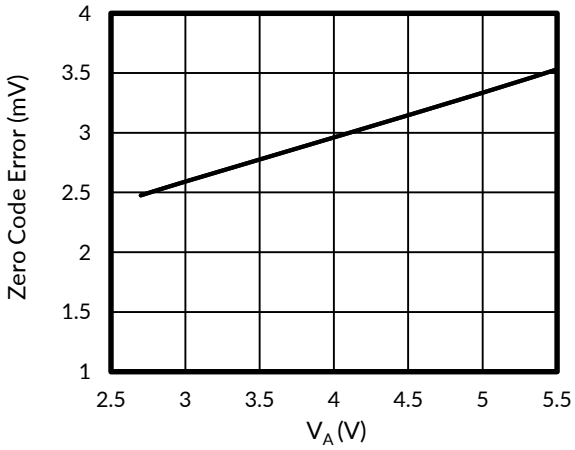


Figure 10. Zero Code Error vs V_A

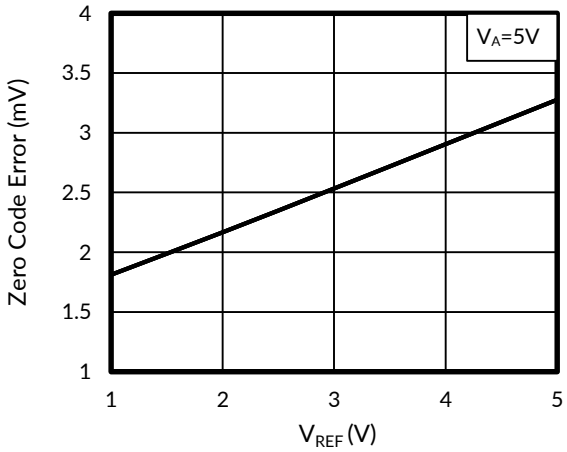


Figure 11. Zero Code Error vs V_{REF}

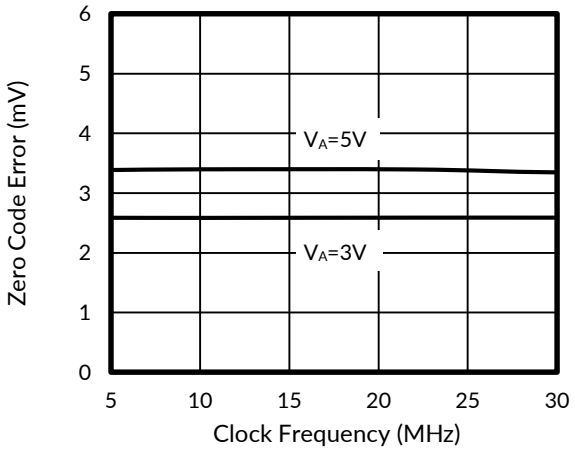


Figure 12. Zero Code Error vs F_{SCLK}

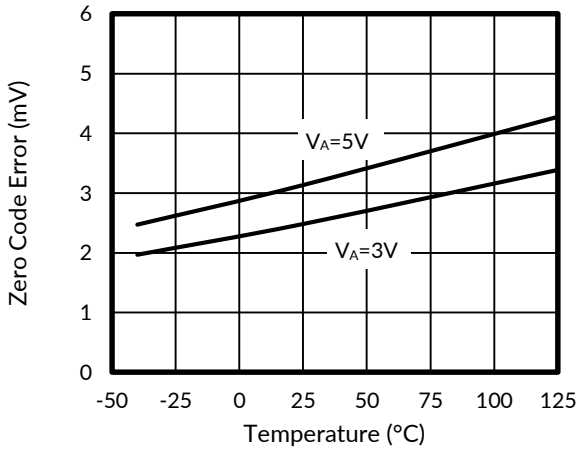


Figure 13. Zero Code Error vs Temperature

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_A = 2.7 V to 5.5 V, $V_{REF1,2}$ = V_A, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated.

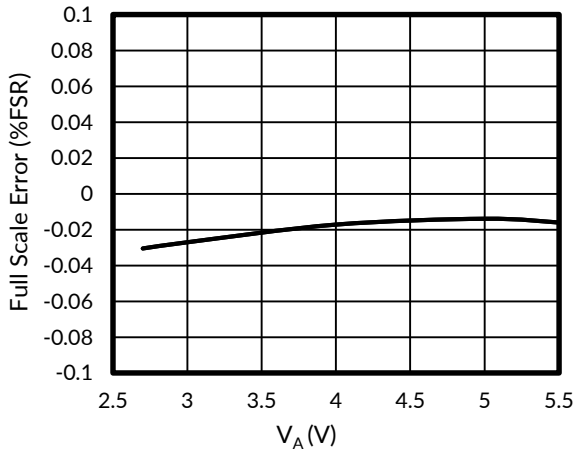


Figure 14. Full-Scale Error vs V_A

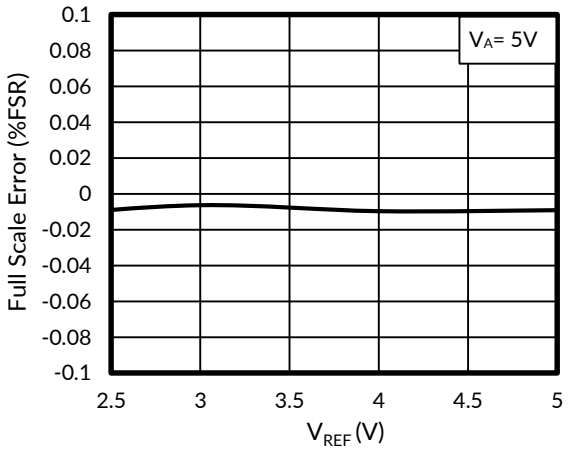


Figure 15. Full-Scale Error vs V_{REF}

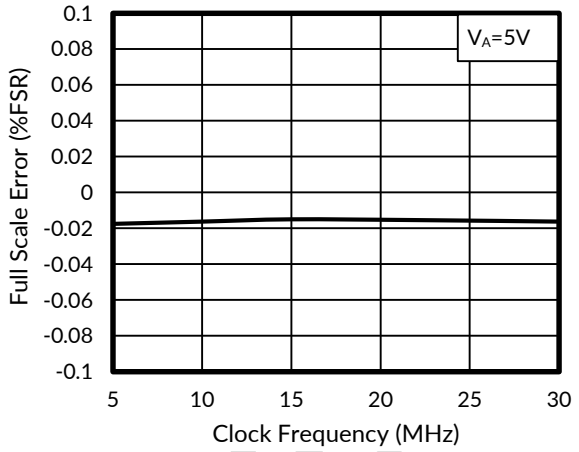


Figure 16. Full-Scale Error vs F_{SCLK}

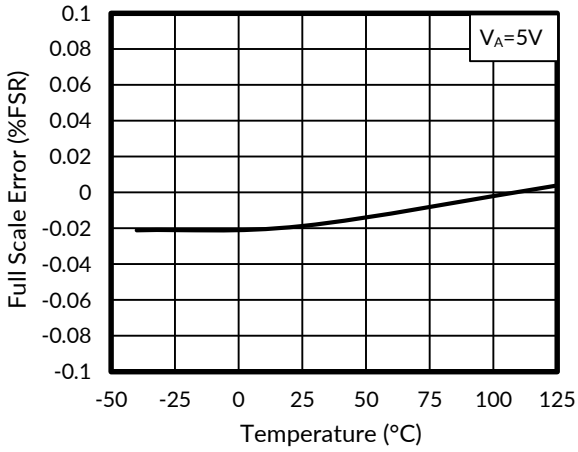


Figure 17. Full-Scale Error vs Temperature

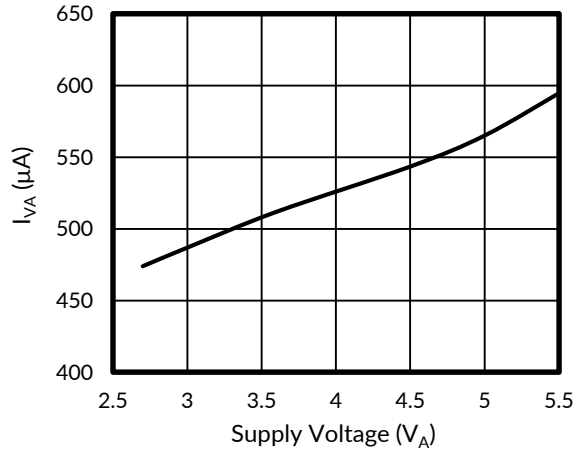


Figure 18. I_{VA} vs V_A

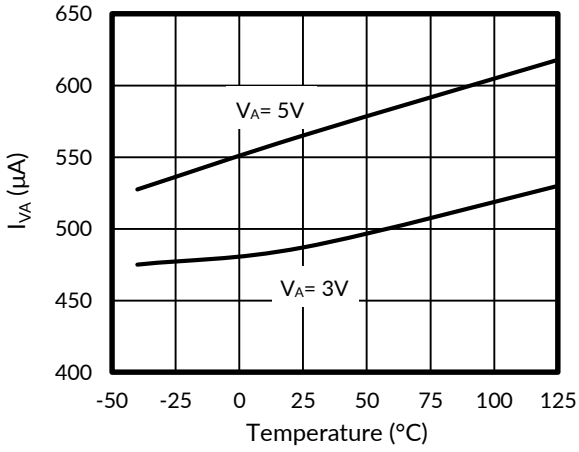


Figure 19. I_{VA} vs Temperature

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_A = 2.7 V to 5.5 V, $V_{REF1,2} = V_A$, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated.

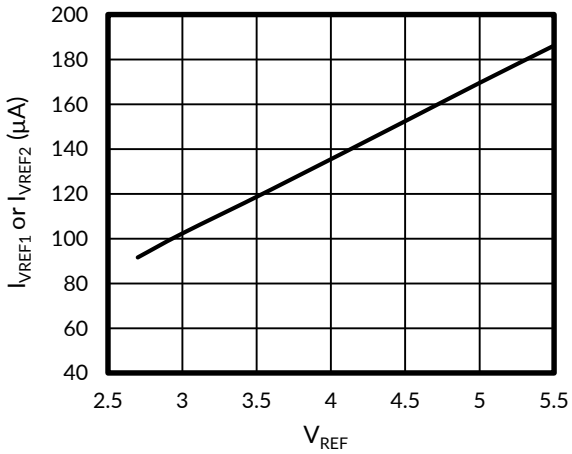


Figure 20. I_{VREF} vs V_{REF}

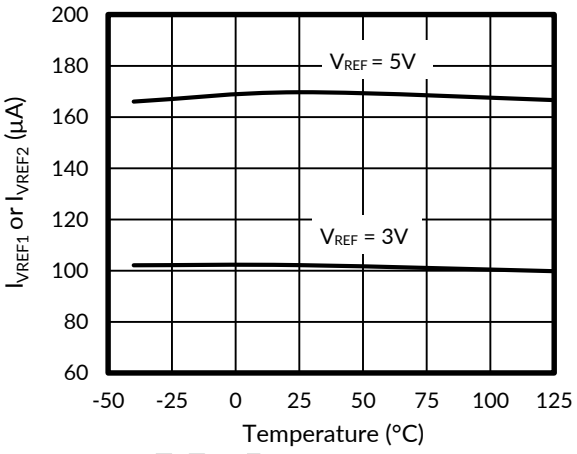


Figure 21. I_{VREF} vs Temperature

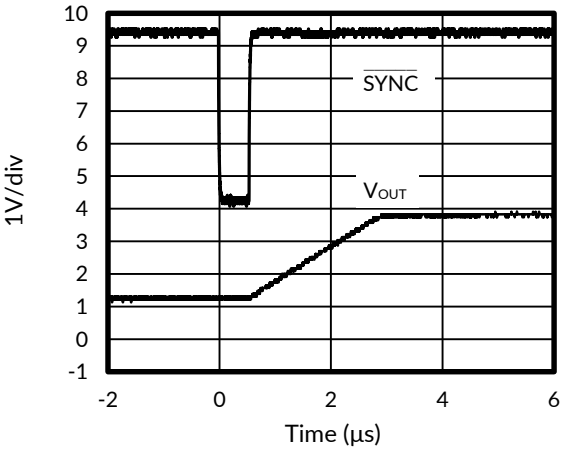


Figure 22. Settling Time

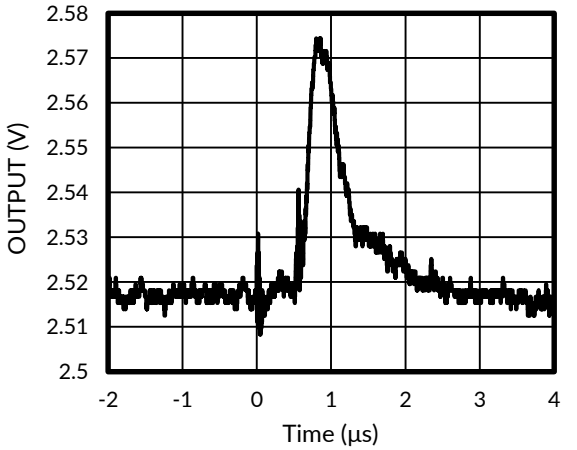


Figure 23. Glitch Response

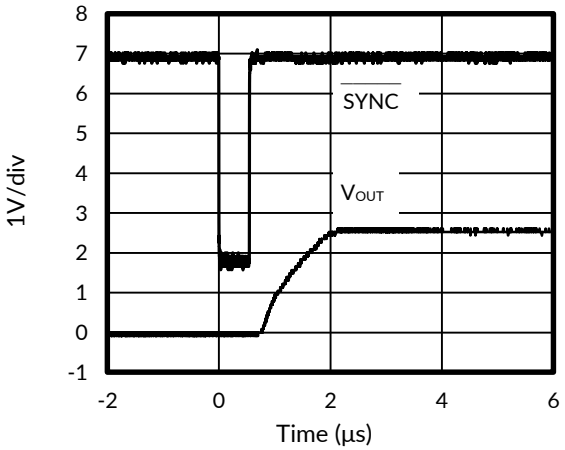


Figure 24. Wake-Up Time

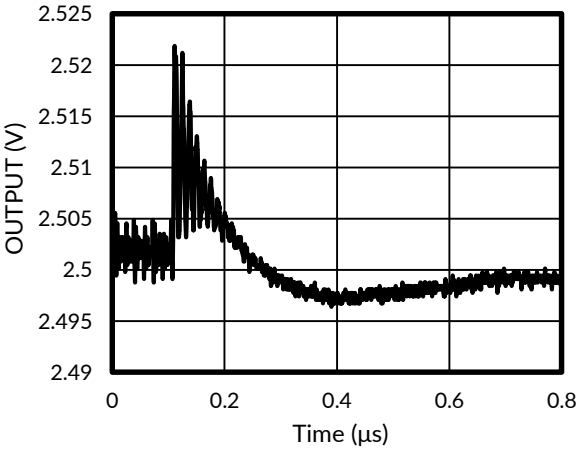


Figure 25. DAC-to-DAC Crosstalk

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_A = 2.7 V to 5.5 V, $V_{REF1,2}$ = V_A, f_{SCLK} = 30 MHz, T_A = 25°C, unless otherwise stated.

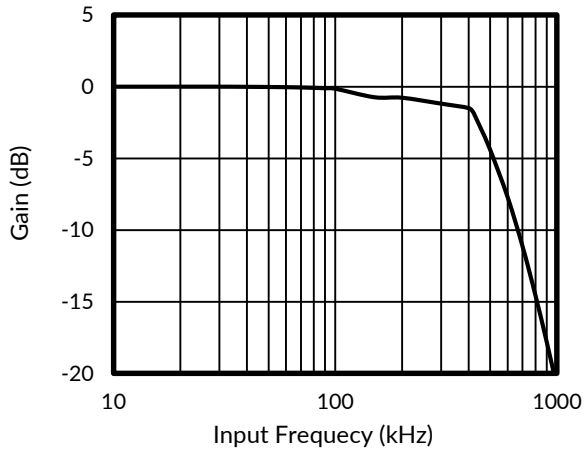


Figure 26. Multiplying Bandwidth

9 DETAILED DESCRIPTION

9.1 Overview

The RS1328 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings followed by an output buffer. The reference voltages are externally applied at V_{REF1} for DAC channels A through D, and V_{REF2} for DAC channels E through H.

9.2 Functional Block Diagram

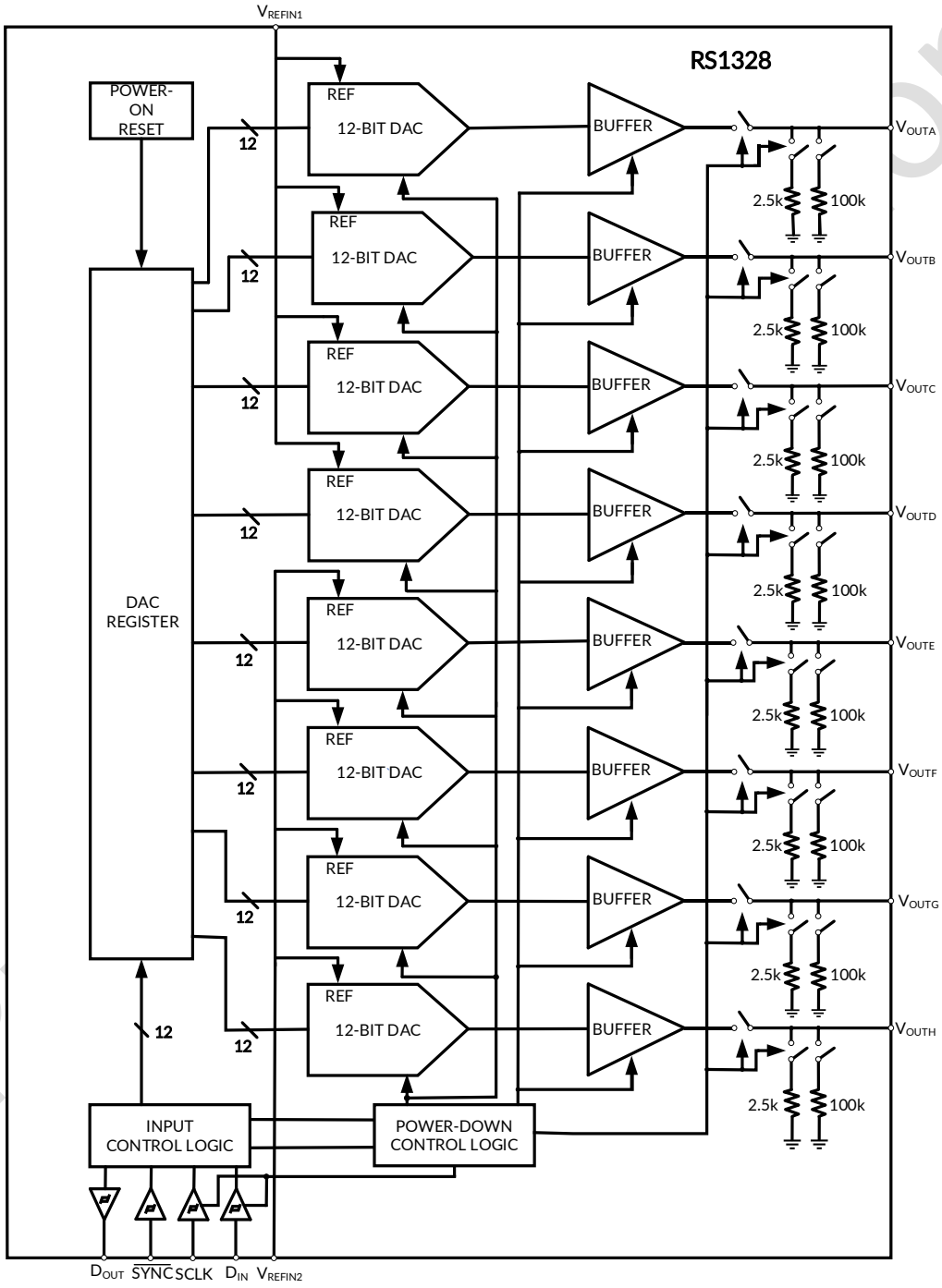


Figure 27 Functional Block Diagram

9.3 Feature Description

9.3.1 DAC Architecture

For simplicity, a single resistor string is shown in Figure 28. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage of:

$V_{OUTA,B,C,D} = V_{REF1} \times (D / 4096)$

where

D is the decimal equivalent of the binary code that is loaded into the DAC register.

$V_{OUTE,F,G,H} = V_{REF2} \times (D / 4096)$

D can take on any value between 0 and 4095. This configuration ensures that the DAC is monotonic.

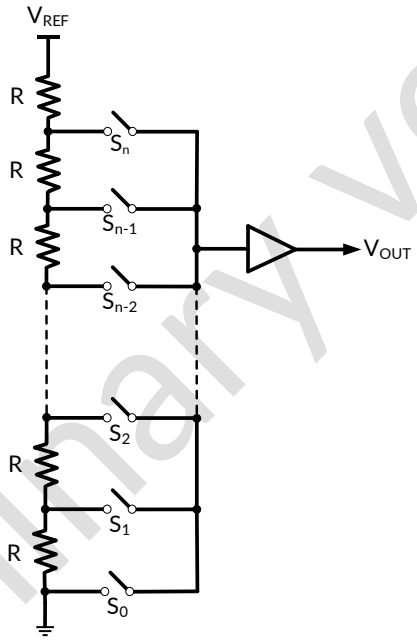


Figure 28. DAC Resistor String

Because all eight DAC channels of the RS1328 can be controlled independently, each channel consists of a DAC register and a 12-bit DAC. Figure 29 is a simple block diagram of an individual channel in the RS1328. Depending on the mode of operation, data written into a DAC register causes the 12-bit DAC output to be updated, or an additional command is required to update the DAC output. Further description of the modes of operation can be found in Serial Interface.

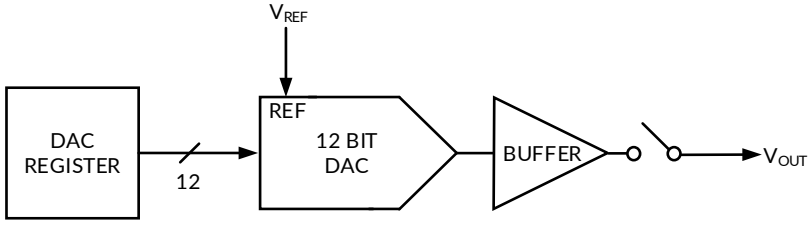


Figure 29. Single-Channel Block Diagram

9.3.2 Output Amplifiers

The output amplifiers are rail-to-rail, providing an output voltage range of 0 V to V_A when the reference is V_A. All amplifiers, including rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0 V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_A, only the lowest codes experience a loss in linearity.

The output amplifiers can drive a load of 2 kΩ in parallel with 1500 pF to ground or to V_A. The zero-code and full- scale outputs forgiven load currents are available in the Electrical Characteristics.

9.3.3 Reference Voltage

The RS1328 uses dual external references, V_{REF1} and V_{REF2}, which are shared by channels A, B, C, D and channels E, F, G, H, respectively. The reference pins are not buffered and have an input impedance of 30 kΩ. RS recommends driving V_{REF1} and V_{REF2} by voltage sources with low output impedance. The reference voltage range is 0.5 V to V_A, providing the widest possible output dynamic range.

9.3.4 Serial Interface

The three-wire interface is compatible with SPI, QSPI, and MICROWIRE, as well as most DSPs, and operates at clock rates up to 40 MHz. A valid serial frame contains 16 falling edges of SCLK. See Table 1 for information on a write sequence.

A write sequence begins by bringing the $\overline{SYNC}$ line low. Once $\overline{SYNC}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. To avoid mis-clocking data into the shift register, it is critical that $\overline{SYNC}$ not be brought low on a falling edge of SCLK (see minimum and maximum setup times for $\overline{SYNC}$ in AC and Timing Characteristics and Figure 30). On the 16th falling edge of SCLK, the last data bit is clocked into the register. The write sequence is concluded by bringing the $\overline{SYNC}$ line high. Once $\overline{SYNC}$ is high, the programmed function (a change in the DAC channel address, mode of operation, or register contents) is executed. To avoid mis-clocking data into the shift register, it is critical that $\overline{SYNC}$ be brought high between the 16th and 17th falling edges of SCLK (see minimum and maximum hold times for $\overline{SYNC}$ in AC and Timing Characteristics and Figure 30).

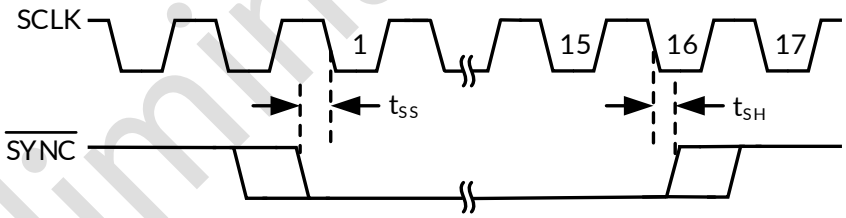


Figure 30. Single-Channel Block Diagram

If $\overline{SYNC}$ is brought high before the 15th falling edge of SCLK, the write sequence is aborted and the data that has been shifted into the input register is discarded. If $\overline{SYNC}$ is held low beyond the 17th falling edge of SCLK, the serial data presented at D_{IN} will begin to be output on D_{OUT}. More information on this mode of operation can be found in Daisy-Chain Operation. In either case, $\overline{SYNC}$ must be brought high for the minimum specified time before the next write sequence is initiated with a falling edge of $\overline{SYNC}$.

Since the D_{IN} buffer draws more current when it is high, it should be idled low between write sequences to minimize power consumption. On the other hand, $\overline{SYNC}$ should be idled high to avoid the activation of daisy chain operation where D_{OUT} is active.

9.3.5 Daisy-Chain Operation

Daisy-chain operation allows communication with any number of RS1328s using a single serial interface. As long as the correct number of data bits are input in a write sequence (multiple of sixteen bits), a rising edge of $\overline{SYNC}$ will properly update all DACs in the system.

To support multiple devices in a daisy chain configuration, SCLK and $\overline{SYNC}$ are shared across all RS1328s and D_{OUT} of the first DAC in the chain is connected to D_{IN} of the second. Figure 31 shows three RS1328s connected in daisy chain fashion. Similar to a single channel write sequence, the conversion for a daisy chain operation begins on a falling edge of $\overline{SYNC}$ and ends on a rising edge of $\overline{SYNC}$. A valid write sequence for n devices in a chain requires n times 16 falling edges to shift the entire input data stream through the chain. Daisy chain operation is ensured for a maximum SCLK speed of 30 MHz.

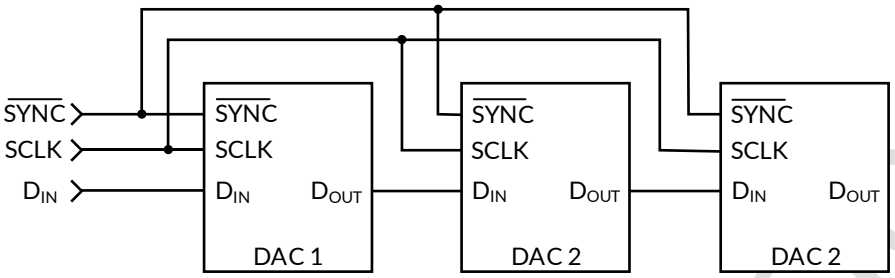


Figure 31. Daisy-Chain Configuration

The serial data output pin, D_{OUT}, is available on the RS1328s to allow daisy-chaining of multiple RS1328s devices in a system. In a write sequence, D_{OUT} remains low for the first 14 falling edges of SCLK before going high on the 15th falling edge. Subsequently, the next 16 falling edges of SCLK will output the first 16 data bits entered into D_{IN}. Figure 32 shows the timing of 3 RS1328s in Figure 31. In this instance, It takes 48 falling edges of SCLK followed by a rising edge of $\overline{SYNC}$ to load all three RS1328 with the appropriate register data. On the rising edge of $\overline{SYNC}$, the programmed function is executed in each RS1328s simultaneously.

When connecting multiple devices in a daisy-chain configuration, it is important to note that the RS1328s will update the D_{OUT} signal on the falling edge of SCLK, and this will be sampled by the next DAC in the daisy chain on the next falling edge of the clock. Ensure that the timing requirements are met for proper operation. Specifically, pay attention to the data hold time after the SCLK falling (t_{DH}) requirement. Improper layout or loading may delay the clock signal between devices. If delayed to the point that data changes prior to meeting the hold time requirement, incorrect data can be sampled. If the clock delay cannot be resolved, an alternative solution is to add a delay between the D_{OUT} of one device and D_{IN} of the following device in the daisy chain. This increases the hold time margin and allows for correct sampling. Be aware though, that the tradeoff with this fix is that too much delay eventually impacts the setup time.

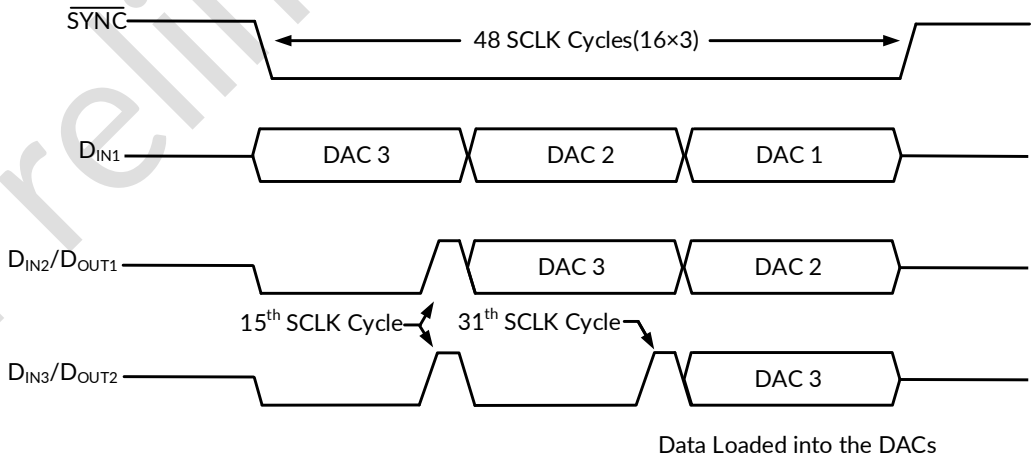


Figure 32. Daisy Chain Timing Diagram

9.3.6 DAC Input Data Update Mechanism

The RS1328 has two modes of operation, plus a few special command operations. The two modes of operation are Write Register Mode (WRM) and Write Through Mode (WTM). For the rest of this document, these modes will be referred to as WRM and WTM. The special command operations are separate from WRM and WTM because they can be called upon regardless of the current mode of operation. The mode of operation is controlled by the first four bits of the control register, DB15 through DB12. See Table 1 for a detailed summary.

Table 1. Write Register and Write Through Modes

DB[15:12]	DB[11:0]	Description of Mode
1000	XXXXXXXXXX	WRM: The registers of each DAC Channel can be written to without causing their outputs to change.
1001	XXXXXXXXXX	WTM: Writing data to a channel's register causes the DAC output to change.

When the RS1328 first powers up, the DAC is in WRM. In WRM, the registers of each individual DAC channel can be written to without updating the DAC outputs. This is accomplished by setting DB15 to 0, specifying the DAC register to be written to in DB[14:12], and entering the new DAC register setting in DB[11:0] (see Table 2). The RS1328 remains in WRM until the mode of operation is changed to WTM. The mode of operation is changed from WRM to WTM by setting DB[15:12] to 0x1001. Once in WTM, writing data to a DAC channel register causes the DAC output to be updated as well. Changing a DAC channel register in WTM is accomplished in the same manner as in WRM. However, in WTM the DAC register and output are updated at the completion of the command (see Table 2). Similarly, the RS1328 remains in WTM until the mode of operation is changed to WRM by setting DB[15:12] to 0x1000.

Table 2. Commands Impacted by WRM and WTM

DB15	DB[14:12]	DB[11:0]	Description of Mode
0	0 0 0	D11 D10 ... D1 D0	WRM: D[11:0] written to only the data register of ChA WTM: ChA's output is updated by data in D[11:0]
0	0 0 1	D11 D10 ... D1 D0	WRM: D[11:0] written to only the data register of ChB WTM: ChB's output is updated by data in D[11:0]
0	0 1 0	D11 D10 ... D1 D0	WRM: D[11:0] written to only the data register of ChC WTM: ChC's output is updated by data in D[11:0]
0	0 1 1	D11 D10 ... D1 D0	WRM: D[11:0] written to only the data register of ChD WTM: ChD's output is updated by data in D[11:0]
0	1 0 0	D11 D10 ... D1 D0	WRM: D[11:0] written to only the data register of ChE WTM: ChE's output is updated by data in D[11:0]
0	1 0 1	D11 D10 ... D1 D0	WRM: D[11:0] written to only the data register of ChF WTM: ChF's output is updated by data in D[11:0]
0	1 1 0	D11 D10 ... D1 D0	WRM: D[11:0] written to only the data register of ChG WTM: ChG's output is updated by data in D[11:0]
0	1 1 1	D11 D10 ... D1 D0	WRM: D[11:0] written to only the data register of ChH WTM: ChH's output is updated by data in D[11:0]

The special command operations can be exercised at any time regardless of the mode of operation. There are three special command operations. The first command is exercised by setting data bits DB[15:12] to 0x1010. This allows the user to update multiple DAC outputs simultaneously to the values currently loaded in their respective control registers. This command is valuable if the user wants each DAC output to be at a different output voltage, but still have all the DAC outputs changed to their appropriate values simultaneously (see Table 3).

The second special command allows the user to alter the DAC output of channel A with a single write frame. This command is exercised by setting data bits DB[15:12] to 0x1011 and data bits DB[11:0] to the desired control register value. This command also causes the DAC outputs of the other channels to update to their current control register values. The user may choose to exercise this command to save a write sequence. For example, the user may wish to update several DAC outputs simultaneously, including channel A. To accomplish

this task in the minimum number of write frames, the user would alter the control register values of all the DAC channels except channel A while operating in WRM. The last write frame would be used to exercise the special command Channel A Write Mode. In addition to updating the control register of channel A and output to a new value, all of the other channels would be updated as well. At the end of this sequence of write frames, the RS1328 would still be operating in WRM (see Table 3).

The third special command allows the user to set all the DAC control registers and outputs to the same level. This command is commonly referred to as "broadcast" mode, as the same data bits are being broadcast to all of the channels simultaneously. This command is exercised by setting data bits DB[15:12] to 0x1100 and data bits DB[11:0] to the value that the user wishes to broadcast to all the DAC control registers. Once the command is exercised, each DAC output is updated by the new control register value. This command is frequently used to set all the DAC outputs to some known voltage such as 0 V, $V_{REF}/2$, or Full Scale. A summary of the commands can be found in Table 3.

Table 3. Special Command Operations

DB[15:12]	DB[11:0]	Description of Mode
1010	X X X X H G F E D C B A	Update Select: The DAC outputs of the channels selected with a 1 in DB[7:0] are updated simultaneously to the values in their respective control registers.
1011	D11 D10 ... D1 D0	Channel A Write: The control register and DAC output of channel A are updated to the data in DB[11:0]. The outputs of the other seven channels are also updated according to their respective control register values.
1100	D11 D10 ... D1 D0	Broadcast: The data in DB[11:0] is written to all channel control registers and DAC output simultaneously.

9.3.7 Power-On Reset

The power-on reset circuit controls the output voltages of the eight DACs during power-up. Upon application of power, the DAC registers are filled with zeros and the output voltages are set to 0 V. The outputs remain at 0 V until a valid write sequence is made.

9.3.8 Transfer Characteristic

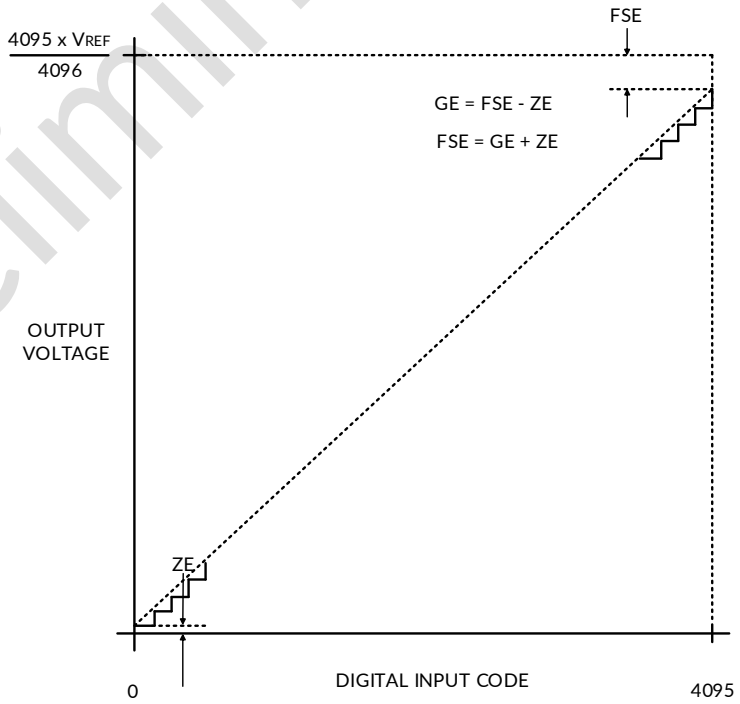


Figure 33. Input / Output Transfer Characteristic

9.4 Device Functional Modes

9.4.1 Power-Down Modes

The RS1328 has three power-down modes, where different output terminations can be selected (see Table 4). With all channels powered down, the supply current drops to 0.1 µA at 3 V and 0.2 µA at 5 V. By selecting the channels to be powered down in DB[7:0] with a 1, individual channels can be powered down separately, or multiple channels can be powered down simultaneously. The three different output terminations include high output impedance, 100 kΩ to ground, and 2.5 kΩ to ground.

The output amplifiers, resistor strings, and other linear circuitry are all shut down in any of the power-down modes. The bias generator, however, is only shut down if all the channels are placed in power-down mode. The contents of the DAC registers are unaffected when in power-down. Therefore, each DAC register maintains its value prior to the RS1328 being powered down unless it is changed during the write sequence that instructed it to recover from power down. Minimum power consumption is achieved in the power-down mode with $\overline{SYNC}$ idled high, D_{IN} idled low, and SCLK disabled. The time to exit power-down (Wake-Up Time) is typically 5 µsec at 3 V and 3 µsec at 5 V.

Table 4. Special Command Operations

DB[15:12]	DB[11:8]	7	6	5	4	3	2	1	0	Output Impedance
1101	XXXX	H	G	F	E	D	C	B	A	Hi-Z outputs
1110	XXXX	H	G	F	E	D	C	B	A	100 kΩ outputs
1111	XXXX	H	G	F	E	D	C	B	A	2.5 kΩ outputs

9.5 Programming

9.5.1 Programming the RS1328

This section presents the step-by-step instructions for programming the serial input register.

9.5.1.1 Updating DAC Outputs Simultaneously

When the RS1328 is first powered on, the DAC is operating in Write Register Mode (WRM). Operating in WRM allows the user to program the registers of multiple DAC channels without causing the DAC outputs to be updated. For example, below are the steps for setting Channel A to a full scale output, Channel B to three quarters full scale, Channel C to half-scale, Channel D to one-quarter full scale and having all the DAC outputs update simultaneously.

As stated previously, the RS1328 powers up in WRM. If the device was previously operating in Write Through Mode (WTM), an extra step to set the DAC into WRM is required. First, the DAC registers must be programmed to the desired values. To set Channel A to an output of full scale, write 0x0FFF to the control register.

This updates the data register for Channel A without updating the output of Channel A. Second, set Channel B to an output of three-quarters full scale by writing 0x1C00 to the control register. This updates the data register for Channel B. Once again, the output of Channel B and Channel A are not updated, because the DAC is operating in WRM. Third, set Channel C to half scale by writing 0x2800 to the control register. Fourth, set Channel D to one quarter full scale by writing 0x3400 to the control register. Finally, update all four DAC channels simultaneously by writing 0xA00F to the control register. This procedure allows the user to update four channels simultaneously with five steps.

Because Channel A was one of the DACs to be updated, one command step could have been saved by writing to Channel A last. Do this by writing to Channel B, C, and D first, and using the special command Channel A Write to update the DAC register and output of Channel A. This special command also updates all DAC outputs while updating Channel A. With this sequence of commands, the user can update four channels simultaneously using four steps. A summary of this command can be found in Table 3.

9.5.1.2 Updating DAC Outputs Independently

If the RS1328 is currently operating in WRM, change the mode of operation to WTM by writing 0x9XXX to the control register. Once the DAC is operating in WTM, any DAC channel can be updated in one step. For example, if a design required Channel G to be set to half scale, the user can write 0x6800 to the control register to update the data register and DAC output of Channel G. Similarly, write 0x5FFF to the control register to set the output of Channel F to full scale. Channel A is the only channel that has a special command that allows its DAC output to be updated in one command, regardless of the mode of operation. Write 0xBFFF to the control register to set the DAC output of Channel A to full scale in one step.

10 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RS component specification, and RS does not warrant its accuracy or completeness. RS's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Using References as Power Supplies

While the simplicity of the RS1328 implies ease of use, it is important to recognize that the path from the reference input ($V_{REF1,2}$) to the DAC outputs has a zero Power Supply Rejection Ratio (PSRR). Therefore, the user must provide a noise-free supply voltage to $V_{REF1,2}$. To utilize the full dynamic range of the RS1328, the supply pin (V_A) and $V_{REF1,2}$ can be connected together and share the same supply voltage. Because the RS1328 consumes very little power, a reference source can be used as the reference input or the supply voltage. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low-noise regulators can also be used. Listed below are a few reference and power supply options for the RS1328.

10.2 Application Information

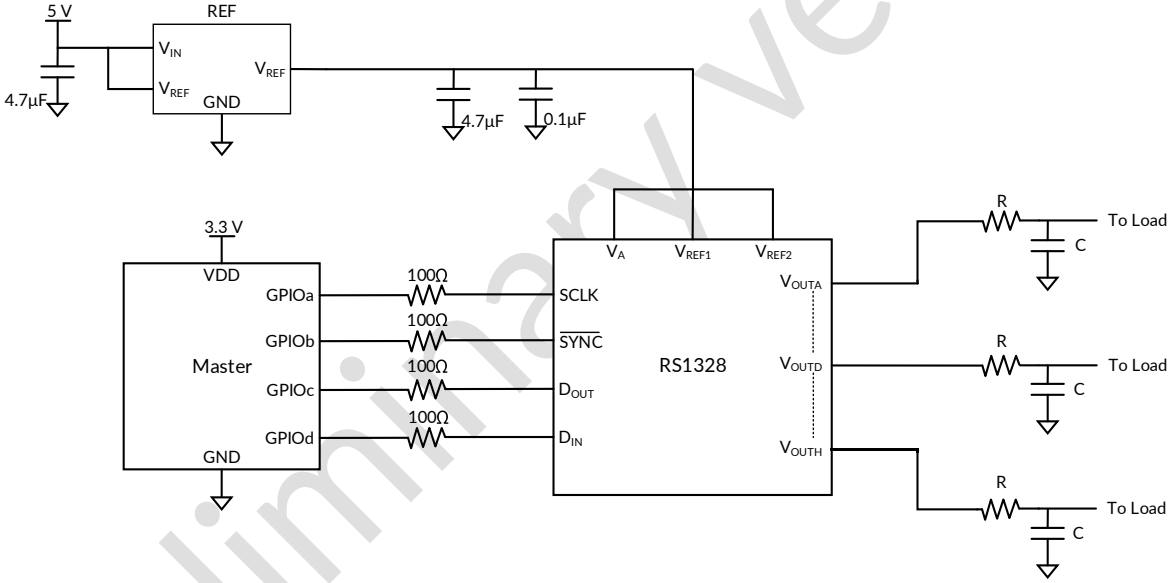


Figure 34. Typical Application Circuits

10.2.1 Design Requirements

There are two references for the RS1328. One reference input serves channels A through D, while the other reference serves channels E through H. The 16-bit input shift register of the RS1328 controls the mode of operation, the power-down condition, and the register/output value of the DAC channels. All eight DAC outputs can be updated simultaneously or individually.

10.2.2 Design Requirements

Each reference input pin can be set independently, or the reference pins can be shorted together as shown in Figure 34. Acceptable reference voltages are 0.5 V to V_A. Utilizing an RC filter on the output to roll off output noise is optional.

11 POWER SUPPLY RECOMMENDATIONS

For best performance, the RS1328 power supply should be bypassed with at least a 1 μF and a 0.1 μF capacitor. The 0.1 μF capacitor must be placed right at the device supply pin. The 1 μF or larger valued capacitor can be a tantalum capacitor, while the 0.1 μF capacitor must be a ceramic capacitor with low ESL and low ESR. If a ceramic capacitor with low ESL and low ESR is used for the 1 μF value and can be placed right at the supply pin, the 0.1 μF capacitor can be eliminated. Capacitors of this nature typically span the same frequency spectrum as the 0.1 μF capacitor, and thus eliminate the need for the extra capacitor. The power supply for the RS1328 should only be used for analog circuits.

Avoid the crossover of analog and digital signals. This helps minimize the amount of noise from the transitions of the digital signals from coupling onto the sensitive analog signals, such as the reference pins and the DAC outputs.

12 LAYOUT

12.1 Layout Guidelines

For best accuracy and minimum noise, the printed circuit board containing the RS1328 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located in the same board layer. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will utilize a "fencing" technique to prevent the mixing of analog and digital ground current. Separate ground planes should only be utilized when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the RS1328. Ensure that digital signals with fast edge rates do not pass over split ground planes. The signals must always have a continuous return path below their traces.

12.2 Layout Example

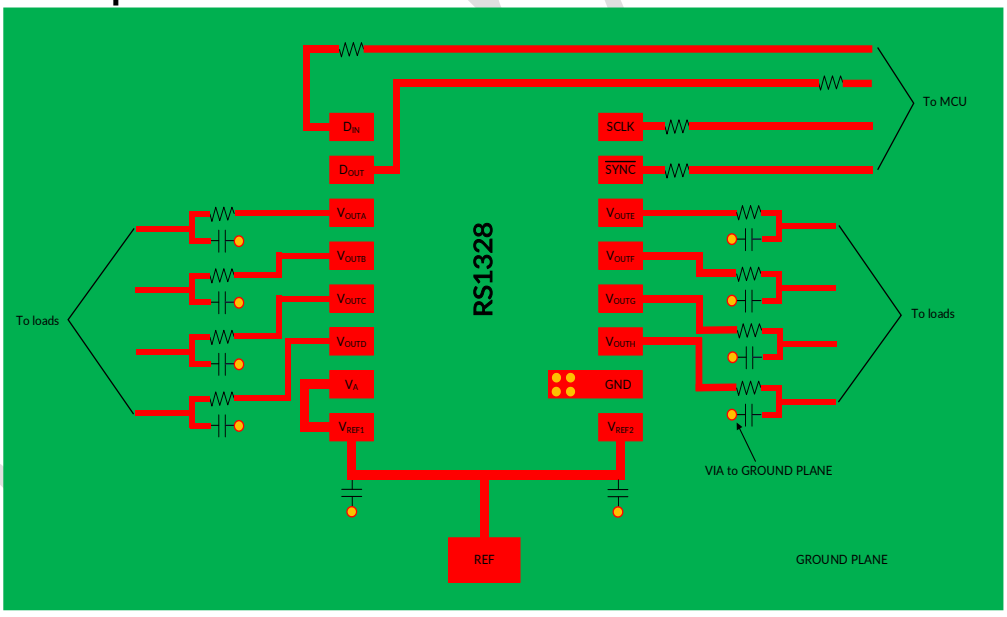
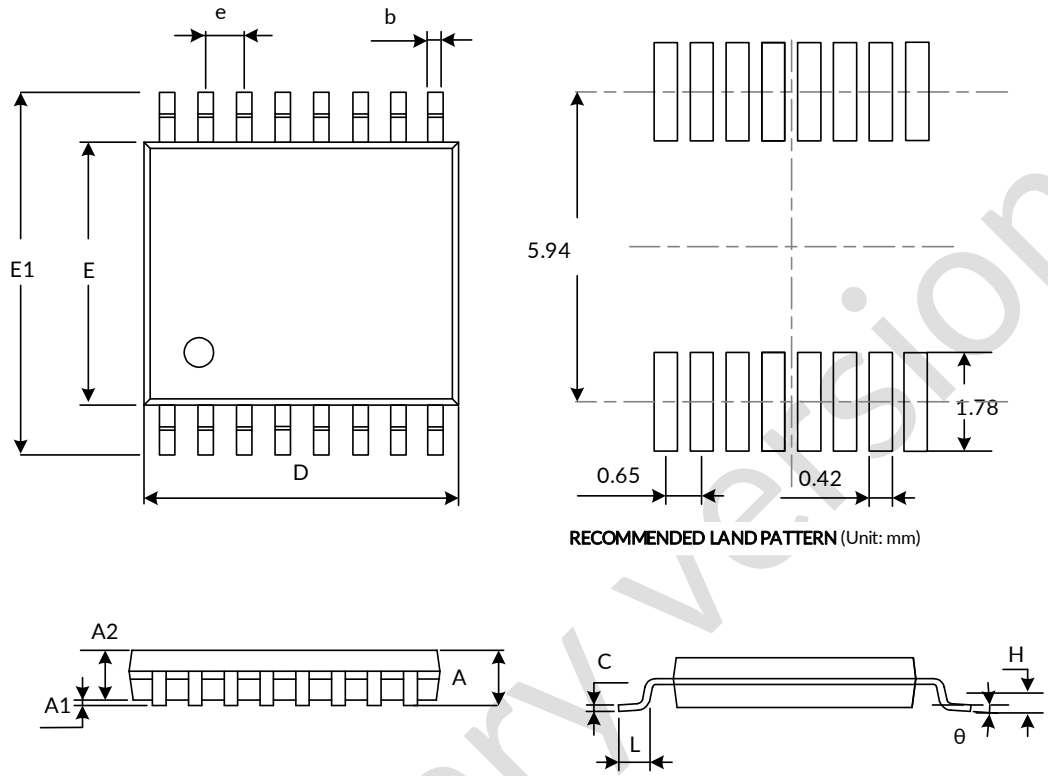


Figure 35. Layout Example

13 PACKAGE OUTLINE DIMENSIONS

TSSOP16 (3)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D (1)	4.860	5.100	0.191	0.201
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650 (BSC) (2)		0.026 (BSC) (2)	
L	0.500	0.700	0.020	0.028
H	0.250 TYP		0.010 TYP	
θ	1°	7°	1°	7°

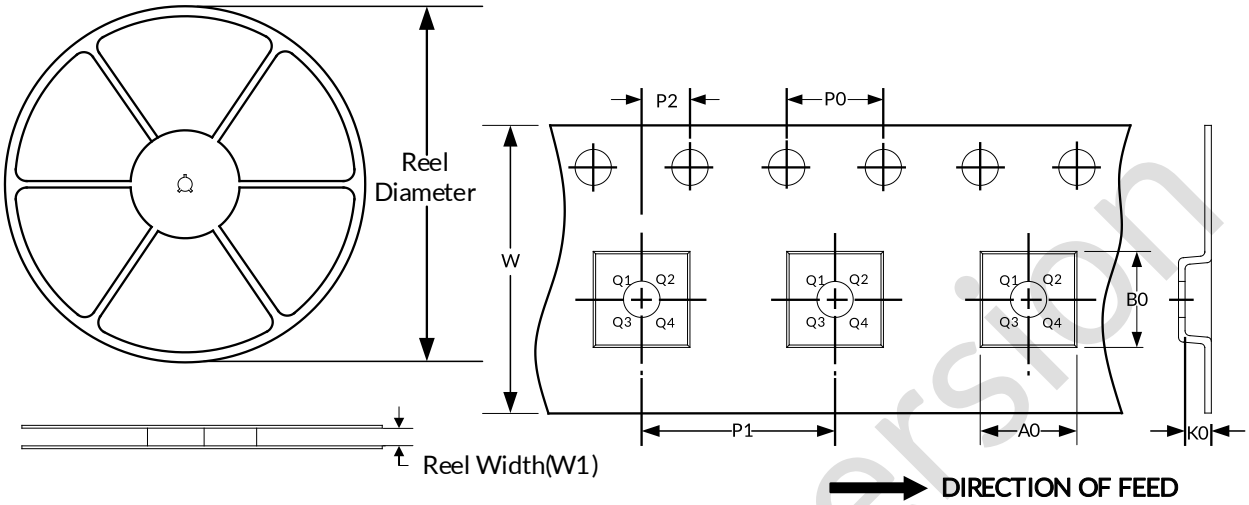
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP16	13"	12.4	6.90	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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