RS1324 12-Bit Micro Power Quad Digital-to-Analog Converter With Rail-to-Rail Output

1 FEATURES

- **Ensured Monotonicity**
- **Low Power Operation**
- **Rail-to-Rail Voltage Output**
- **Power-On Reset to 0 V**
- **Simultaneous Output Updating**
- **Wide Power Supply Range: 2.7 V to 5.5 V**
- **Industry's Smallest Package**
- **Power-Down Modes**
- **Resolution: 12 Bits**
- **INL: +1.2/-1.2 LSB (Typical)**
- **DNL: +0.3/-0.2 LSB (Typical)**
- **Setting Time: 2 µs (Typical)**
- **Zero Code Error: 4.3 mV (Typical)**
- **Full-Scale Error: ±0.01% FS (Typical)**
- **Supply Power:**
  - Normal: 1.13mW at 3V or 2.54mW at 5V (Typical)
  - Power Down: 0.03µW at 3V or 0.15µW at 5V (Typical)

2 APPLICATIONS

- **Battery-Powered Instruments**
- **Digital Gain and Offset Adjustment**
- **Programmable Voltage and Current Sources**
- **Programmable Attenuators**

3 DESCRIPTIONS

The RS1324 device is a full-featured, general-purpose, quad, 12-bit, voltage-output, digital-to-analog converter (DAC) that can operate from a single 2.7 V to 5.5 V supply and consumes 1.13 mW at 3 V or 2.54 mW at 5 V. The RS1324 is packaged in MSOP10 package.

The on-chip output amplifier allows rail-to-rail output swing and the three-wire serial interface operates at clock rates up to 40 MHz over the entire supply voltage range. The serial interface is compatible with standard SPI, QSPI, MICROWIRE, and DSP interfaces.

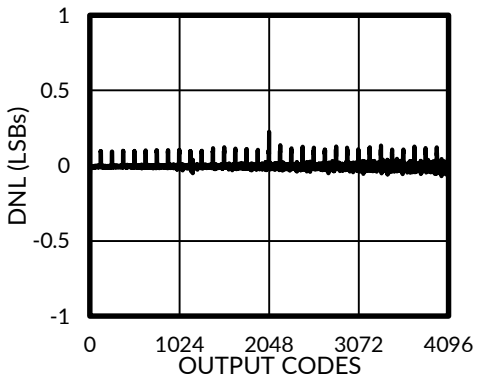
The reference for the RS1324 serves all four channels and can vary in voltage between 1 V and V_A, providing the widest possible output dynamic range. The RS1324 has a 16-bit input shift register that controls the outputs to be updated, the mode of operation, the power-down condition, and the binary input data. All four outputs can be updated simultaneously or individually depending on the setting of the two mode of operation bits.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1324	MSOP10	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DNL at V_A = 3 V



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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2025/01/02	Preliminary version completed
A.0.1	2025/08/21	1. Update Electrical Characteristics and Typical Characteristics 2. Add Thermal Information 3. Add Application Curve and Layout Example

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS1324	RS1324XN	-40°C ~125°C	MSOP10	RS1324	MSL1	Tape and Reel, 4000

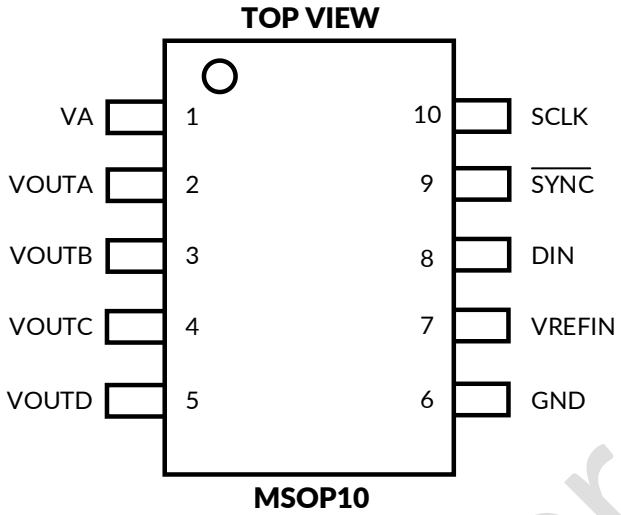
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 PIN CONFIGURATION AND FUNCTIONS



PIN DESCRIPTION

NAME	SOT	TYPE (1)	DESCRIPTION
V_A	1	S	Power supply input. Must be decoupled to GND.
V_{OUTA}	2	O	Channel A analog output voltage.
V_{OUTB}	3	O	Channel B analog output voltage.
V_{OUTC}	4	O	Channel C analog output voltage.
V_{OUTD}	5	O	Channel D analog output voltage.
GND	6	G	Ground reference for all on-chip circuitry.
V_{REFIN}	7	I	Unbuffered reference voltage shared by all channels. Must be decoupled to GND.
D_{IN}	8	I	Serial data input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
$\overline{SYNC}$	9	I	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data is transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{SYNC}$ is brought high before the 16th clock, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
SCLK	10	I	Serial clock input. Data is clocked into the input shift register on the falling edges of this pin.

(1) G = Ground, I = Input, O = Output, and S = Supply.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

	MIN	MAX	UNIT
Supply voltage, V_A		6.5	V
Voltage on any input pin	-0.3	6.5	V
Input current at any pin (3)		10	mA
Package input current (3)		20	mA
Power consumption at T_A = 25°C	See (4)		
Junction temperature, T_J (4)		150	°C
Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.

(3) When the input voltage at any pin exceeds 5.5 V or is less than GND, the current at that pin must be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.

(4) The absolute maximum junction temperature (T_{Jmax}) for this device is 150°C. The maximum allowable power dissipation is dictated by T_{Jmax}, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_{DMAX} = (T_{Jmax} - T_A) / \theta_{JA}$. The values for maximum power dissipation is reached only when the device is operated in a severe fault condition (that is, when input or output pins are driven beyond the operating ratings, or the power supply polarity is reversed).

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-Device Model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

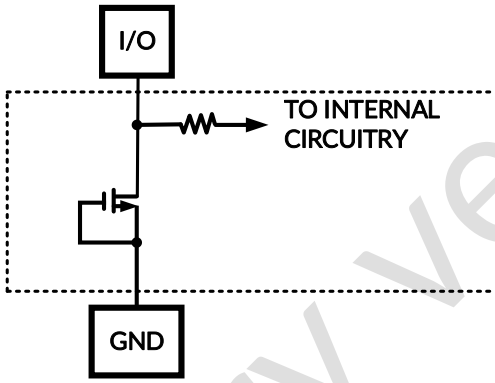
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_A	Supply Voltage	2.7	5.5	V
V_{REFIN}	Reference Voltage	1	V_A	V
	Digital Input Voltage (2)	0	5.5	V
	Output Load	0	1500	pF
	SCLK Frequency		40	MHz
T_A	Operating Temperature	–40	125	°C

(1) All voltages are measured with respect to GND = 0V, unless otherwise specified.
(2) The inputs are protected as shown below. Input voltage magnitudes up to 5.5V, regardless of V_A, do not cause errors in the conversion result. For example, if V_A is 3V, the digital input pins can be driven with a 5V logic device.



7.4 Thermal Information

THERMAL METRIC (1) (2)		RS1324XN MSOP10 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	240	°C/W
$R_{\theta JC\ (top)}$	Junction-to-case (top) thermal resistance	53.3	°C/W
$R_{\theta JB}$	Junction-to-ambient thermal resistance	78.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.6	°C/W
$R_{\theta JC\ (bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Reflow temperature profiles are different for lead-free packages.

7.5 Electrical Characteristics

T_A = 25°C, V_A = 2.7 V to 5.5 V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, and input code range 48 to 4047 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
STATIC PERFORMANCE							
	Resolution	–40°C ≤ T_A ≤ 125°C		12			Bits
	Monotonicity	–40°C ≤ T_A ≤ 125°C		12			Bits
INL	Integral Non-Linearity	T_A = 25°C		-3.1	+1.2/-1.2	2.3	LSB
		–40°C ≤ T_A ≤ 125°C			+2/-1.3		LSB
DNL	Differential Non-Linearity	V_A = 2.7 V to 4.5 V	T_A = 25°C	-0.5	+0.3/-0.2	0.7	LSB
			–40°C ≤ T_A ≤ 125°C		+0.35/-0.2		
		V_A = 4.5 V to 5.5 V	T_A = 25°C		+0.15/-0.1		LSB
			–40°C ≤ T_A ≤ 125°C		+0.2/-0.2		
ZE	Zero Code Error	I_{OUT} = 0 mA	T_A = 25°C		4.3		mV
			–40°C ≤ T_A ≤ 125°C		4.7		
			T_A = 25°C, V_A = 2.7 V			4.7	
FSE	Full-Scale Error	I_{OUT} = 0 mA	T_A = 25°C		-0.01	±0.1	%FSR
			–40°C ≤ T_A ≤ 125°C		-0.04		
GE	Gain Error	All ones Loaded to DAC register	T_A = 25°C		-0.1	±0.25	%FSR
			–40°C ≤ T_A ≤ 125°C		-0.2		
ZCED	Zero Code Error Drift				8		µV/°C
TC GE	Gain Error Tempco	V_A = 3 V			-0.3		ppm FSR/°C
		V_A = 5 V			-0.2		
OUTPUT CHARACTERISTICS (V_{OUT})							
	Output Voltage Range (2)	–40°C ≤ T_A ≤ 125°C		0		V_{REFIN}	V
I_{OZ}	High-Impedance Output Leakage Current (2)	–40°C ≤ T_A ≤ 125°C			+1		µA
ZCO	Zero Code Output	V_A = 2.7 V, I_{OUT} = 200 µA			9	11	mV
		V_A = 2.7 V, I_{OUT} = 1 mA			38	45	
		V_A = 5.5 V, I_{OUT} = 200 µA			5	7	
		V_A = 5.5 V, I_{OUT} = 1 mA			21	23	
FSO	Full Scale Output	V_A = 2.7 V, I_{OUT} = 200 µA		2.686	2.687		V
		V_A = 2.7 V, I_{OUT} = 1 mA		2.638	2.642		
		V_A = 5.5 V, I_{OUT} = 200 µA		5.492	5.493		
		V_A = 5.5 V, I_{OUT} = 1 mA		5.466	5.468		
I_{OS}	Output Short-Circuit Current (Source)	V_A = 3 V, V_{OUT} = 0 V, Input Code = FFFh			-38		mA
		V_A = 5 V, V_{OUT} = 0 V, Input Code = FFFh			-40		
I_{OS}	Output Short-Circuit Current (Sink)	V_A = 3 V, V_{OUT} = 3 V, Input Code = 000h.			60		mA
		V_A = 5 V, V_{OUT} = 5 V, Input Code = 000h.			62		
I_O	Continuous Output Current	Available on each DAC output, –40°C ≤ T_A ≤ 125°C				10	mA
C_L	Maximum Load Capacitance	R_L = ∞			1500		pF
		R_L = 2 kΩ			1500		
Z_{OUT}	DC Output Impedance	V_A = 2.7V, Input Code = 7FFh			0.42		Ω
		V_A = 5.5V, Input Code = 7FFh			0.35		

Electrical Characteristics (continued)

T_A = 25°C, V_A = 2.7 V to 5.5 V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, and input code range 48 to 4047 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
REFERENCE INPUT CHARACTERISTICS							
V_{REFIN}(3)	Input Range Minimum	T_A = 25°C			0.2		V
		–40°C ≤ T_A ≤ 125°C		1			
	Input Range Maximum	–40°C ≤ T_A ≤ 125°C				V_A	V
	Input Impedance				30		kΩ
LOGIC INPUT CHARACTERISTICS							
I_{IN}	Input Current	–40°C ≤ T_A ≤ 125°C			+1		µA
V_{IL}	Input Low Voltage	V_A = 3 V	T_A = 25°C		0.7		V
			–40°C ≤ T_A ≤ 125°C			0.6	
		V_A = 5 V	T_A = 25°C		1.3		V
			–40°C ≤ T_A ≤ 125°C			0.8	
V_{IH}	Input High Voltage	V_A = 3 V	T_A = 25°C		1.4		V
			–40°C ≤ T_A ≤ 125°C	2.1			
		V_A = 5 V	T_A = 25°C		2.1		V
			–40°C ≤ T_A ≤ 125°C	2.4			
C_{IN}	Input Capacitance	–40°C ≤ T_A ≤ 125°C			3		pF
POWER REQUIREMENTS							
V_A (3)	Supply Voltage Minimum	–40°C ≤ T_A ≤ 125°C		2.7			V
	Supply Voltage Maximum	–40°C ≤ T_A ≤ 125°C				5.5	V
I_N(4)	Normal Supply Current	f_{SCLK} = 30 MHz, output unloaded, V_A = 2.7 V to 3.6 V	T_A = 25°C		376		µA
			–40°C ≤ T_A ≤ 125°C		438		
		f_{SCLK} = 30 MHz, output unloaded, V_A = 4.5 V to 5.5 V	T_A = 25°C		508		µA
			–40°C ≤ T_A ≤ 125°C		586		
		f_{SCLK} = 0 MHz, output unloaded,	V_A = 2.7 V		233	257	µA
			V_A = 5.5 V		273	306	
I_{PD}	Power-Down Supply Current	All PD modes, output unloaded, $\overline{SYNC}$ = DIN = 0 V after PD mode loaded, V_A = 2.7 V to 3.6 V	T_A = 25°C		0.01	0.06	µA
			–40°C ≤ T_A ≤ 125°C		1		µA
		All PD modes, output unloaded, $\overline{SYNC}$ = DIN = 0 V after PD mode loaded, V_A = 4.5 V to 5.5 V	T_A = 25°C		0.03	0.08	µA
			–40°C ≤ T_A ≤ 125°C		2		µA
P_N (4)	Normal Supply Power	f_{SCLK} = 30 MHz, output unloaded, V_A = 2.7 V to 3.6 V	T_A = 25°C		1.13		mW
			–40°C ≤ T_A ≤ 125°C		1.58		
		f_{SCLK} = 30 MHz, output unloaded, V_A = 4.5 V to 5.5 V	T_A = 25°C		2.54		mW
			–40°C ≤ T_A ≤ 125°C		3.22		
		f_{SCLK} = 0 MHz, output unloaded	V_A = 2.7 V to 3.6 V		0.61	0.71	mW
			V_A = 4.5 V to 5.5 V		1.50	1.73	

Electrical Characteristics (continued)

T_A = 25°C, V_A = 2.7 V to 5.5 V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, and input code range 48 to 4047 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
P_{PD}	Power-Down Supply Power	All PD modes, output unloaded, $\overline{SYNC}$ = DIN = 0 V after PD mode loaded	V_A = 2.7 V to 3.6 V		0.03	0.17	µW
			V_A = 4.5 V to 5.5 V		0.15	0.44	µW

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(2) This parameter is ensured by design and/or characterization and is not tested in production.
(3) To ensure accuracy, it is required that V_A and V_{REFIN} be well bypassed.
(4) This parameter varies with the frequencies of SCLK and SYNC, and it is measured under the conditions of f_{SCLK} = 30MHz and $f_{\overline{SYNC}}$ = 588KHz.

7.6 AC and Timing Characteristics

T_A = 25°C, V_A = 2.7 V to 5.5 V, V_{REFIN} = V_A, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, and input code range 48 to 4047 (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
f_{SCLK}	SCLK Frequency	T_A = 25°C			40		MHz
		–40°C ≤ T_A ≤ 125°C			30		
t_s	Output Voltage Settling Time (2)	400h to C00h code change RL = 2 kΩ, CL = 200pF	T_A = 25°C		2		µs
			–40°C ≤T_A ≤ 125°C		3		
SR	Output Slew Rate				1		V/µs
	Glitch Impulse	Code change from 800h to 7FFh			25		nV-sec
	Digital Feedthrough				0.5		nV-sec
	Digital Crosstalk				1		nV-sec
	DAC-to-DAC Crosstalk				3		nV-sec
	Multiplying Bandwidth	V_{REF} = 2.5 V ± 0.1 Vpp			450		kHz
	Total Harmonic Distortion	V_{REFIN} = 2.5 V ± 0.1 Vpp Input frequency = 10 kHz			90		dB
t_{WU}	Wake-Up Time	V_A = V_{REF} = 3 V			4		µs
		V_A = V_{REF} = 5 V			8		
$1/f_{SCLK}$	SCLK Cycle Time	T_A = 25°C			33		ns
		–40°C ≤ T_A ≤ 125°C			33		
t_{CH}	SCLK High Time	T_A = 25°C			7		ns
		–40°C ≤ T_A ≤ 125°C		10			
t_{CL}	SCLK Low Time	T_A = 25°C			7		ns
		–40°C ≤ T_A ≤ 125°C		10			
t_{SS}	$\overline{SYNC}$ Set-Up Time Prior to SCLK Falling Edge	T_A = 25°C			7		ns
		–40°C ≤ T_A ≤ 125°C		10			
t_{DS}	Data Set-Up Time Prior to SCLK Falling Edge	T_A = 25°C			4		ns
		–40°C ≤ T_A ≤ 125°C		5			
t_{DH}	Data Hold Time After SCLK Falling Edge	T_A = 25°C			4		ns
		–40°C ≤ T_A ≤ 125°C		5			
t_{CFSR}	SCLK Fall Prior to Rise of $\overline{SYNC}$	T_A = 25°C			3		ns
		–40°C ≤ T_A ≤ 125°C		4			
$t_{\overline{SYNC}}$	$\overline{SYNC}$ High Time	T_A = 25°C			9		ns
		–40°C ≤ T_A ≤ 125°C		10			

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are ensured to AOQL (Average Outgoing Quality Level).
(2) This parameter is ensured by design and/or characterization and is not tested in production.

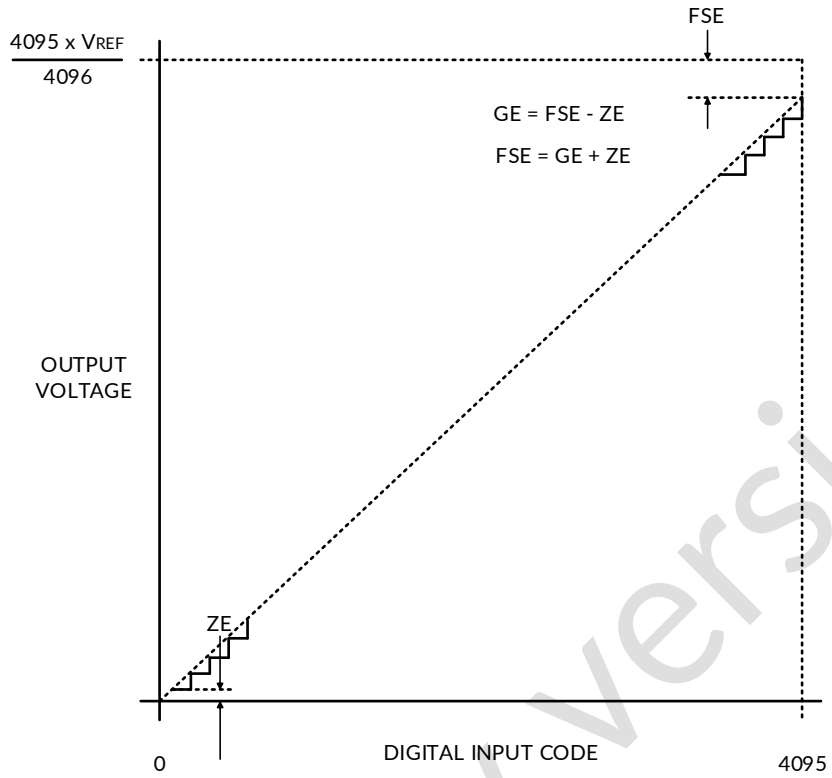


Figure 1. Input / Output Transfer Characteristic

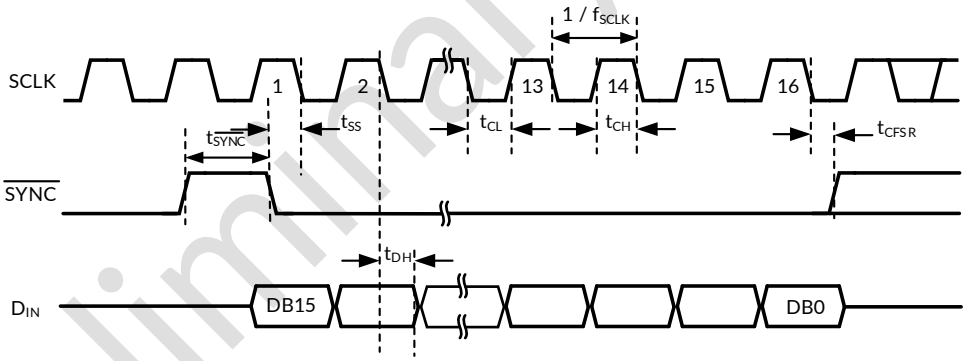


Figure 2. Serial Timing Diagram

7.7 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{REF} = V_A, f_{SCLK} = 30 MHz, and input code range 48 to 4047 (unless otherwise noted)

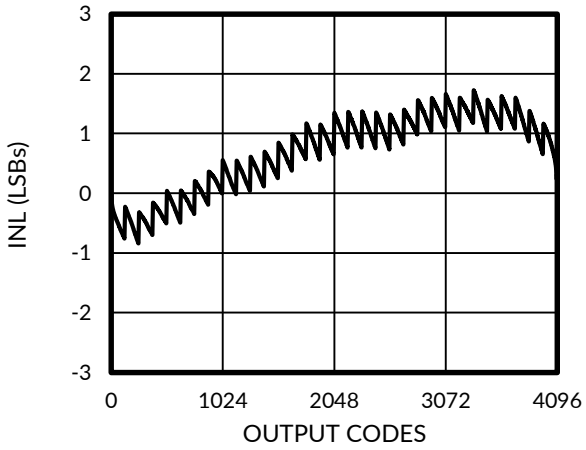


Figure 3. INL at V_A = 3 V

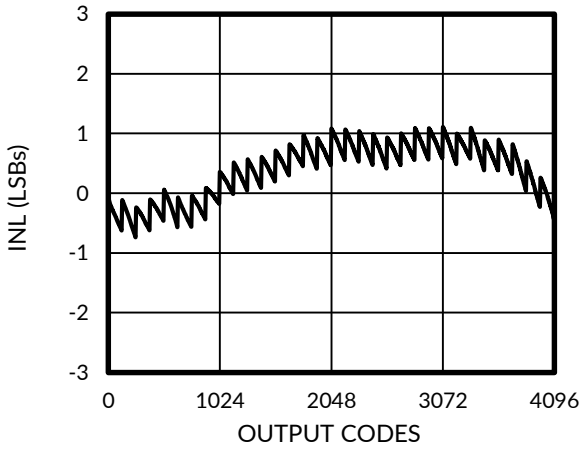


Figure 4. INL at V_A = 5 V

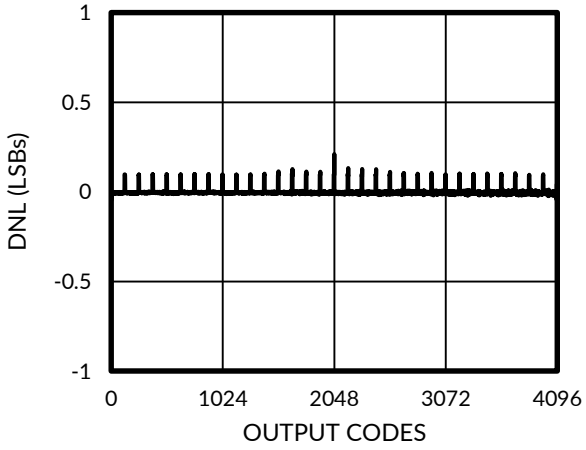


Figure 5. DNL at V_A = 3 V

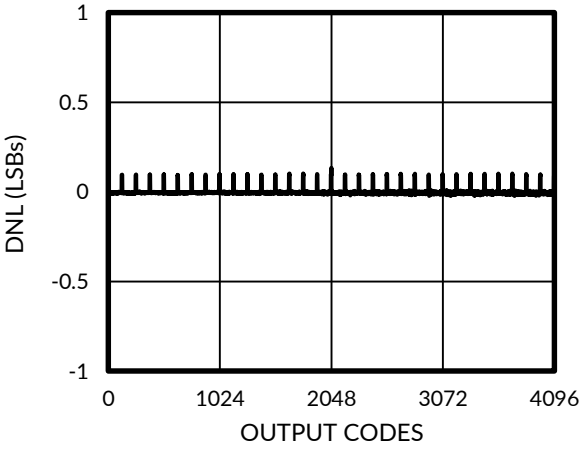


Figure 6. DNL at V_A = 5 V

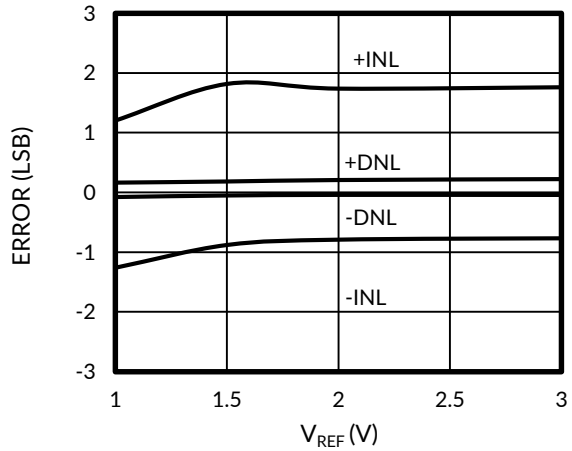


Figure 7. INL/DNL vs V_{REFIN} at V_A = 3 V

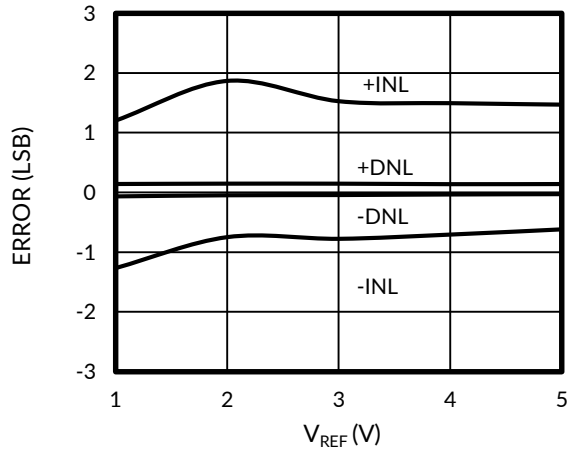


Figure 8. INL/DNL vs V_{REFIN} at V_A = 5 V

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{REF} = V_A, f_{SCLK} = 30 MHz, and input code range 48 to 4047 (unless otherwise noted)

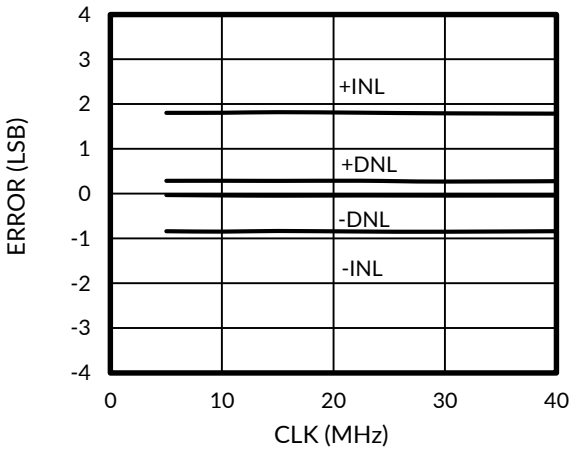


Figure 9. INL/DNL vs f_{SCLK} at V_A = 2.7 V

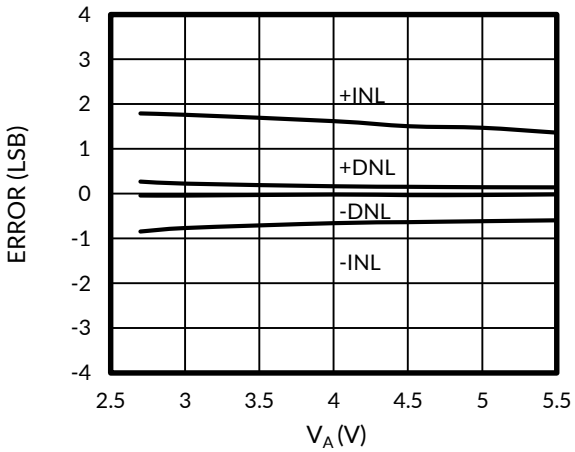


Figure 10. INL/DNL vs V_A

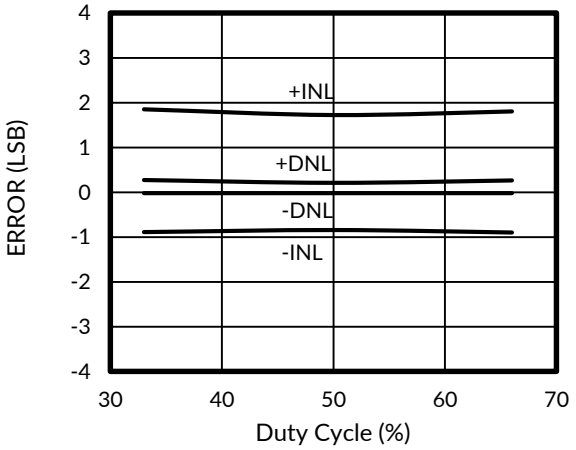


Figure 11. INL/DNL vs Clock Duty Cycle at V_A = 3 V

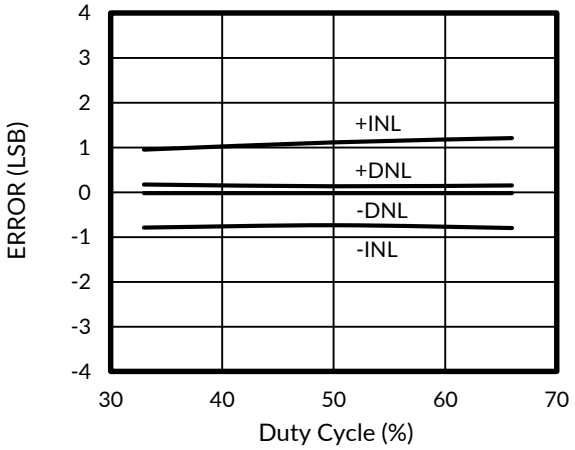


Figure 12. INL/DNL vs Clock Duty Cycle at V_A = 5 V

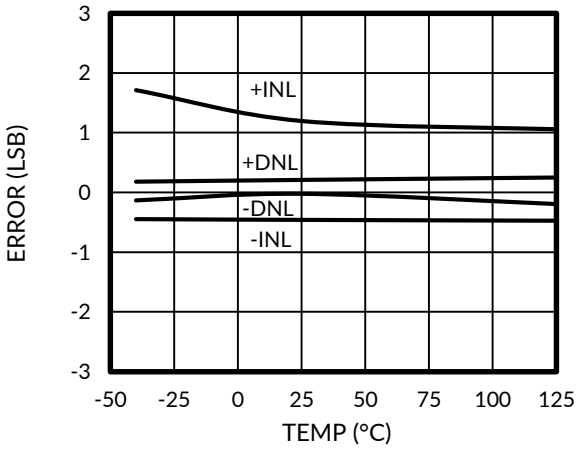


Figure 13. INL/DNL vs Temperature at V_A = 3 V

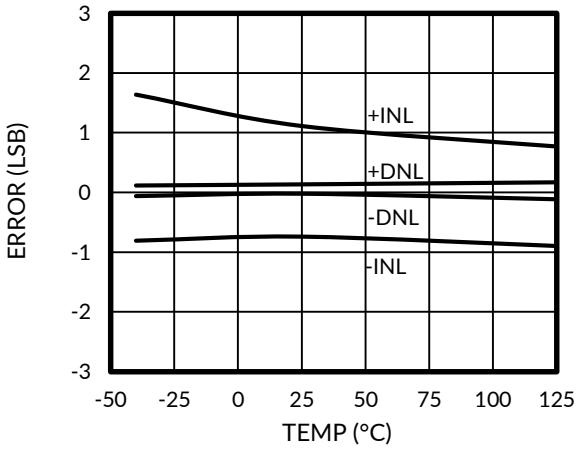


Figure 14. INL/DNL vs Temperature at V_A = 5 V

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{REF} = V_A, f_{SCLK} = 30 MHz, and input code range 48 to 4047 (unless otherwise noted)

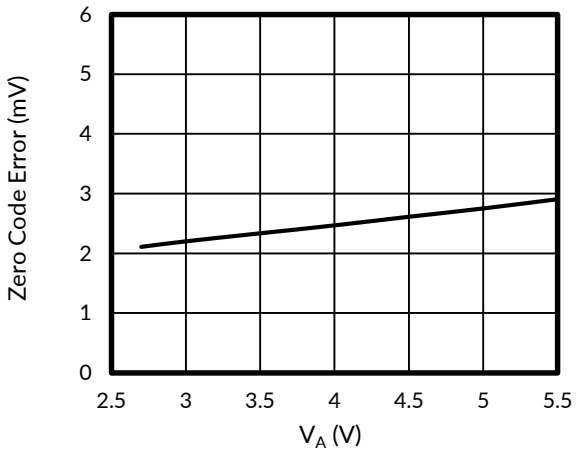


Figure 15. Zero Code Error vs V_A

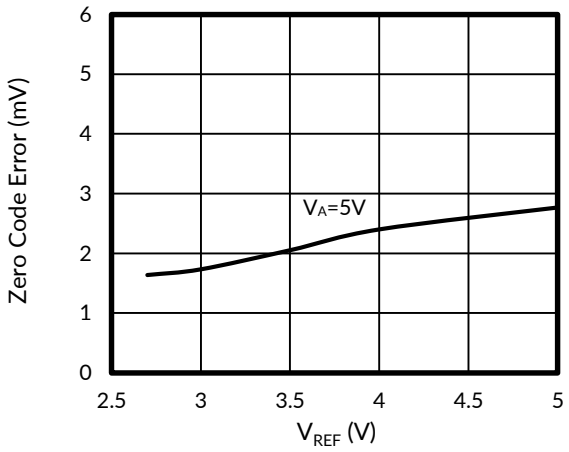


Figure 16. Zero Code Error vs V_{REFIN}

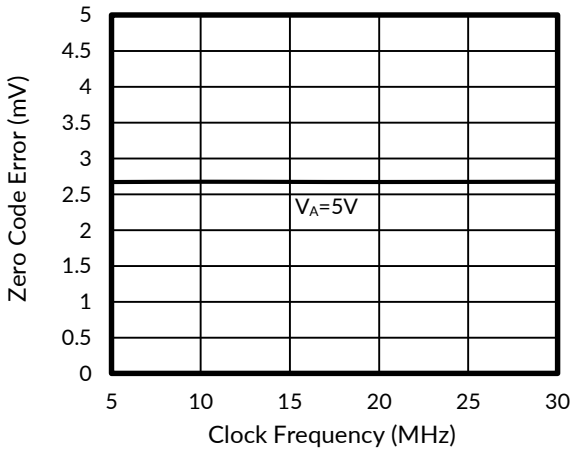


Figure 17. Zero Code Error vs f_{SCLK}

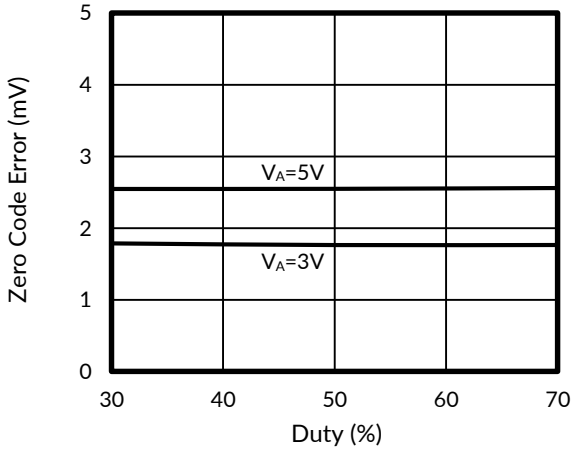


Figure 18. Zero Code Error vs Clock Duty Cycle

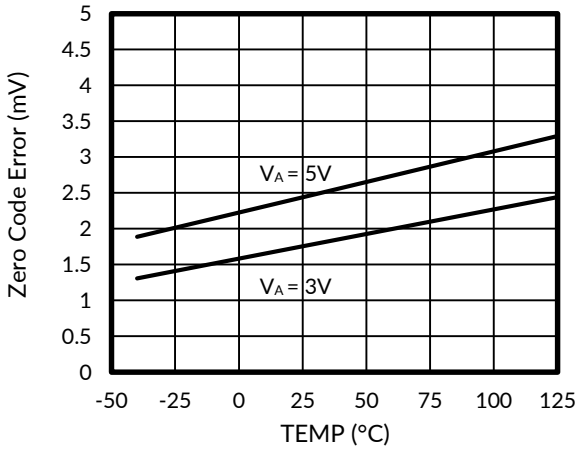


Figure 19. Zero Code Error vs Temperature

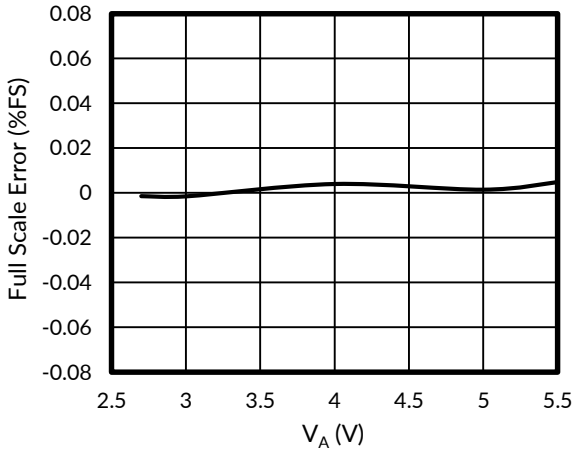


Figure 20. Full-Scale Error vs V_A

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{REF} = V_A, f_{SCLK} = 30 MHz, and input code range 48 to 4047 (unless otherwise noted)

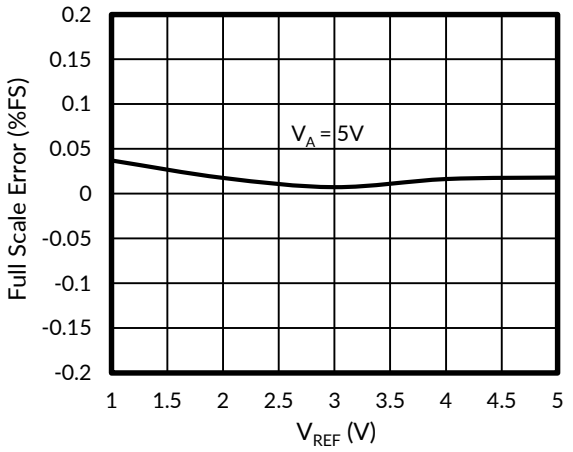


Figure 21. Full-Scale Error vs V_{REFIN}

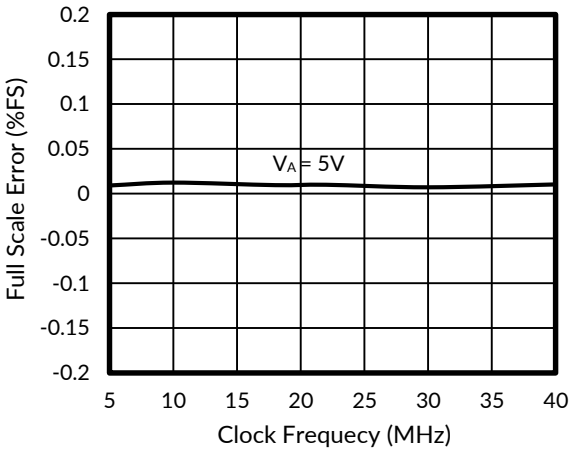


Figure 22. Full-Scale Error vs f_{SCLK}

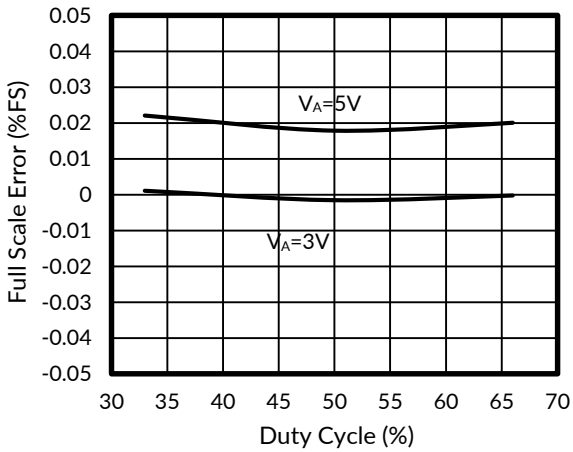


Figure 23. Full-Scale Error vs Clock Duty Cycle

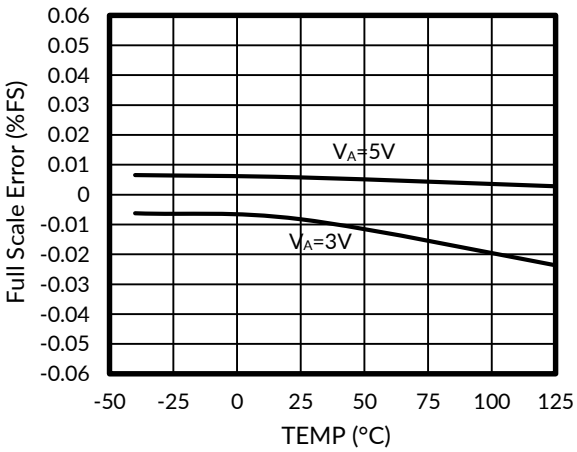


Figure 24. Full-Scale Error vs Temperature

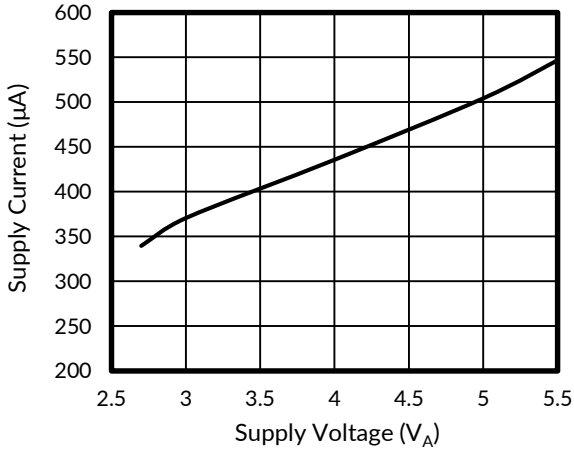


Figure 25. Supply Current vs V_A

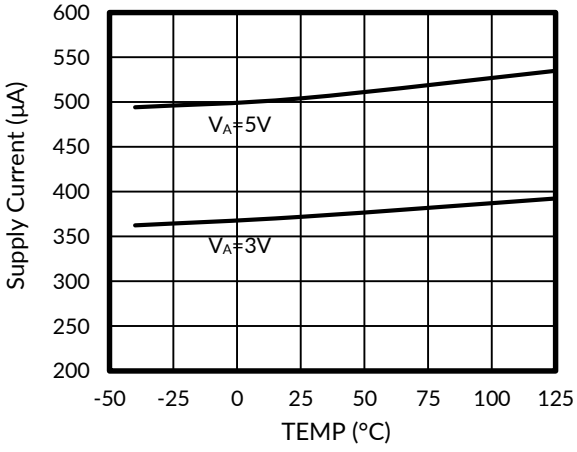


Figure 26. Supply Current vs Temperature

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

T_A = 25°C, V_{REF} = V_A, f_{SCLK} = 30 MHz, and input code range 48 to 4047 (unless otherwise noted)

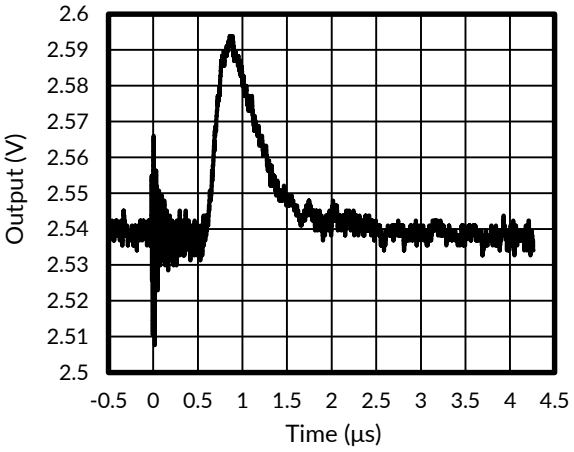


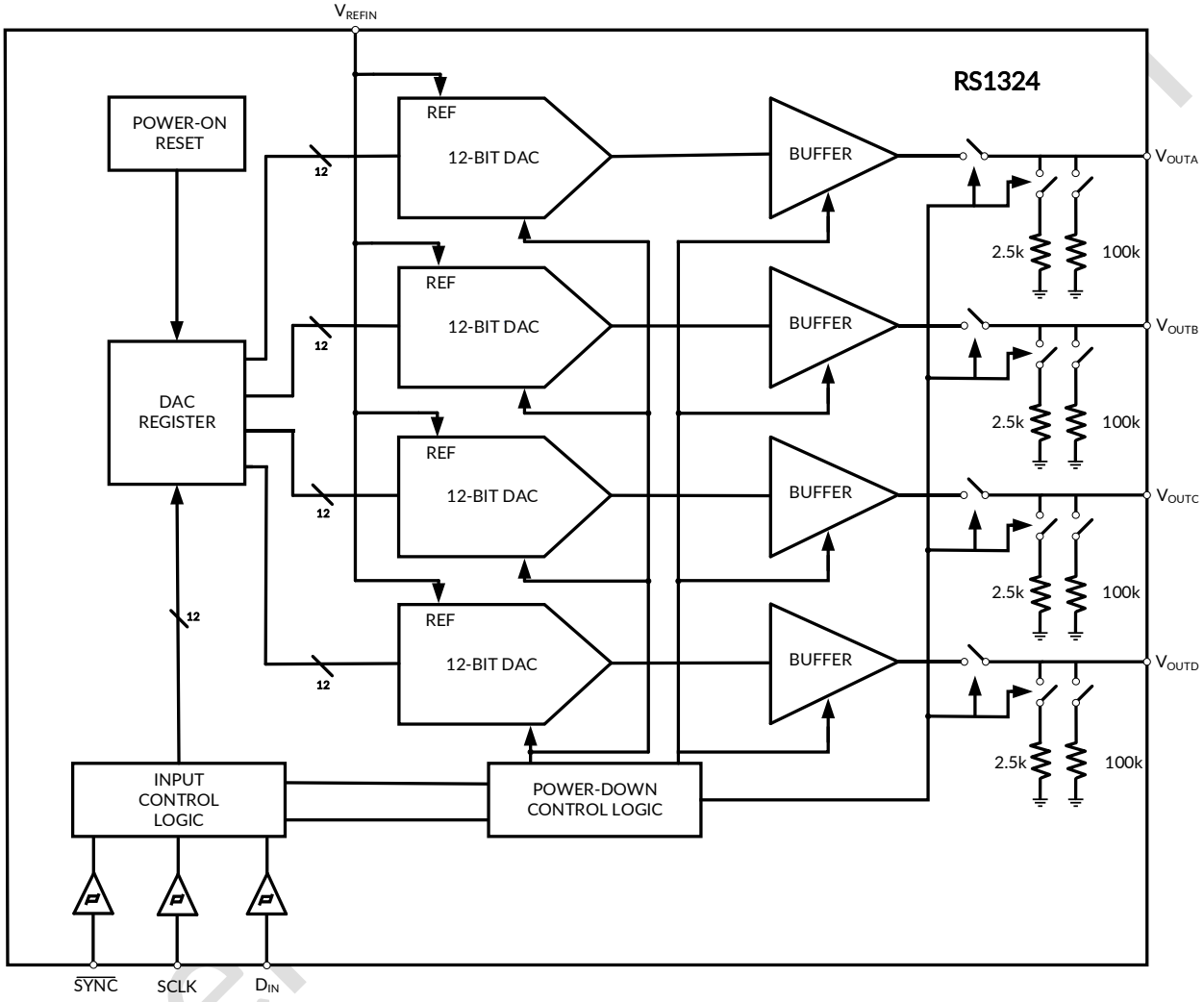
Figure 27. 5V Glitch Response

8 DETAILED DESCRIPTION

8.1 Overview

The RS1324 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Section

For simplicity, a single resistor string is shown in Figure 28. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage of:

$$V_{OUTA,B,C,D} = V_{REFIN} \times (D / 4096) \quad (1)$$

where

- D is the decimal equivalent of the binary code that is loaded into the DAC register

D can take on any integer value from 0 to 4095. This configuration ensures that the DAC is monotonic.

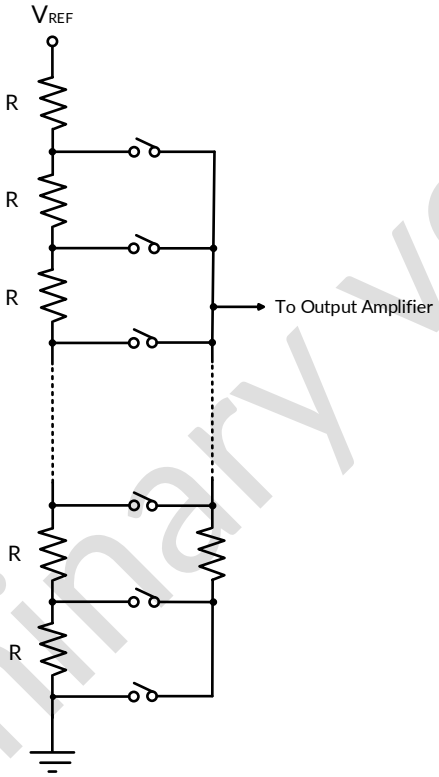


Figure 28. DAC Resistor String

8.3.2 Output Amplifier

The output amplifier is rail-to-rail, providing an output voltage range of 0V to V_A when the reference is V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_A, there is only a loss in linearity in the lowest codes. The output capabilities of the amplifier are described in the Electrical Characteristics.

The output amplifiers are capable of driving a load of 2kΩ in parallel with 1500pF to ground or to V_A. The zero-code and full-scale outputs for given load currents are available in the Electrical Characteristics.

8.3.3 Reference Voltage

The RS1324 uses a single external reference that is shared by all four channels. The reference pin, V_{REFIN}, is not buffered and has an input impedance of 30 kΩ. RS recommends driving the V_{REFIN} by a voltage source with low-output impedance. The reference voltage range is 1 V to V_A, providing the widest possible output dynamic range.

Feature Description (continued)

8.3.4 Power-On Reset

The power-on reset circuit controls the output voltages of the four DACs during power-up. Upon application of power, the DAC registers are filled with zeros and the output voltages are 0 V. The outputs remain at 0 V until a valid write sequence is made to the DAC.

8.4 Device Functional Modes

8.4.1 Power-Down Modes

The RS1324 has four power-down modes, two of which are identical. In power-down mode, the supply current drops to 0.06 μA at 3 V and 0.08 μA at 5 V at 25°C. The RS1324 is set in power-down mode by setting OP1 and OP0 to 11. Because this mode powers down all four DACs, the address bits, A1 and A0, are used to select different output terminations for the DAC outputs. Setting A1 and A0 to 00 or 11 causes the outputs to be tri-stated (a high impedance state). While setting A1 and A0 to 01 or 10 causes the outputs to be terminated by 2.5kΩ or 100 kΩ to ground respectively (see Table 1).

Table 1. Power-Down Modes

A1	A0	OP1	OP0	OPERATING MODE
0	0	1	1	High-Z outputs
0	1	1	1	2.5 kΩ to GND
1	0	1	1	100 kΩ to GND
1	1	1	1	High-Z outputs

The bias generator, output amplifiers, resistor strings, and other linear circuitry are all shut down in any of the power-down modes. However, the contents of the DAC registers are unaffected when in power down. Each DAC register maintains its value prior to the RS1324 being powered down unless it is changed during the write sequence which instructed it to recover from power down. Minimum power consumption is achieved in the power-down mode with $\overline{SYNC}$ and DIN idled low and SCLK disabled. The time to exit power down (Wake-Up Time) is typically t_{WU}, which is stated in Timing Requirements.

8.5 Programming

8.5.1 Serial Interface

The three-wire interface is compatible with SPI, QSPI, and MICROWIRE, as well as most DSPs and operates at clock rates up to 40 MHz. See Timing Requirements for information on a write sequence.

A write sequence begins by bringing the $\overline{SYNC}$ line low. Once $\overline{SYNC}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. To avoid misclocking data into the shift register, it is critical that $\overline{SYNC}$ not be brought low simultaneously with a falling edge of SCLK (see Figure 2). On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the DAC channel address, mode of operation, or register contents) is executed. At this point the $\overline{SYNC}$ line may be kept low or brought high. Any data and clock pulses after the 16th falling clock edge are ignored. In either case, $\overline{SYNC}$ must be brought high for the minimum specified time before the next write sequence is initiated with a falling edge of $\overline{SYNC}$.

Because the $\overline{SYNC}$ and D_{IN} buffers draw more current when they are high, they must be idled low between write sequences to minimize power consumption.

8.5.2 Input Shift Register

The input shift register, Figure 29, has sixteen bits. The first two bits are address bits. They determine whether the register data is for DAC A, DAC B, DAC C, or DAC D. The address bits are followed by two bits that determine the mode of operation (writing to a DAC register without updating the outputs of all four DACs, writing to a DAC register and updating the outputs of all four DACs, writing to the register of all four DACs and updating their outputs, or powering down all four outputs). The final twelve bits of the shift register are the data bits. The

Programming (continued)

data format is straight binary (MSB first, LSB last), with all 0s corresponding to an output of 0 V and all 1s corresponding to a full-scale output of V_{REFIN} − 1 LSB. The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of SCLK.

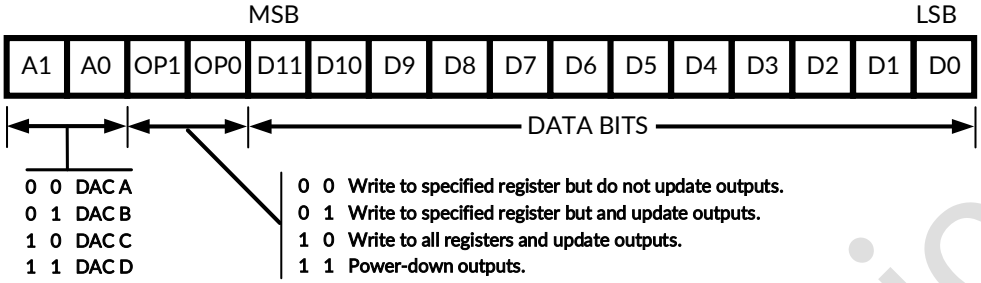


Figure 29. Input Register Contents

Normally, the $\overline{SYNC}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th SCLK falling edge. However, if $\overline{SYNC}$ is brought high before the 16th falling edge, the data transfer to the shift register is aborted and the write sequence is invalid. Under this condition, the DAC register is not updated and there is no change in the mode of operation or in the DAC output voltages.

8.5.3 Microwire Interface

Figure 30 shows an interface between a Microwire compatible device and the RS1324. Data is clocked out on the rising edges of the SK signal. As a result, the SK of the Microwire device must be inverted before driving the SCLK of the RS1324.

Figure 30. Microwire Interface

8.5.4 Bipolar Operation

The RS1324 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in Figure 31. This circuit will provide an output voltage range of ±5 V. A rail-to-rail amplifier must be used if the amplifier supplies are limited to ±5 V.

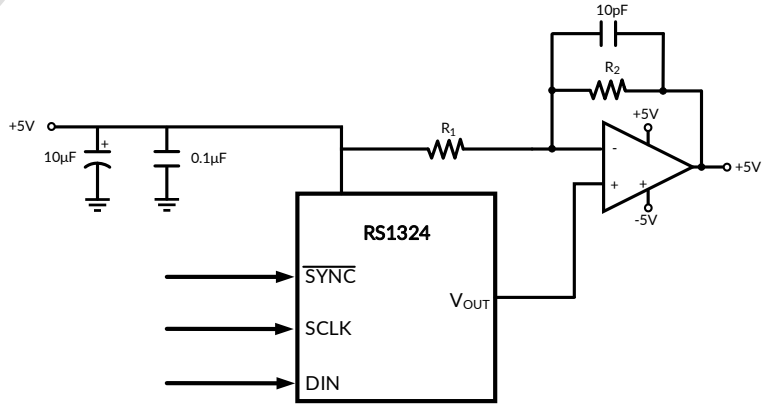


Figure 31. Bipolar Operation

Programming (continued)

8.5.4.1 Design Requirements

- The RS1324 uses a single supply.
- The output is required to be bipolar with a voltage range of ±5 V.
- Dual supplies are used for the output amplifier.

8.5.4.2 Detailed Design Procedure

The output voltage of this circuit for any code is found to be

$$V_O = (V_A \times (D / 4096) \times ((R1 + R2) / R1) - V_A \times R2 / R1 \quad (2)$$

where

- D is the input code in decimal form.

With V_A = 5 V and R1 = R2,

$$V_O = (10 \times D / 4096) - 5\ V \quad (3)$$

8.5.4.3 Application Curve

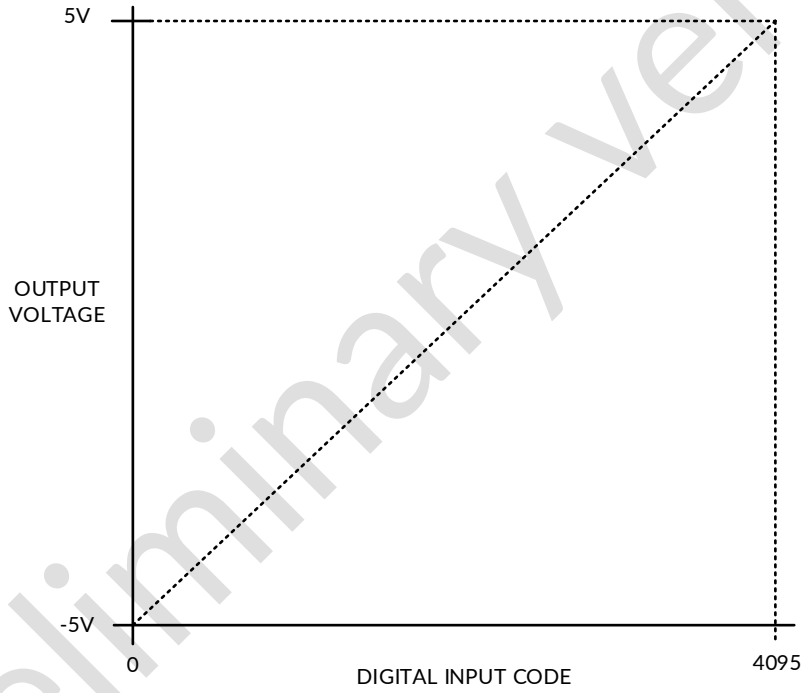


Figure 32. Bipolar Input and Output Transfer Characteristic

9 LAYOUT

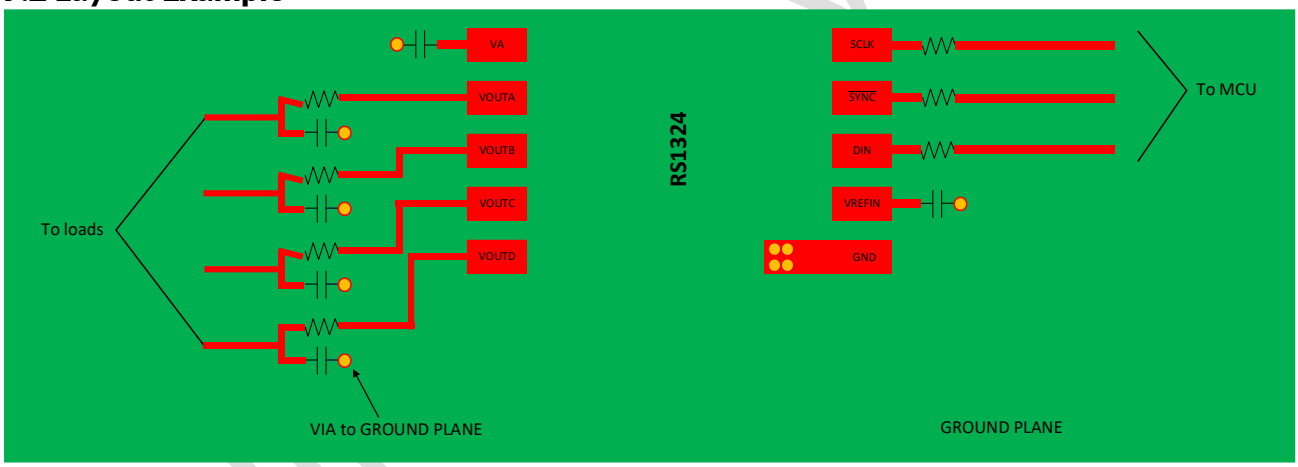
9.1 Layout Guidelines

For best accuracy and minimum noise, the printed-circuit board containing the RS1324 should have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located on the same board layer. There should be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design uses a fencing technique to prevent the mixing of analog and digital ground current. Separate ground planes should only be used when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the RS1324. Special care is required to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

The RS1324 power supply should be bypassed with a 10-µF and a 0.1-µF capacitor as close as possible to the device with the 0.1 µF right at the device supply pin. The 10-µF capacitor should be a tantalum type and the 0.1-µF capacitor should be a low ESL, low ESR type. The power supply for the RS1324 should only be used for analog circuits.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. These clock and data lines should have controlled impedances.

9.2 Layout Example



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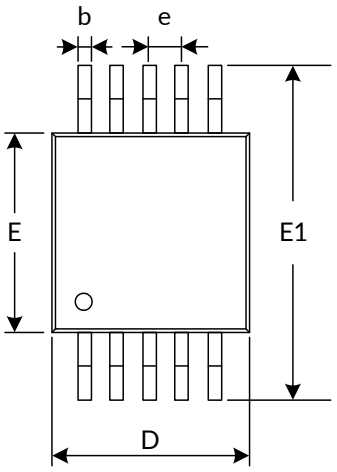
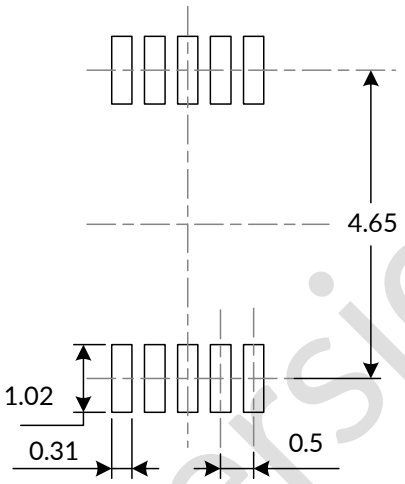
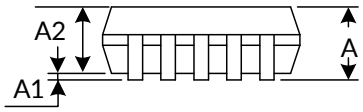
10 PACKAGE OUTLINE DIMENSIONS

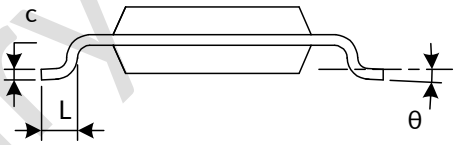
MSOP10 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D (1)	2.900	3.100	0.114	0.122
e	0.50(BSC) (2)		0.020(BSC) (2)	
E (1)	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

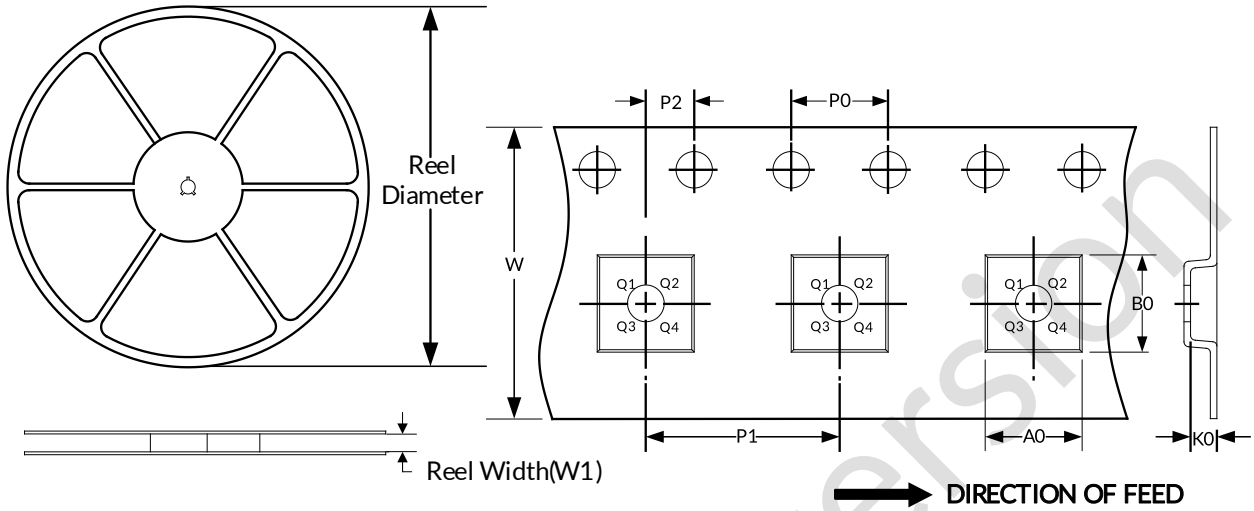
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

11 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP10	13”	12.4	5.20	3.30	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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