40V, 300mA, Low-Quiescent Current Adjustable Output Linear Regulator

1 FEATURES

- **Input Voltage Range: 3 V to 40 V**
- **Output Voltage Range:**
  - Fixed Option: 1.8V, 2.5V, 3.0V, 3.3V and 5.0V
  - Adjustable Option: 1.25V to 15V
- **Very Low I_Q: 7μA (TYP)**
- **Up to 300mA Load Current**
- **Very Low Dropout: 395mV at 300mA (V_{OUT}=5V)**
- **Power Good**
- **Programmable Power Good Delay**
- **Over Temperature Protection**
- **Over Current Limit Protection**
- **Short Circuit Protection is Typical 350mA**
- **Output Voltage Accuracy: ±1.5%**
- **Available in a ESOP8 Package**

2 APPLICATIONS

- **Industrial/Automotive Applications**
- **Portable/Battery-Powered Equipment**
- **Ultra Low-Power Microcontrollers**
- **Cellular Handsets**
- **Medical Imaging**

3 DESCRIPTIONS

The RS3017 is a Low Dropout Linear Regulator designed by CMOS technology. Which can provide 300mA output current. The device allows input voltage as high as 40V. It is very suitable for standby microprocessor control-unit systems, especially in automotive applications. Wide input voltage can make it well withstand the impact of surge voltage and ensure the stability of output voltage.

The RS3017 provides a wide variety of fixed output-voltage options: 1.8V, 2.5V, 3.0V, 3.3V and 5.0V; Also, it provides the output-adjustable option (from 1.25V to 15V).

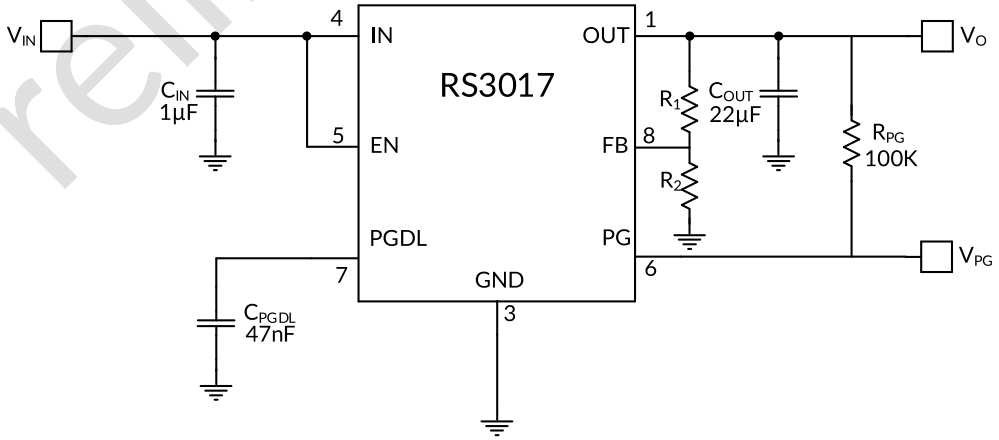
The regulator output current is limited internally, and the device is protected against short-circuit, over-load, and over-temperature conditions.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS3017	ESOP8	4.90mm×3.90mm

(1) For all available packages, see the orderable addendum at the next page of the data sheet.

4 TYPICAL APPLICATION SCHEMATIC



5 FUNCTIONAL BLOCK DIAGRAM

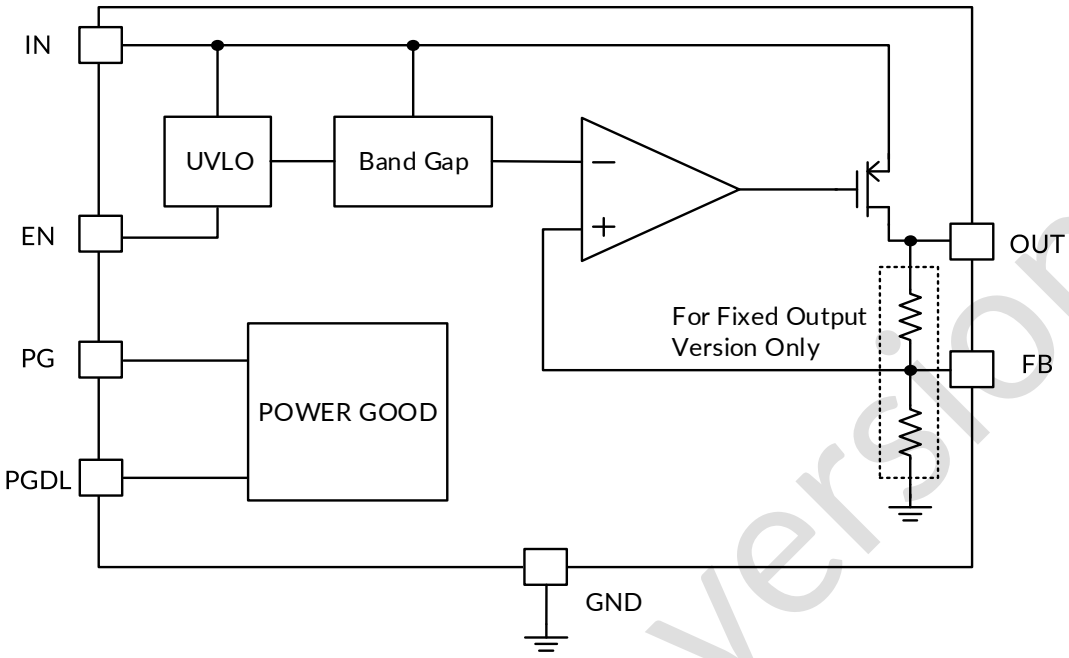


Table of Contents

6 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2025/07/01	Preliminary version completed
A.0.1	2025/11/28	1. Update PIN CONFIGURATION AND FUNCTIONS 2. Update Absolute Maximum Ratings

7 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	V_{OUT}(V)	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS3017-1.8	RS3017-1.8XEK-G	1.8	ESOP8	3017-18	TBD	Tape and Reel, 4000
RS3017-2.5	RS3017-2.5XEK-G	2.5	ESOP8	3017-25	TBD	Tape and Reel, 4000
RS3017-3.0	RS3017-3.0XEK-G	3.0	ESOP8	3017-30	TBD	Tape and Reel, 4000
RS3017-3.3	RS3017-3.3XEK-G	3.3	ESOP8	3017-33	TBD	Tape and Reel, 4000
RS3017-5.0	RS3017-5.0XEK-G	5.0	ESOP8	3017-50	TBD	Tape and Reel, 4000
RS3017-ADJC	RS3017-ADJCXEK-G	ADJ	ESOP8	3017-ADJC	TBD	Tape and Reel, 4000

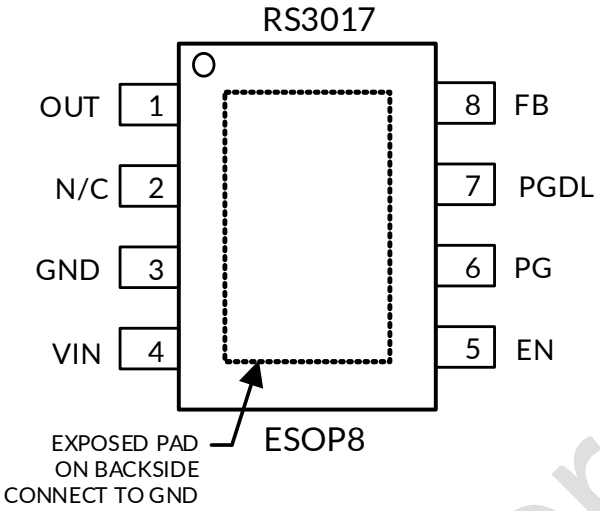
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

8 PIN CONFIGURATION AND FUNCTIONS



PIN DESCRIPTION

NAME	PIN	I/O (1)	FUNCTION
	ESOP8		
OUT	1	O	Regulated output voltage.
N/C	2	-	Not-connected pin.
GND	3	G	Ground reference.
VIN	4	I	Input power-supply voltage.
EN	5	I	Enable pin. The device enters the standby state when the enable pin becomes lower than the enable threshold.
PG	6	O	Power good. This open-drain pin must connect to V_{OUT} via an external resistor. V_{PG} is logic level high when V_{OUT} is above the power-on-reset threshold.
PGDL	7	O	Power good delay adjustment. Connecting a capacitor from this pin to GND changes the PG reset delay.
FB	8	I	Feedback pin when using external resistor divider.

(1) I = Input, O = Output, G=Ground.

9 SPECIFICATIONS

9.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{IN}	Input voltage		-0.3	45	V
V_{EN}	V_{EN} voltage range		-0.3	45	V
V_{OUT}	V_{OUT} voltage range		-0.3	20	V
V_{PG}	V_{PG} voltage range		-0.3	20	V
V_{PGDL}	V_{PGDL} voltage range		-0.3	6.6	V
V_{FB}	V_{FB} voltage range		-0.3	6.6	V
T_J	PN Junction temperature (3)		-40	150	°C
P_D	Continuous power dissipation (4)		Internally limited		W
θ_{JA}	Junction-to-ambient thermal resistance (5)	ESOP8		30	°C/W
θ_{JC}	Junction-to-case thermal resistance (5)			20	°C/W
Ψ_{JT}	Junction-to-top characterization parameter (5)			10	°C/W
T_{stg}	Storage temperature range		-40	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the GND pin.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(4) Internal thermal shutdown circuitry protects the device from permanent damage. The actual chip output current is subject to the input-output voltage difference, ambient temperature and PCB heat dissipation design.

(5) The package thermal impedance is calculated in accordance with JESD-51.

9.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), MIL-STD 883J	±4000	V
		Charge-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1000	V
		Machine Model (MM), JESD22-A115C (2010)	±100	V

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input Voltage Range	3	40	V
EN	Voltage Range of EN Pin	0	40	V
V_{OUT}	Output Voltage Range	1.25	15	V
PG	Voltage Range of PG Pin	0	15	V
I_{OUT}	Output Current Range	1	300	mA
C_{OUT}	Capacitor of V_{OUT} pin	2.2	100	μF
T_J	PN Junction temperature	-40	150	°C

(1) All voltages are with respect to the GND pin.

(2) The chip's operating temperature is determined by the junction temperature (T_J), the relationship between T_A and T_J, please refer to the application note as below. The larger the T_A, the smaller the space left for the chip temperature rise.

9.4 Electrical Characteristics

Over operating temperature range (−40°C ≤ T_J ≤ 150°C), V_{IN} = 14V, I_{OUT}=1mA, C_{OUT} = 22μF, C_{PGDL}=47nF, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY AND CURRENTS							
Input Voltage (1)	V_{IN}			3		40	V
Under Voltage Lockout	UVLO	VIN rising			2.6		V
Hysteresis	V_{HYS}	VIN falling			250		mV
Quiescent Current	I_Q	V_{IN}=14V, I_{OUT}=0mA (Adjustable, V_{OUT}=FB)			7		μA
		V_{IN}=40V, I_{OUT}=0mA (Adjustable, V_{OUT}=FB)			8		
Ground Pin Current	I_{GND}	I_{OUT} = 300mA			0.6		mA
Shutdown Current	I_{SD}	V_{EN}=0V, V_{IN}=40V			1		μA
OUTPUT VOLTAGE							
Output Voltage Range	V_{OUT}	Adjustable Version		V_{FB}		15	V
Feedback Voltage (1)	V_{FB}	Adjustable Version, T_J = 25°C, I_{OUT}=1mA		1.2315	1.250	1.2685	V
Feedback Pin Current	I_{FB}	Adjustable Version, V_{FB}=1.3V				0.05	μA
DC Output Accuracy (1)	ΔV_{OUT}	T_J = 25°C, I_{OUT} = 1mA			±1.5		%
Line Regulation (1)	$\Delta V_{OUT(\Delta VIN)}$	Adjustable Version, V_{OUT}=FB; V_{IN} = 3V to 40V, I_{OUT} = 1mA			0.001		%/V
Load Regulation (1)	$\Delta V_{OUT(\Delta IOUT)}$	Adjustable Version, V_{OUT}=FB; I_{OUT} = 1mA to 300mA			1		mV
Output Voltage Temperature Coefficient (4)	$\frac{\Delta V_{OUT}}{\Delta T_A \times V_{OUT}}$	I_{OUT} = 1mA, T_J = -40°C ~ 85°C			50		ppm/°C
		I_{OUT} = 1mA, T_J = -40°C ~ 125°C			45		
		I_{OUT} = 1mA, T_J = -40°C ~ 150°C			40		
Maximum Output Current (5)	I_{OUTMAX}			300			mA
DROPOUT VOLTAGE							
Dropout Voltage (6)	V_{DO}	I_{OUT} = 300mA	V_{IN} = 3V, V_{DO}=V_{IN}-V_{OUT}		525		mV
			V_{OUT} = 3.3V		460		
			V_{OUT} = 5.0V		395		
POWER SUPPLY REJECTION RATIO AND NOISE							
Power Supply Rejection Ratio (7)	PSRR	V_{IN} =14V, V_{OUT} = 3.3V, I_{OUT} = 10mA	f = 100Hz		61		dB
			f = 1KHz		53		dB
			f = 10KHz		64		dB
			f = 100KHz		57		dB
Output Noise Voltage (7)	V_N	BW=10Hz~100KHz, V_{OUT}=FB, I_{OUT}=10mA			80		μV_{RMS}
ENABLE AND STARTUP TIME							
EN Input Logic High Voltage	V_{IH}	V_{IN} = 3V to 40V, EN rising		1.7			V
EN Input Logic Low Voltage	V_{IL}	V_{IN} = 3V to 40V, EN falling				0.4	V
EN Input Leakage Current	I_{EN}	V_{IN} = 40V, V_{EN} = 0V				0.01	μA
		V_{IN} = 40V, V_{EN} = 40V			1.5		μA
Output Voltage Delay Time	TD	From V_{EN} > V_{IH} to V_{OUT} = 10% of V_{OUT}nom			200		μs
Output Rise Time	TR	From V_{OUT} = 10% to 90% of V_{OUT}nom			850		μs

PG AND DELAY						
PG Rising Threshold	V_{th_PG}	V_{FB} rising		90%		VFB
PG Rising Threshold Hysteresis	$V_{th\_PG\_hys}$	V_{FB} falling		5.5%		
PG Low Voltage	V_{PG}	Sink 1mA Current		0.1		V
PG Leakage Current	I_{PG_LKG}	V_{PG} = 5V		0.01		μA
PGDL Charging Current	I_{PGDL}	V_{PGDL} = 1V		5.7		μA
PGDL Rising Threshold	PGDL_H	PGDL rising		1.74		V
PGDL Falling Threshold	PGDL_L	PGDL falling		0.4		V
PG Delay Time	t_{PGDL}	C_{PGDL} = 47nF		14.5		ms
PG Deglitch Time	$t_{(Deglitch)}$	C_{PGDL} = 47nF		250		μs
PROTECTIONS						
Over Current Limit	I_{LMT}	V_{IN} = 14V, V_{OUT} = 0.95*V_{OUT}nom		550		mA
Short-Circuit Current Limit	I_{SC}	V_{IN} = 14V, V_{OUT} = 0V		350		mA
Thermal Shutdown Threshold (7)	T_{TSD}	T_J rising		160		°C
Thermal Shutdown Hysteresis (7)	T_{HYS}	T_J falling from shutdown		30		°C

NOTE:

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 3V, whichever is greater.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) Output voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.

(5) Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when V_{IN} < V_{OUT} + V_{DROP}.

(6) The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 2% below the value of V_{OUT} for V_{IN} = V_{OUT}nom + 1V.

(7) Guaranteed by design and characterization, not a FT item.

9.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{IN} = 14V, C_{IN} = 1µF, C_{OUT} = 22µF, C_{PGDL} = 47nF, unless otherwise noted.

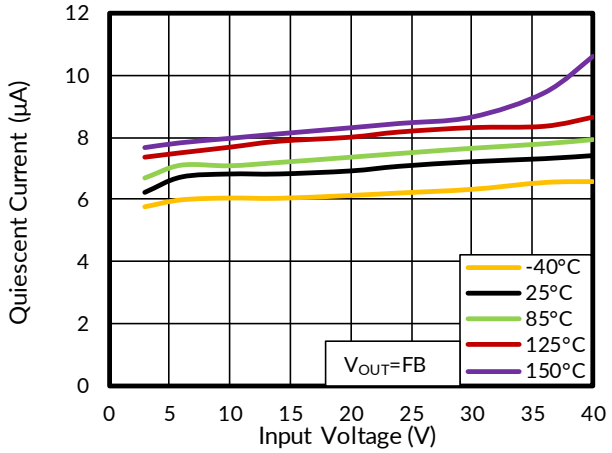


Figure 1. Quiescent Current vs Input Voltage

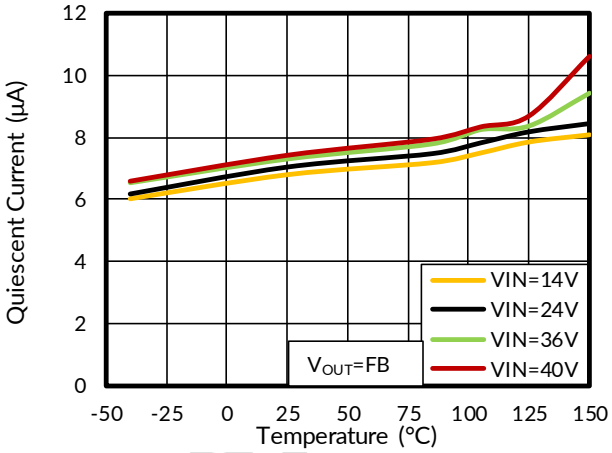


Figure 2. Quiescent Current vs Junction Temperature

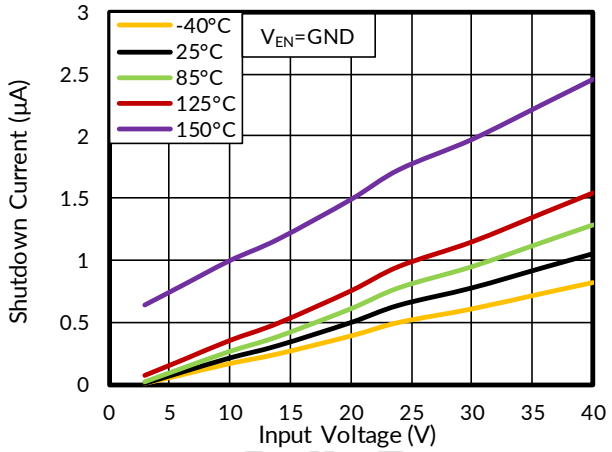


Figure 3. Shutdown Current vs Input Voltage

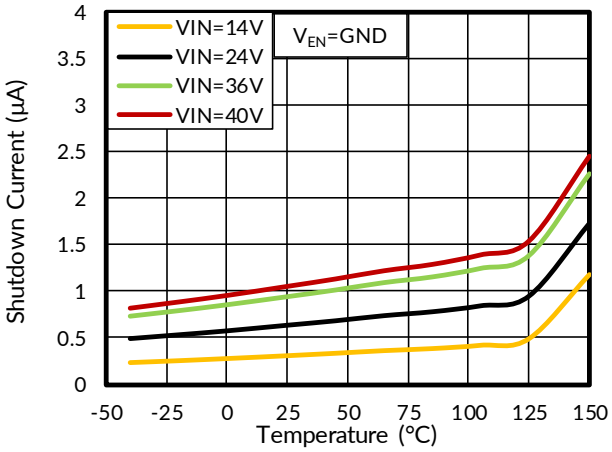


Figure 4. Shutdown Current vs Junction Temperature

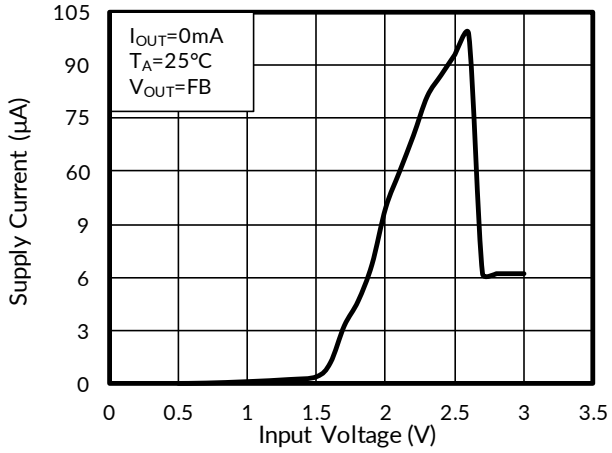


Figure 5. Supply Current vs Input Voltage

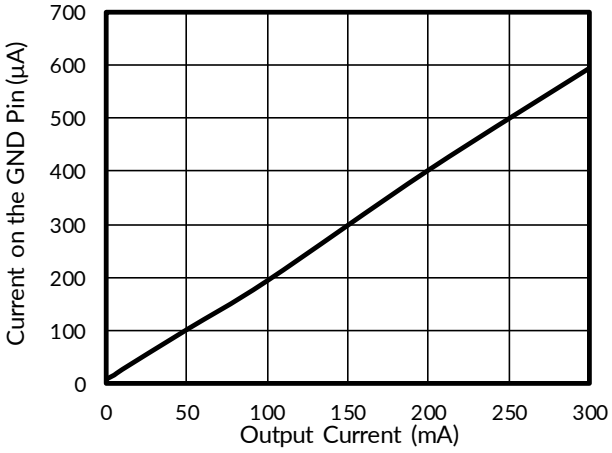


Figure 6. Ground Pin Current vs Output Current

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{IN} = 14V, C_{IN} = 1μF, C_{OUT} = 22μF, C_{PGDL} = 47nF, unless otherwise noted.

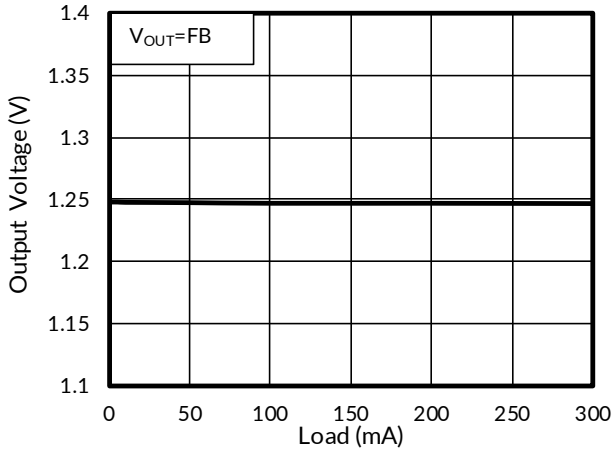


Figure 7. Load Regulation

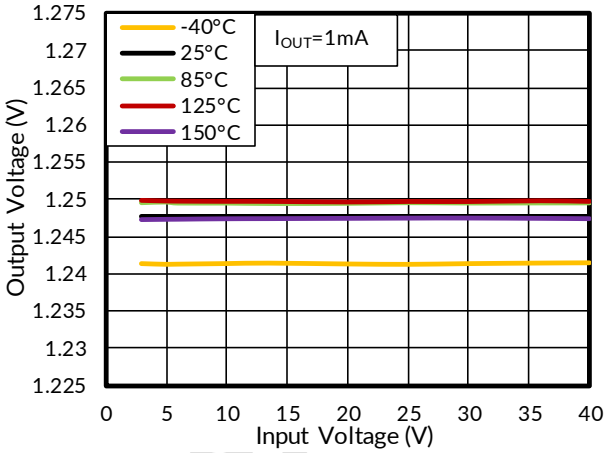


Figure 8. Line Regulation

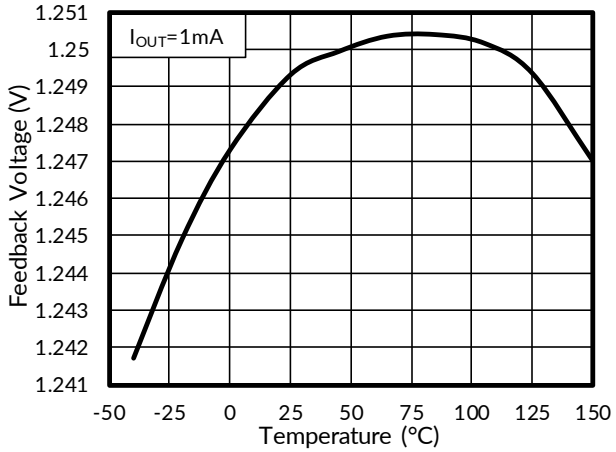


Figure 9. Feedback Voltage vs Junction Temperature

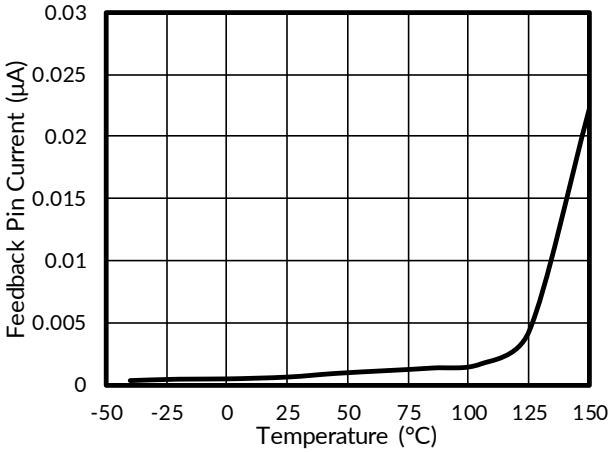


Figure 10. Feedback Pin Current vs Junction Temperature

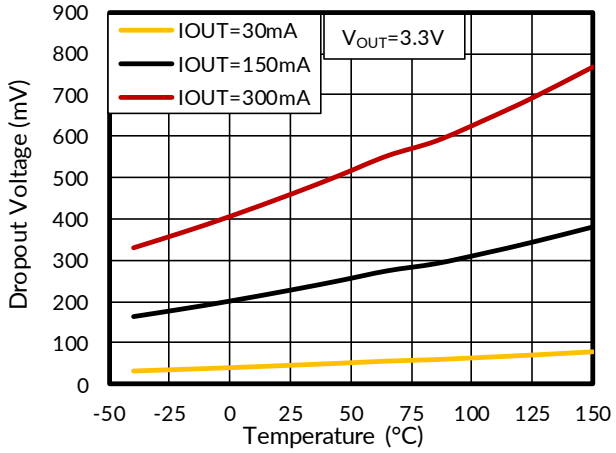


Figure 11. Dropout Voltage vs Junction Temperature

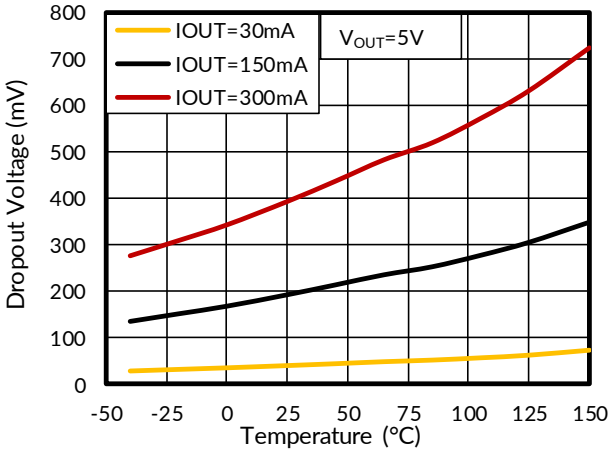


Figure 12. Dropout Voltage vs Junction Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{IN} = 14V, C_{IN} = 1μF, C_{OUT} = 22μF, C_{PGDL} = 47nF, unless otherwise noted.

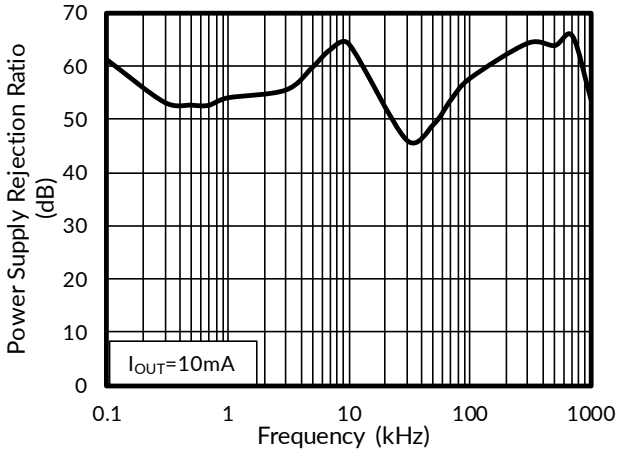


Figure 13. Power Supply Rejection Ratio vs Frequency

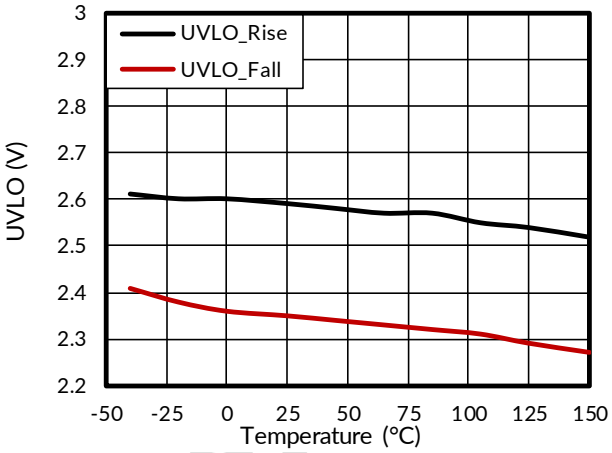


Figure 14. UVLO vs Junction Temperature

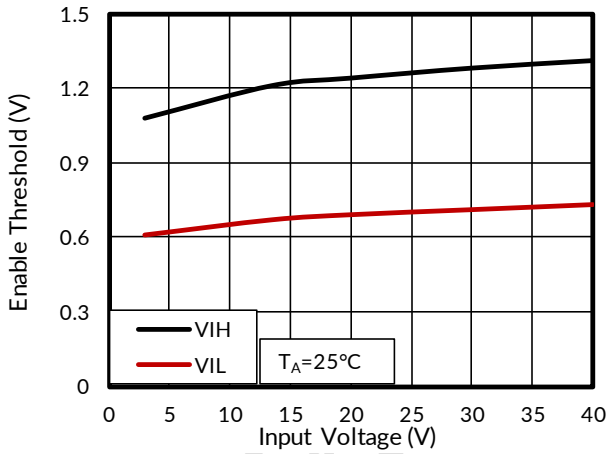


Figure 15. Enable Threshold vs Input Voltage

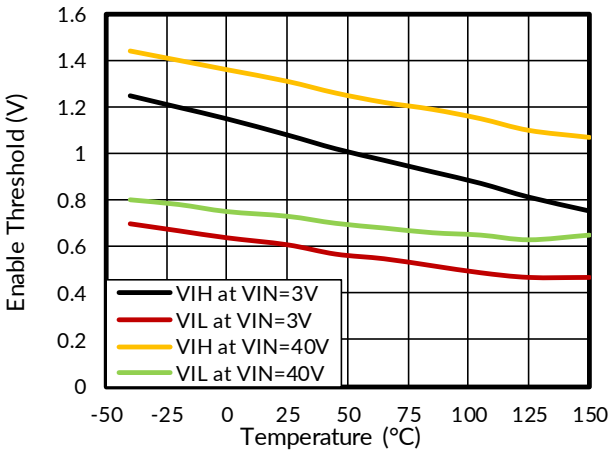


Figure 16. Enable Threshold vs Junction Temperature

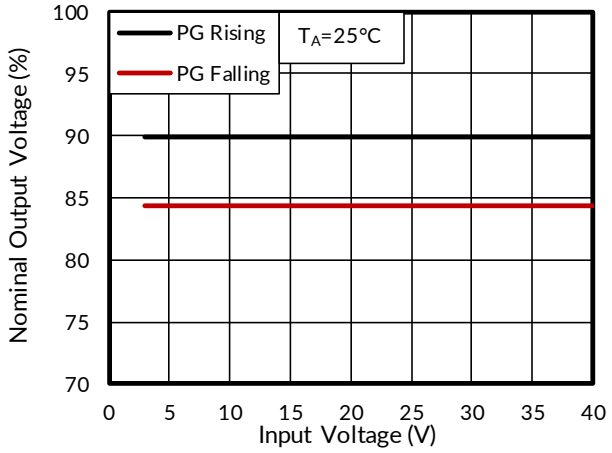


Figure 17. Power-Good Threshold Voltage vs Input Voltage

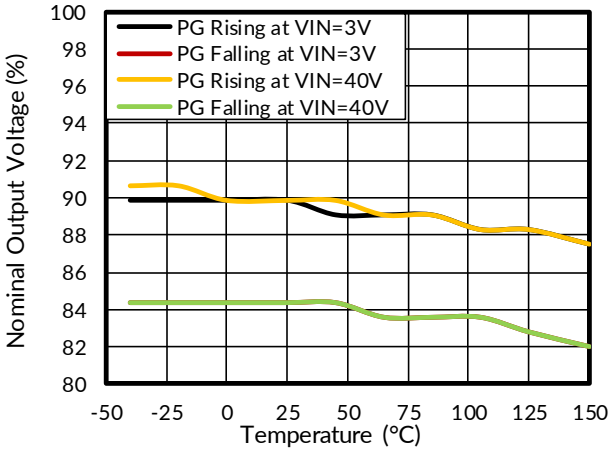


Figure 18. Power-Good Threshold Voltage vs Junction Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{IN} = 14V, C_{IN} = 1μF, C_{OUT} = 22μF, C_{PGDL} = 47nF, unless otherwise noted.

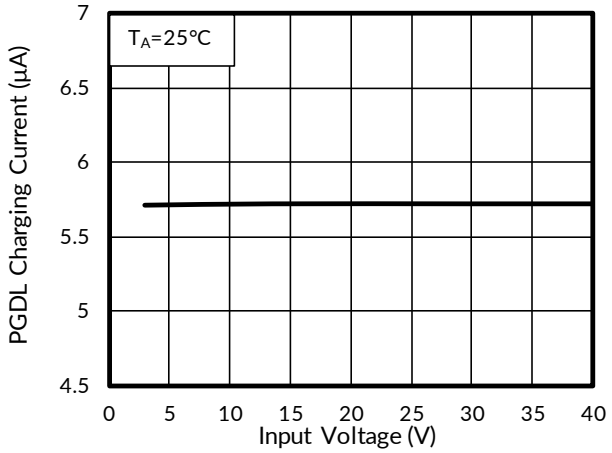


Figure 19. PGDL Charging Current (V_{PGDL} = 1V)

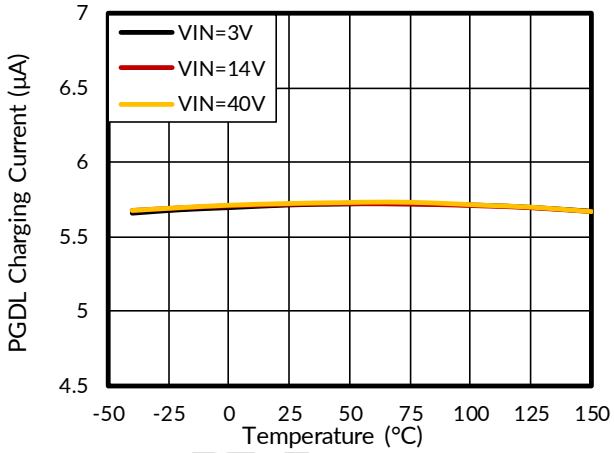


Figure 20. PGDL Charging Current (V_{PGDL} = 1V)

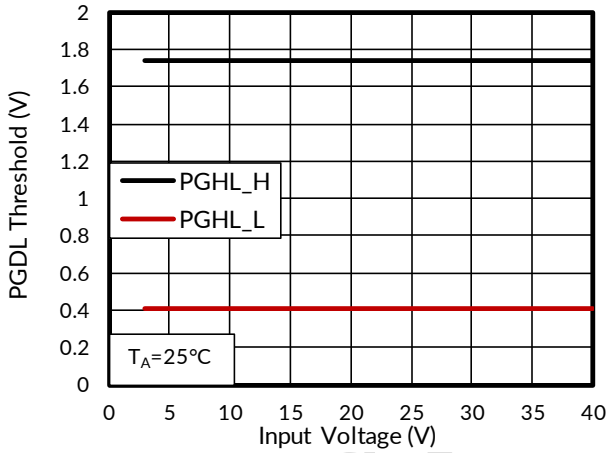


Figure 21. PGDL Charging Threshold

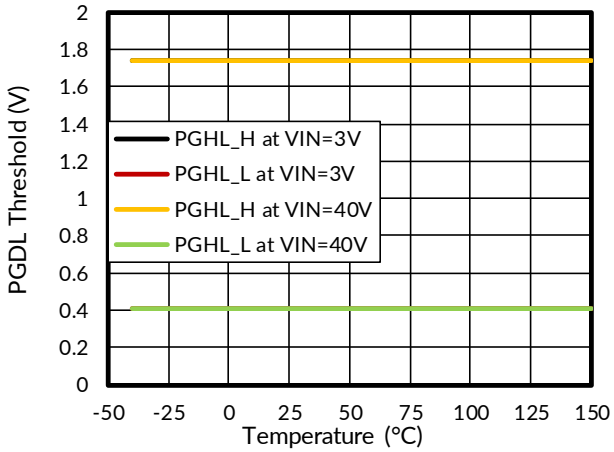


Figure 22. PGDL Charging Threshold

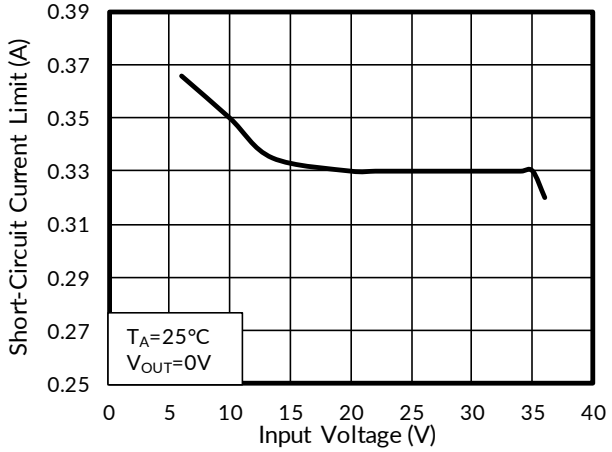


Figure 23. Short-Circuit Current Limit vs Input Voltage

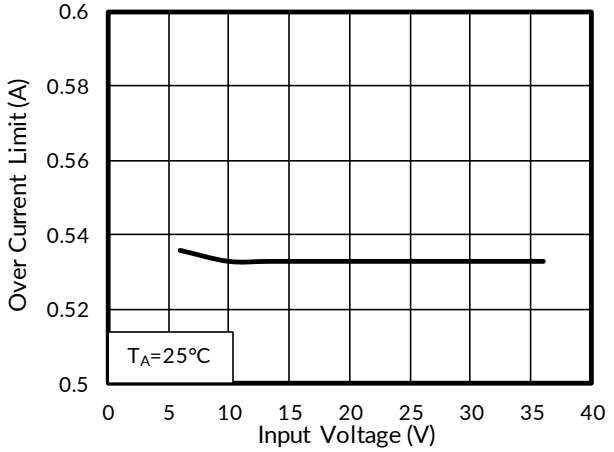


Figure 24. Over Current Limit vs Input Voltage

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{IN} = 14V, C_{IN} = 1μF, C_{OUT} = 22μF, C_{PGDL} = 47nF, unless otherwise noted.

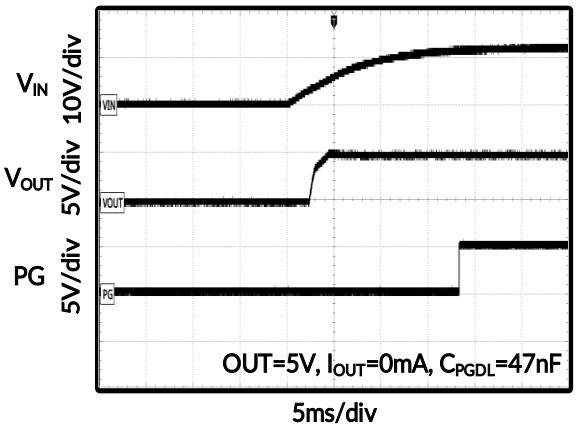


Figure 25. Start-Up Through V_{IN}

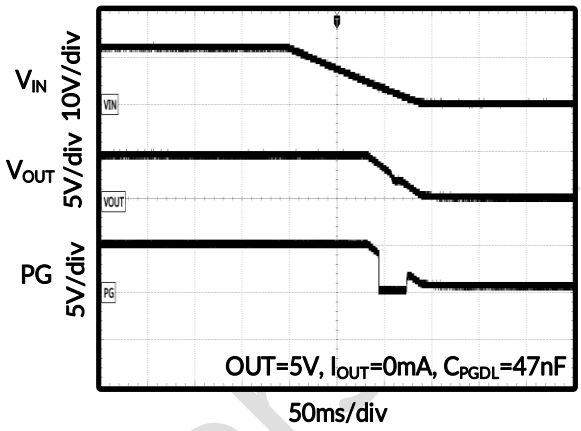


Figure 26. Start-Up Through V_{IN}

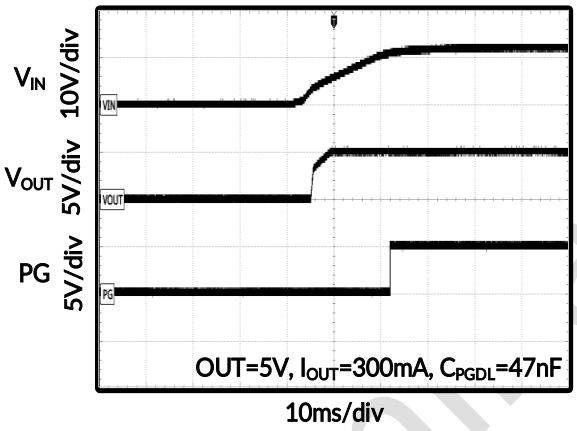


Figure 27. Start-Up Through V_{IN}

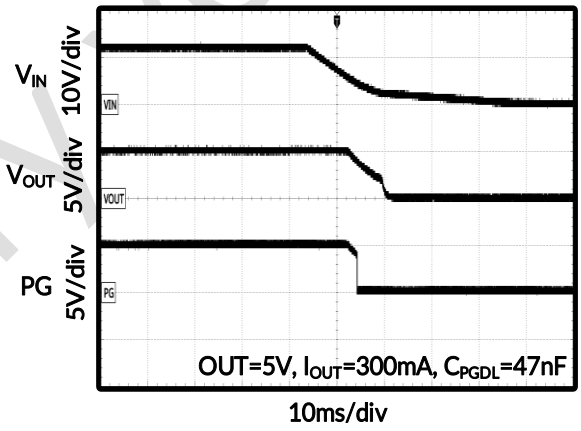


Figure 28. Start-Up Through V_{IN}

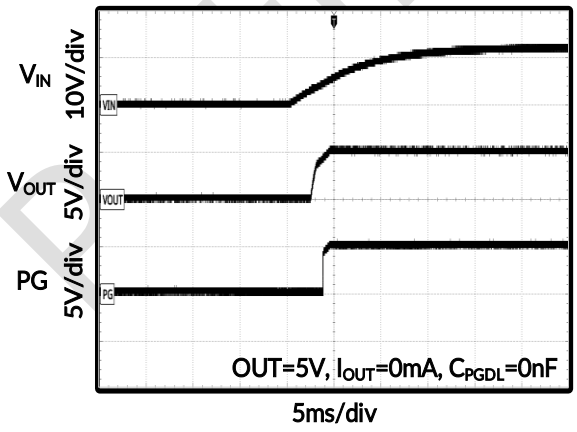


Figure 29. Start-Up Through V_{IN}

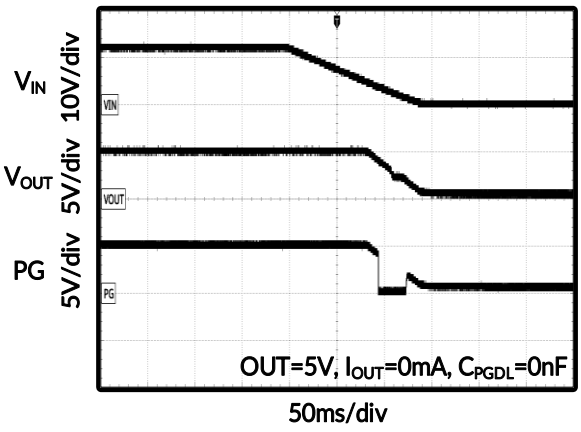


Figure 30. Start-Up Through V_{IN}

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{IN} = 14V, C_{IN} = 1μF, C_{OUT} = 22μF, C_{PGDL} = 47nF, unless otherwise noted.

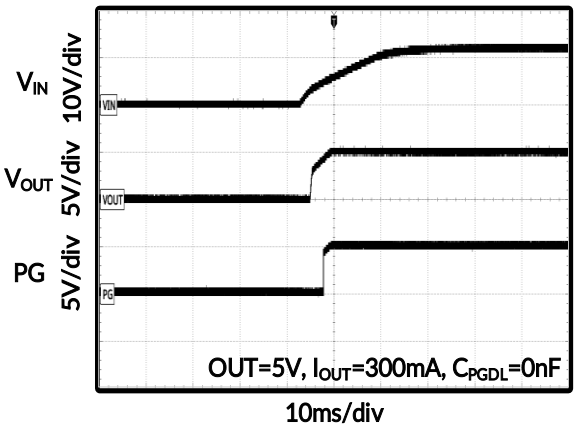


Figure 31. Start-Up Through V_{IN}

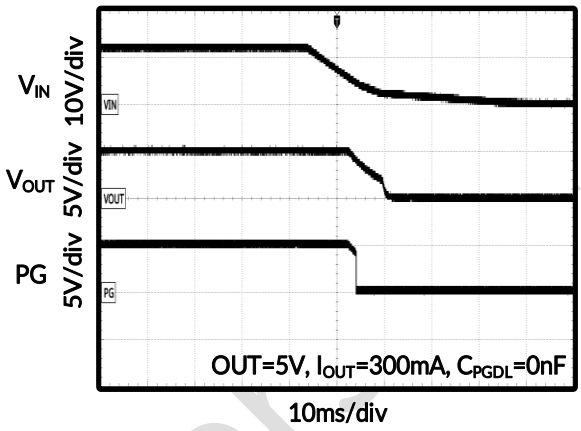


Figure 32. Start-Up Through V_{IN}

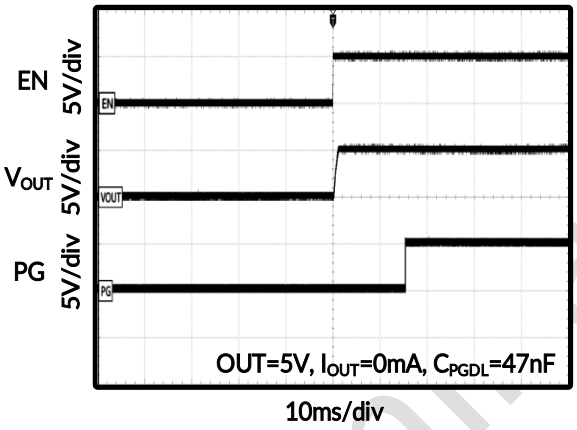


Figure 33. Start-Up Through EN

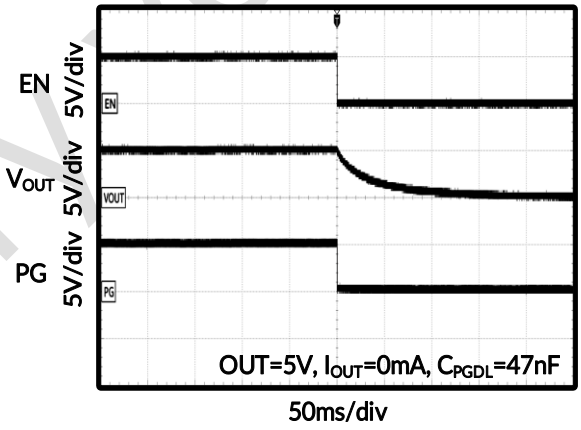


Figure 34. Start-Up Through EN

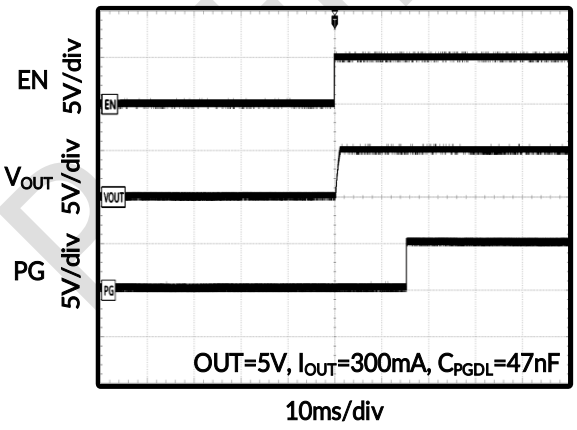


Figure 35. Start-Up Through EN

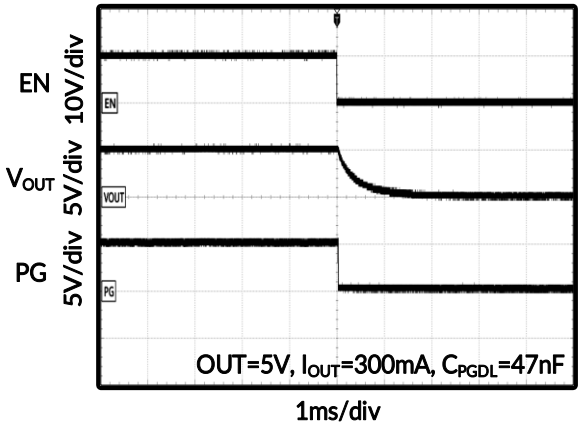


Figure 36. Start-Up Through EN

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{IN} = 14V, C_{IN} = 1μF, C_{OUT} = 22μF, C_{PGDL} = 47nF, unless otherwise noted.

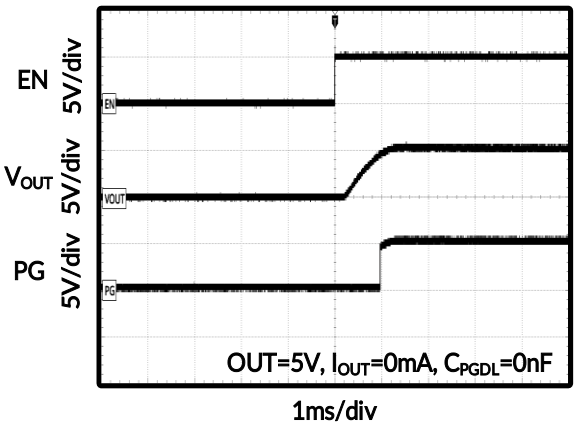


Figure 37. Start-Up Through EN

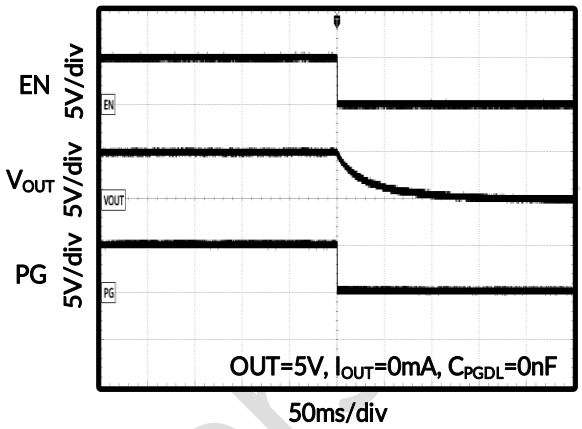


Figure 38. Start-Up Through EN

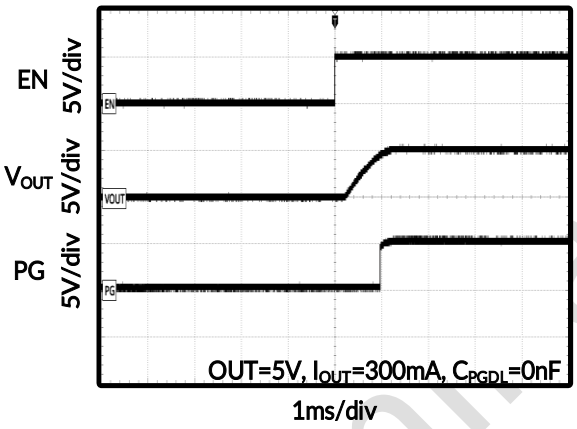


Figure 39. Start-Up Through EN

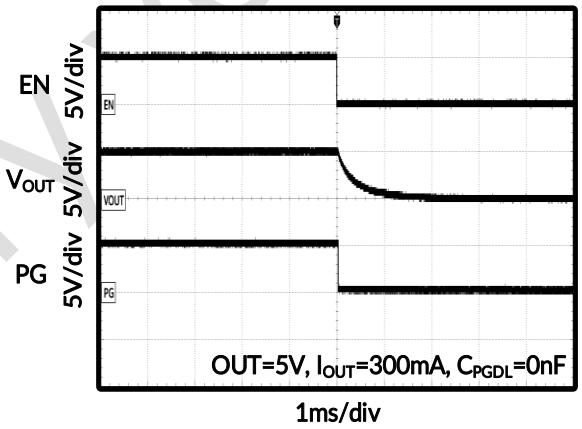


Figure 40. Start-Up Through EN

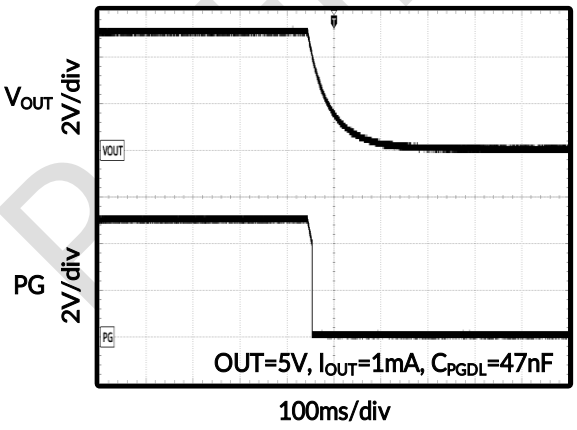


Figure 41. Over-Temperature Protection

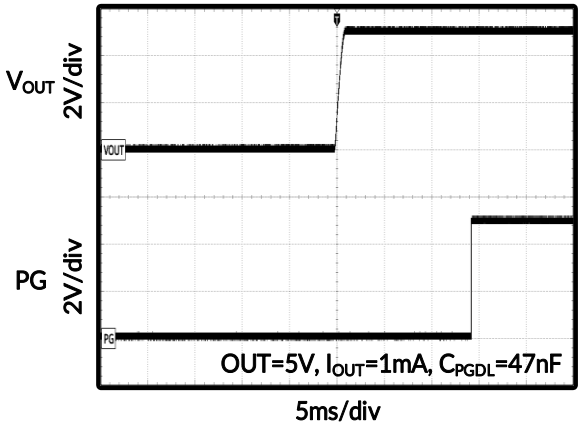


Figure 42. Over-Temperature Protection

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{IN} = 14V, C_{IN} = 1μF, C_{OUT} = 22μF, C_{PGDL} = 47nF, unless otherwise noted.

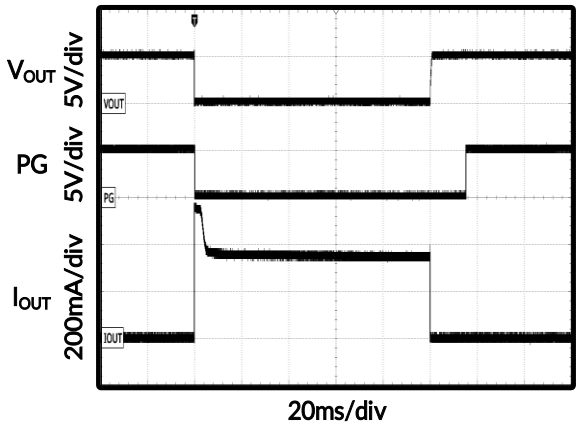


Figure 43. Turn On First, Then Short Circuit

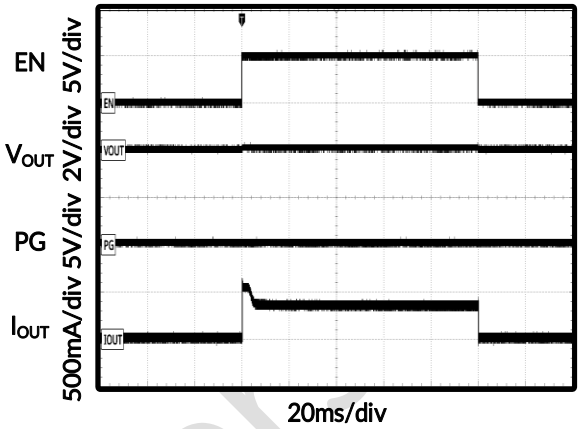


Figure 44. Short Circuit First, Then EN Power ON

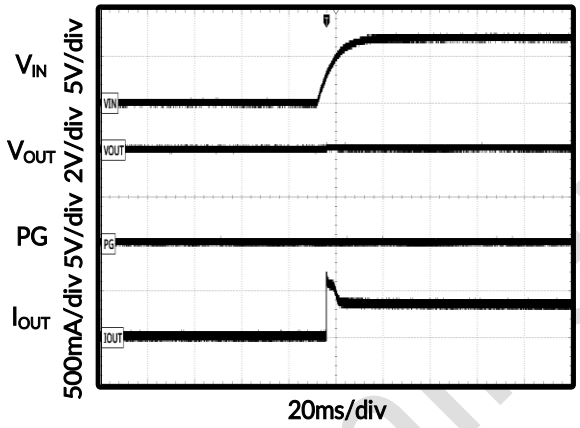


Figure 45. Short Circuit First, Then VIN Power ON

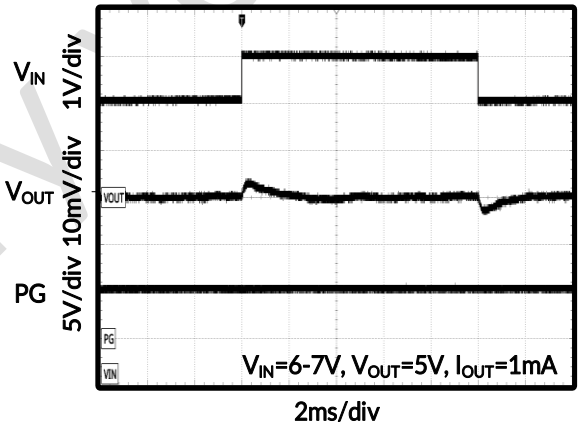


Figure 46. Line Transient Response

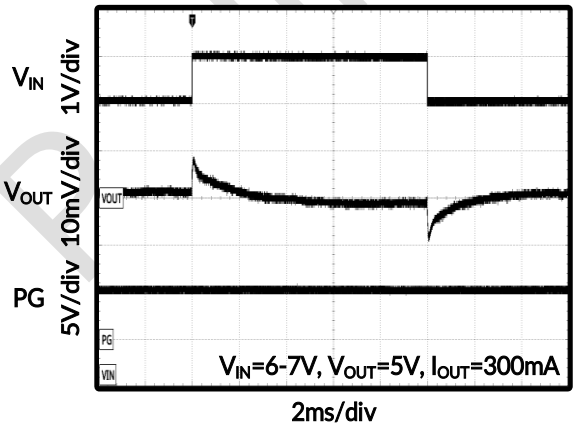


Figure 47. Line Transient Response

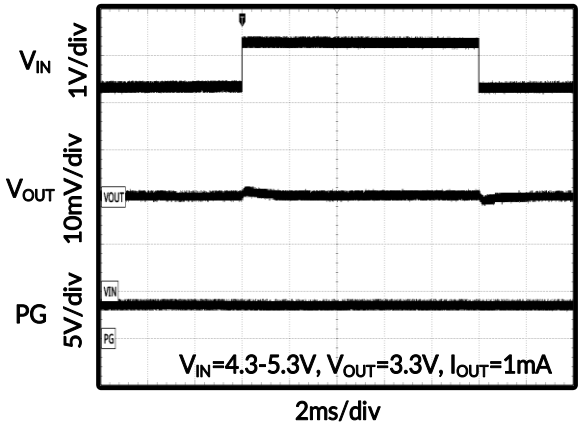


Figure 48. Line Transient Response

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At V_{IN} = 14V, C_{IN} = 1μF, C_{OUT} = 22μF, C_{PGDL} = 47nF, unless otherwise noted.

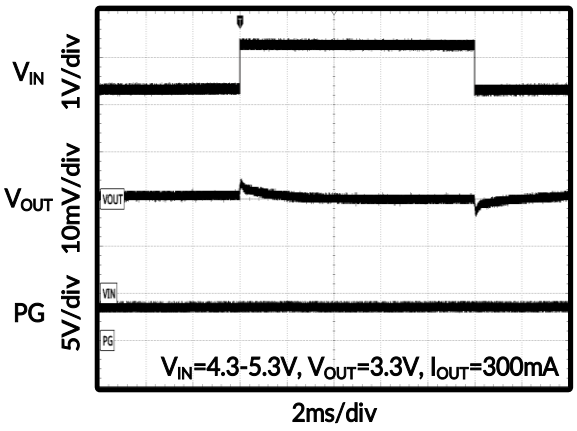


Figure 49. Line Transient Response

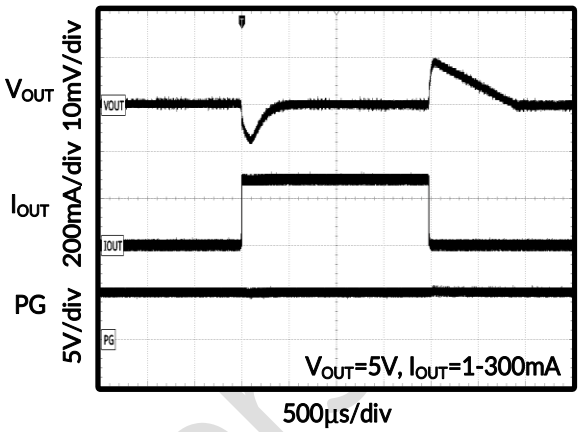


Figure 50. Load Transient Response

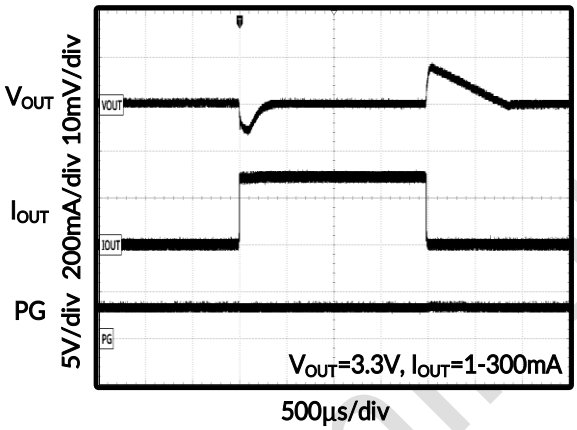


Figure 51. Load Transient Response

10 DETAILED DESCRIPTION

10.1 Overview

The RS3017 is a Low Dropout Linear Regulator designed by CMOS technology. Which can provide 300mA output current. The device allows input voltage as high as 40V. It is very suitable for standby microprocessor control-unit systems, especially in automotive applications. Wide input voltage can make it well withstand the impact of surge voltage and ensure the stability of output voltage.

The RS3017 provides a wide variety of fixed output-voltage options: 1.8V, 2.5V, 3.0V, 3.3V and 5.0V; Also, it provides the output-adjustable option (from 1.25V to 15V).

The regulator output current is limited internally, and the device is protected against short-circuit, over-load, and over-temperature conditions.

10.2 Under Voltage Lockout (UVLO)

The RS3017 family of devices uses an under voltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

10.3 Shutdown

Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off and a high voltage (> V_{IH}) on this pin enables the regulator output. The EN pin can be connected to the VIN pin if not used. Do not leave floating.

10.4 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 130°C, the output circuitry enables.

Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the RS3017 has been designed to protect against temporary thermal overload conditions. The T_{SD} circuitry was not intended to replace proper heat-sinking. Continuously running the RS3017 device into thermal shutdown may degrade device reliability.

10.5 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO threshold minus V_{HYS}, or has not yet exceeded the UVLO threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

10.6 Current-Limit Protection

The RS3017 monitors the current flowing through the output PMOS and limits the maximum current to prevent damage to the load and RS3017 during current overload conditions.

10.7 Short Current-Limit Protection

The short current-limit function reduces the current-limit level down to 350mA (typical) during short circuit conditions.

10.8 PG and Delay

RS3017 has one power good (PG) pin. The PG pin is the open drain of an internal MOSFET. It should be connected to V_{OUT} (<15V) through a resistor. After the V_{FB} reaches 90% of nominal value, the MOSFET turns off

and PG pin is pulled to high by V_{OUT}. When the V_{FB} drops to 84.5% of nominal value, the PG voltage is pulled to GND.
There is a delay time when PG asserts high. The delay time can be programmed by adding a capacitor on PGDL. To select a capacitor for PGDL, use below equation:

$$C_{PGDL}\,(nF) = \frac{t_{PGDL}\,(ms) \times I_{PGDL}\,(\mu A)}{PGDL\_H\,(V)} \quad (1)$$

Where t_{PGDL} is the desired delay time for PG asserts high, I_{PGDL} (5.7μA, TYP) is the PGDL charging current and PGDL_H (1.74V, TYP) is the PGDL rising threshold.

Figure 52 shows the power good timing.

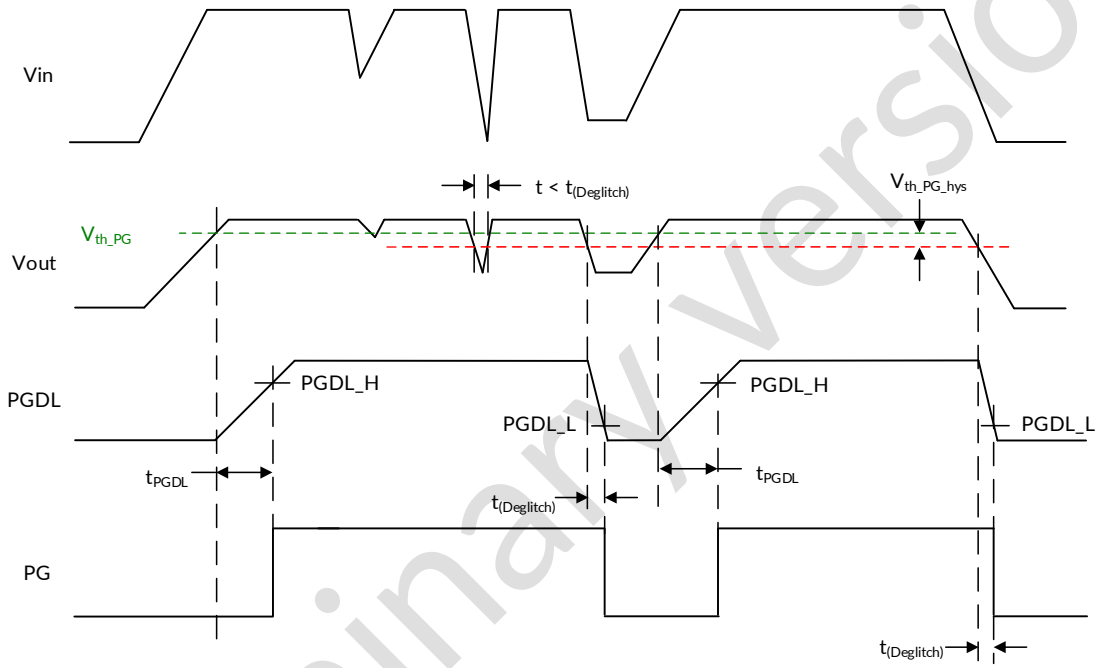


Figure 52. Conditions for Activation of Reset

10.9 Input and Output Capacitor Requirements

Connecting a 1μF low-equivalent series resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher value capacitor can be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the power source.

The RS3017 family of devices is designed to be stable with standard ceramic output capacitors of values 2.2μF or larger. However, for better performance, 22μF or larger is recommended. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature.

10.10 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the Electrical Characteristics table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \le V_{OUT} / (I_{FB} \times 100) \quad (3)$$

11 POWER SUPPLY RECOMMENDATIONS

The device is designed to operate from an input voltage supply range between 3V and 40V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

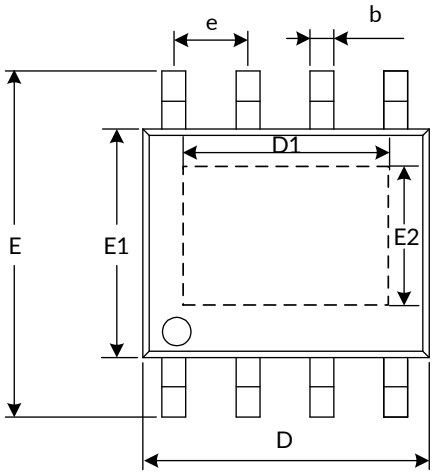
12 LAYOUT

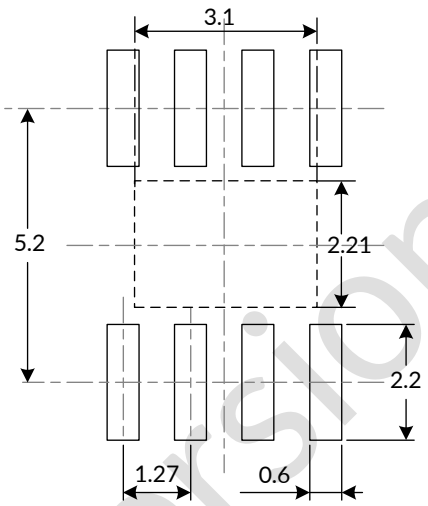
For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

To improve ac performance (such as PSRR, output noise, and transient response), designing the board with separate ground planes for V_{IN} and V_{OUT} is recommended, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

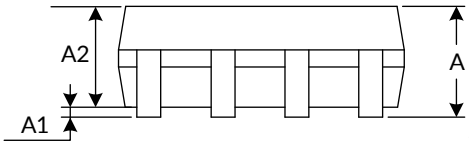
13 PACKAGE OUTLINE DIMENSIONS

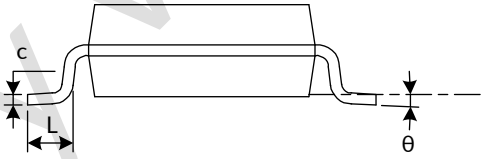
ESOP8 (4)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.650		0.065
A1	0.050	0.150	0.002	0.006
A2	1.300	1.500	0.051	0.059
b	0.390	0.470	0.015	0.019
c	0.200	0.240	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
e	1.270 (BSC) (2)		0.050 (BSC) (2)	
D1	3.100 (REF) (3)		0.122 (REF) (3)	
E2	2.210 (REF) (3)		0.087 (REF) (3)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.500	0.800	0.019	0.032
θ	0°	8°	0°	8°

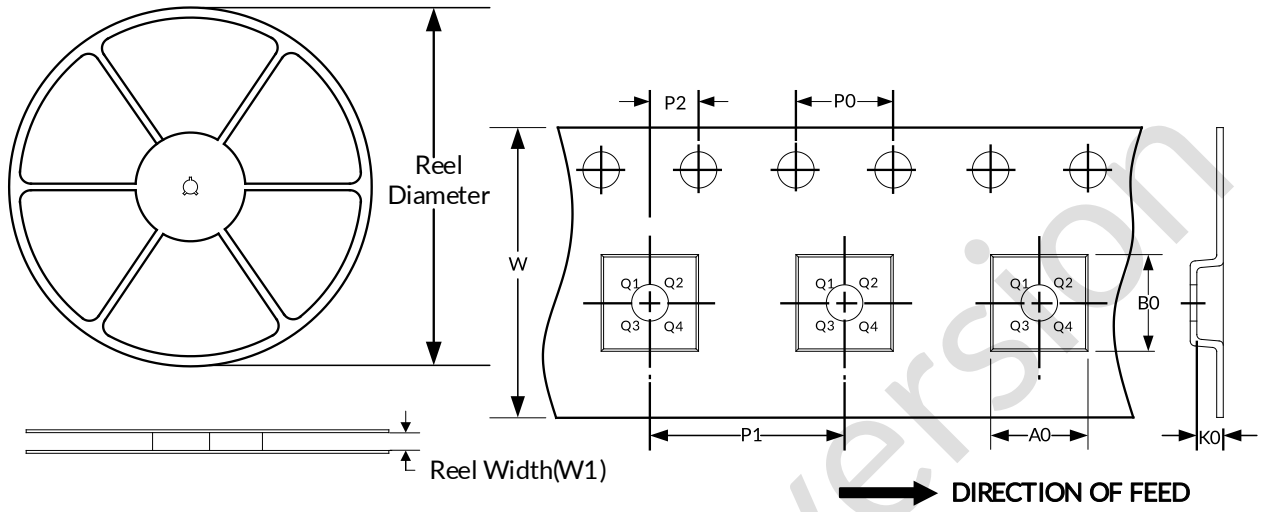
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
ESOP8	13”	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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