RS07 Precision Operational Amplifiers

1 FEATURES

- **Low V_{OS}: 110μV (Max) over -40°C to 125°C**
- **High Open Loop Gain: 140dB**
- **High PSRR: 120dB**
- **Low Bias Current: 10pA**
- **High Gain-Bandwidth Product: 2.5MHz**
- **Low Quiescent Current: 1.45mA**
- **High Capacitive Load: 10nF**
- **Low Noise: 9nV/$\sqrt{\text{Hz}}$ at 10kHz**
- **No External Components Required**
- **Replace Chopper Amplifiers at a Lower Cost**
- **Wide Supply-Voltage Range: 4.5V to 36V**
- **Operating Temperature Range: -40°C to 125°C**
- **Micro SIZE PACKAGES: SOP8**

2 APPLICATIONS

- **Wireless Base Station Control Circuits**
- **Optical Network Control Circuits**
- **Instrumentation**
- **Sensors and Controls**
- **Precision Filters**

3 DESCRIPTIONS

These devices offer low offset and long-term stability by means of a low-noise, chopper-less amplifier circuit. External components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

These devices available in Green SOP8 packages. They operate over an ambient temperature range of -40°C to 125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS07	SOP8	4.90mm×3.90mm
RS07-2	SOP8	4.90mm×3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2024/05/08	Preliminary version completed
A.1	2024/09/27	Initial version completed
A.2	2025/10/30	1. Update Electrical Characteristics and Typical Characteristics 2. Add RS07-2 related information

5 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking (2)	MSL (3)	Package Qty
RS07XK	SOP8	8	1	-40°C ~125°C	RS07	MSL1	Tape and Reel, 4000
RS07-2XK	SOP8	8	2	-40°C ~125°C	RS07-2	MSL1	Tape and Reel, 4000

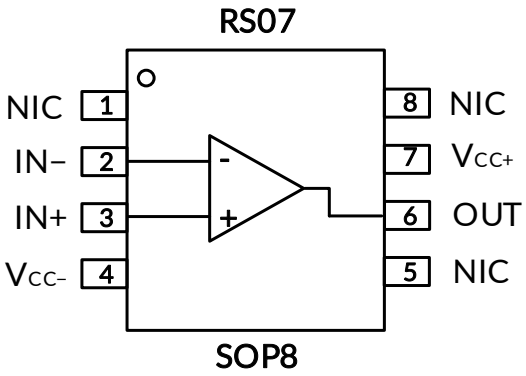
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

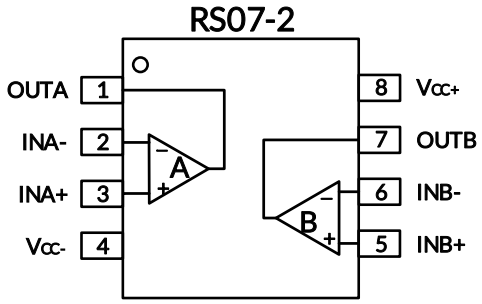
6 PIN CONFIGURATIONS



PIN DESCRIPTION

PIN		I/O (1)	DESCRIPTION
NAME	SOP8		
NIC	1	-	No internal connect
IN-	2	I	Inverting input
IN+	3	I	Noninverting input
V_{CC-}	4	-	Negative supply
NIC	5	-	No internal connect
OUT	6	O	Output
V_{CC+}	7	-	Positive supply
NIC	8	-	No internal connect

(1) I=input, O=output.



PIN DESCRIPTION

PIN		I/O (1)	DESCRIPTION
NAME	SOP8		
INA-	2	I	Inverting input, channel A
INA+	3	I	Noninverting input, channel A
INB-	6	I	Inverting input, channel B
INB+	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
V_{CC-}	4	-	Negative (lowest) power supply or ground (for single supply operation)
V_{CC+}	8	-	Positive (highest) power supply

(1) I=input, O=output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply, V_S=(V+) - (V-)			40	V
	Signal input pin (2)		(V-) - 0.2	(V+) + 0.2	
	Signal output pin (3)		(V-) - 0.2	(V+) + 0.2	
	Differential input voltage		(V-) - (V+)	(V+) - (V-)	
Current	Signal input pin (2)		-10	10	mA
	Signal output pin (3)		-50	50	mA
	Output short-circuits (4)		continuous		
θ_{JA}	Package thermal impedance (5)	SOP8		110	°C/W
Temperature	Operating range, T_A		-40	125	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.2V beyond the supply rails should be current-limited to 10mA or less.

(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.2V beyond the supply rails should be current-limited to ±50mA or less.

(4) Short-circuit to ground, one amplifier per package.

(5) The package thermal impedance is calculated in accordance with JESD-51.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-Body Model (HBM), ANSI/ESDA/JEDEC JS001-2023	±2000	V
	Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1500	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_S= (V+) - (V-)	Single-supply	4.5	36	V
	Dual-supply	±2.25	±18	

7.4 Electrical Characteristics

At T_A = 25°C, V_S= 30V, R_L = 10kΩ, Full [9] = -40°C to 125°C, unless otherwise noted [1]

PARAMETER		CONDITIONS	T_A	MIN[2]	TYP[3]	MAX[2]	UNIT
POWER SUPPLY							
V_S	Operating Voltage Range		Full	4.5		36	V
I_Q	Quiescent Current per Amplifier	V_S = 5V	25°C		1.2	1.4	mA
			Full			1.5	
		V_S = 36V	25°C		1.45	1.65	
			Full			1.9	
PSRR	Power-Supply Rejection Ratio	V_S = 5V to 36V	25°C	100	120		dB
			Full	95			
INPUT							
Vos	Input Offset Voltage	V_S = 30V, V_{CM} = 15V	25°C	-60	±15	60	µV
			Full	-110		110	
Vos Tc	Input Offset Voltage Drift		Full		±0.3		µV/°C
IB	Input Bias Current	V_S = 30V, V_{CM} = 15V	25°C		10	100	pA
I_{OS}	Input Offset Current	V_S = 30V, V_{CM} = 15V	25°C		10	100	pA
A_{OL}	Open-loop Voltage Gain	R_{LOAD} = 10kΩ, V_{OUT} = 0.4V to 29.6V	25°C	115	140		dB
			Full	110			
V_{CM}	Common-Mode Voltage Range		Full	(V-)		(V+)-2	V
CMRR	Common-Mode Rejection Ratio	V_{CM}=0 to 28V	25°C	100	120		dB
			Full	95			
OUTPUT							
V_{OH}	Output Swing from Positive Rail	R_{LOAD} = 10kΩ to V_S/2	25°C		56	150	mV
			Full			200	
V_{OL}	Output Swing from Negative Rail	R_{LOAD} = 10kΩ to V_S/2	25°C		75	150	
			Full			200	
I_{SC}	Short-Circuit Current [6] [7]	Source	25°C	20	40		mA
			Full	8			
		Sink	25°C	10	22		
			Full	6			
AC Specifications							
SR	Slew Rate [8]	G=1, 20V Step	25°C		1.5		V/µs
GBW	Gain-Bandwidth Product		25°C		2.5		MHz
t_S	Settling Time,0.1%	G=1, 10V Step	25°C		8		µs
t_{OR}	Overload Recovery Time		25°C		300		ns
PM	Phase Margin	R_L=10kΩ, C_L= 1nF	25°C		64		°
GM	Gain Margin	R_L=10kΩ, C_L= 1nF	25°C		15		dB
C_{LOAD}	Capacitive Load Drive	A_V=1, no oscillations	25°C		10		nF
NOISE							
En	Input Voltage Noise	V_S = 5V, f = 0.1Hz to 10Hz	25°C		4		µVpp
en	Input Voltage Noise Density [4]	f = 1kHz	25°C		12		nV/$\sqrt{\text{Hz}}$
		f = 10kHz			9		

NOTE:
(1) All unused digital inputs of the device must be held at V_{IO} or GND to ensure proper device operation.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) This parameter is ensured by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
(7) Short circuit test is a momentary test.
(8) Number specified is the slower of positive and negative slew rates.
(9) Specified by characterization only.

7.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

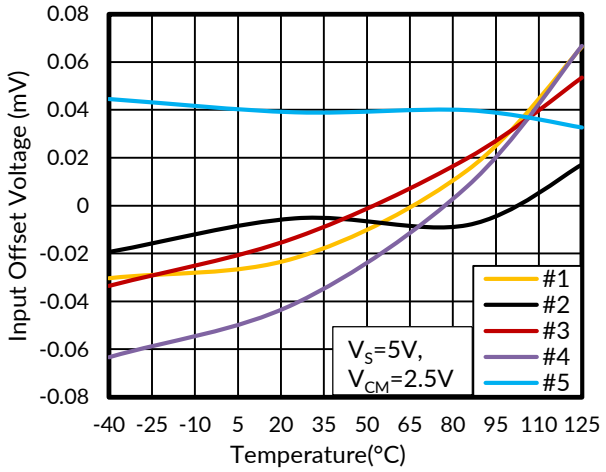


Figure 1. Input Offset Voltage vs Temperature

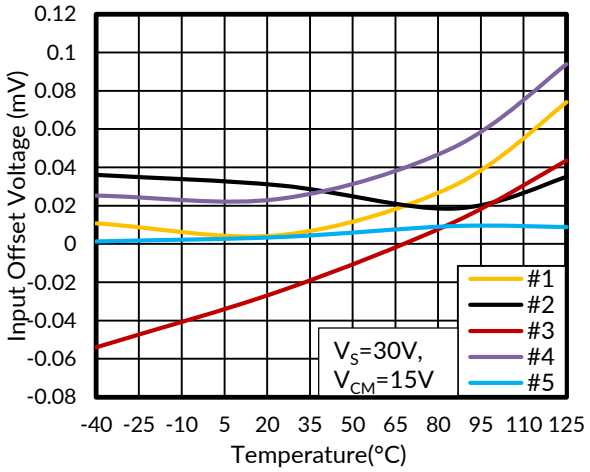


Figure 2. Input Offset Voltage vs Temperature

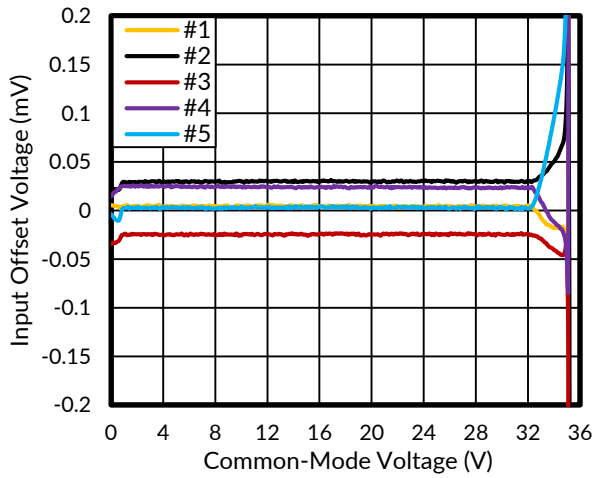


Figure 3. Input Offset Voltage vs Common-Mode Voltage

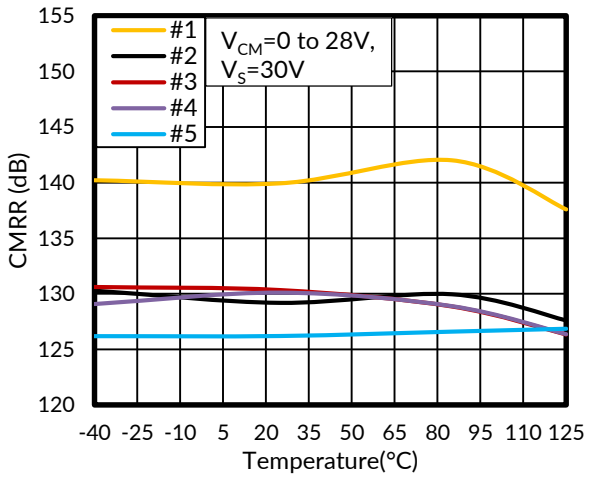


Figure 4. Common-Mode Rejection Ratio vs Temperature

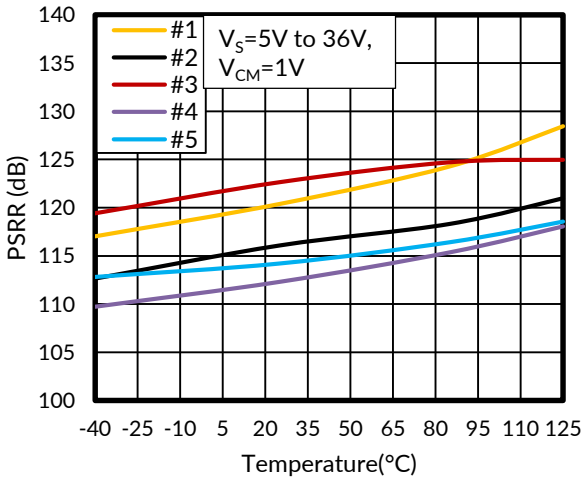


Figure 5. Power-Supply Rejection Ratio vs Temperature

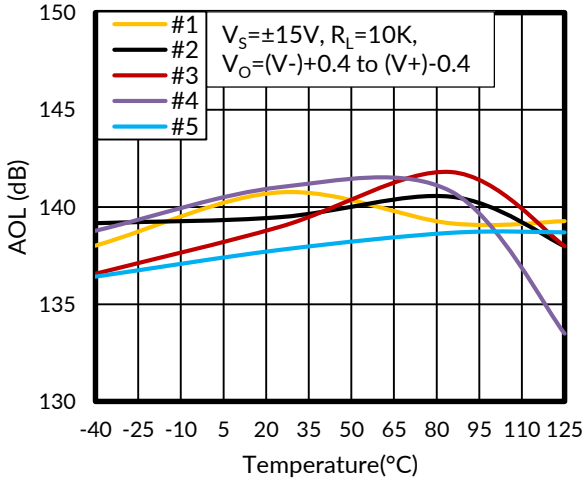


Figure 6. Open-Loop Gain vs Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

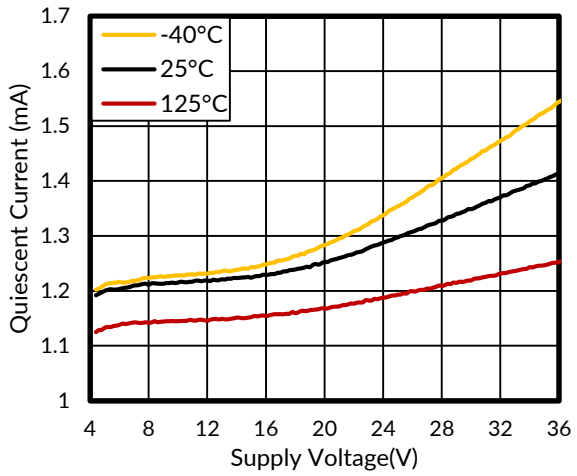


Figure 7. Supply Voltage vs Quiescent Current

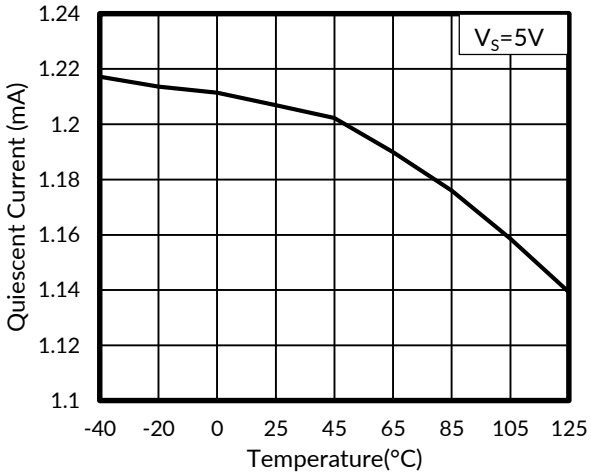


Figure 8. Quiescent Current vs Temperature

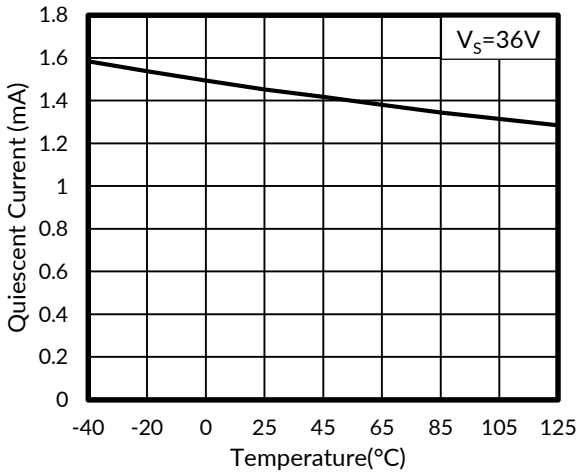


Figure 9. Quiescent Current vs Temperature

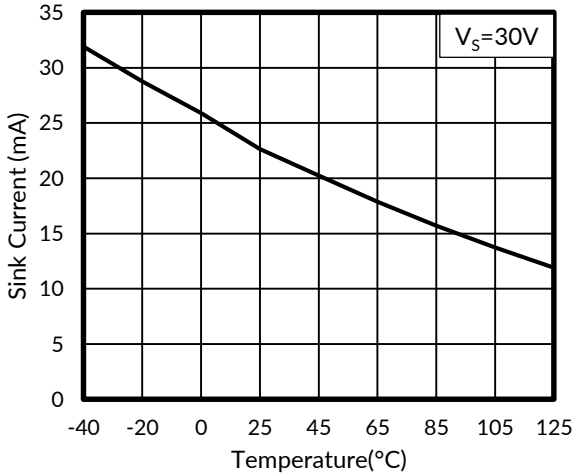


Figure 10. Sink Current vs Temperature

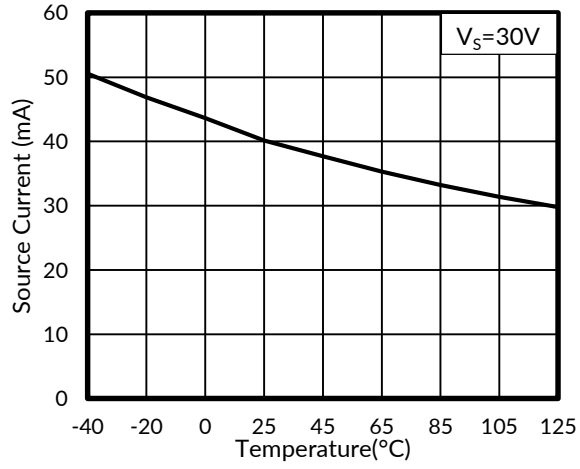


Figure 11. Source Current vs Temperature

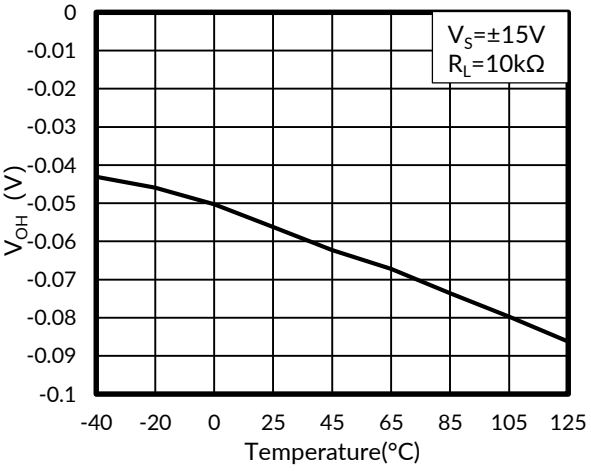


Figure 12. Output Swing from Rail vs Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

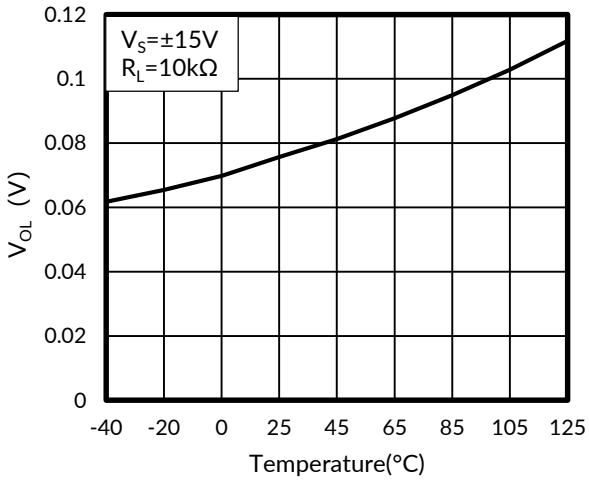


Figure 13. Output Swing from Rail vs Temperature

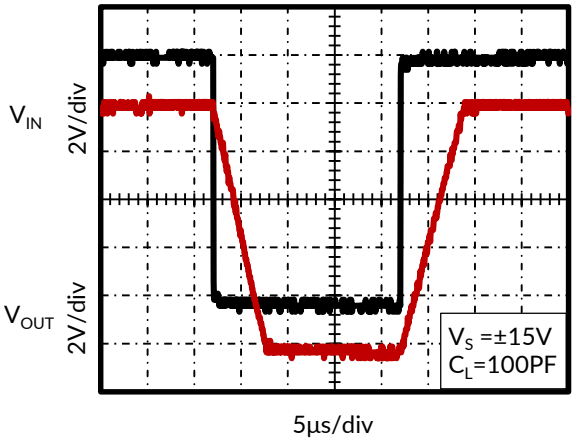


Figure 14. Large-Signal Step Response

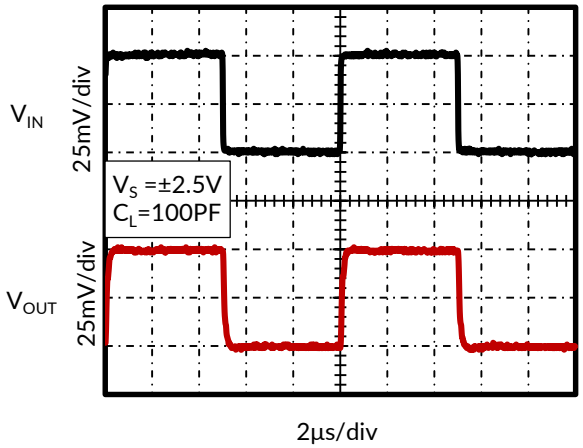


Figure 15. Small-Signal Step Response

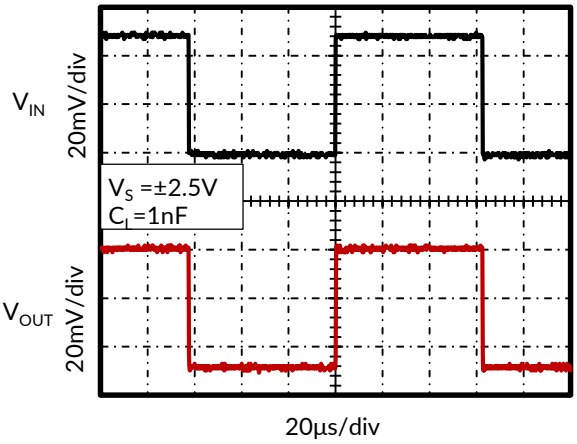


Figure 16. Small-Signal Step Response

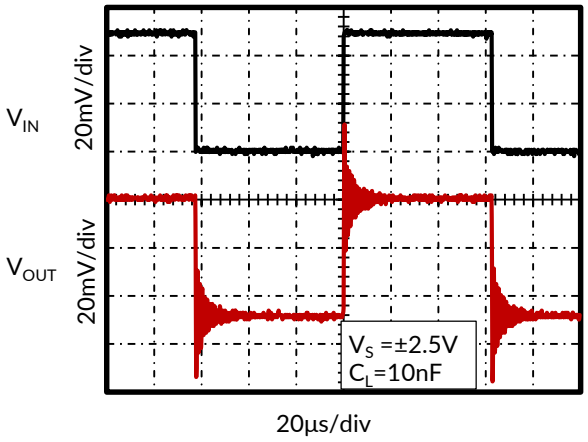


Figure 17. Small-Signal Step Response

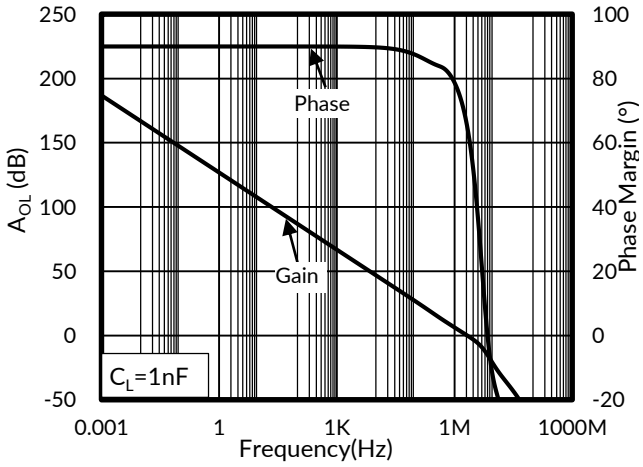


Figure 18. Open−Loop Gain and Phase vs Frequency

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

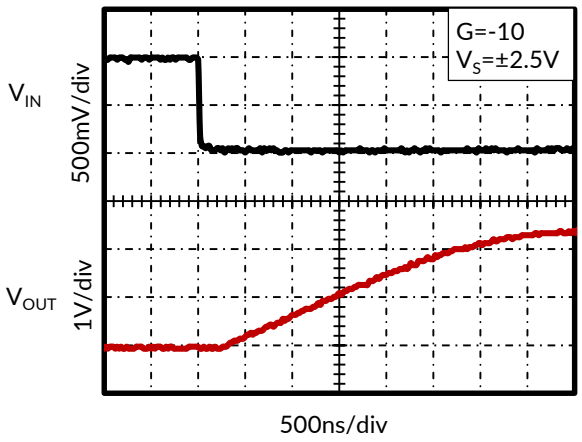


Figure 19. Negative Overload Recovery

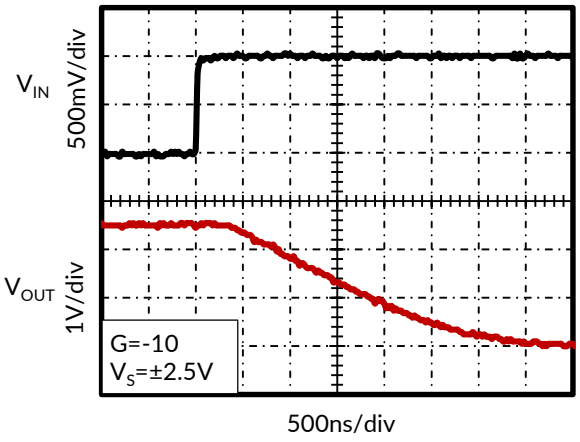


Figure 20. Positive Overload Recovery

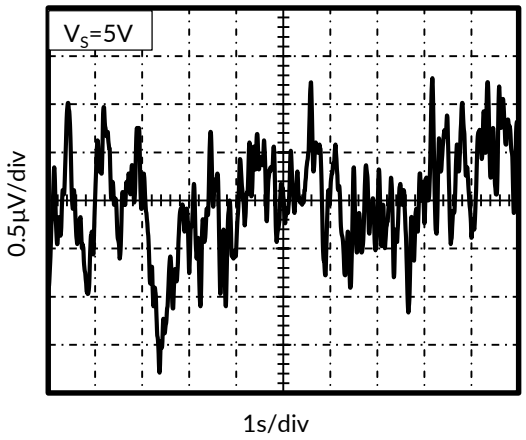


Figure 21. 0.1Hz to 10Hz Input Voltage Noise

8 LAYOUT

8.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. On multilayer PCBs, one or more layers are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicularly, as opposed to in parallel, with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.2 Layout Example

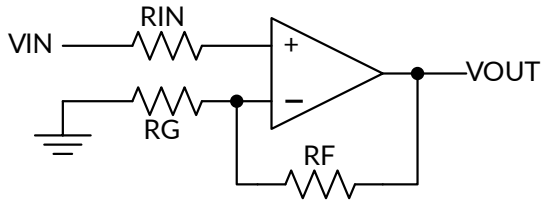


Figure 22. Operational Amplifier Schematic for Noninverting Configuration

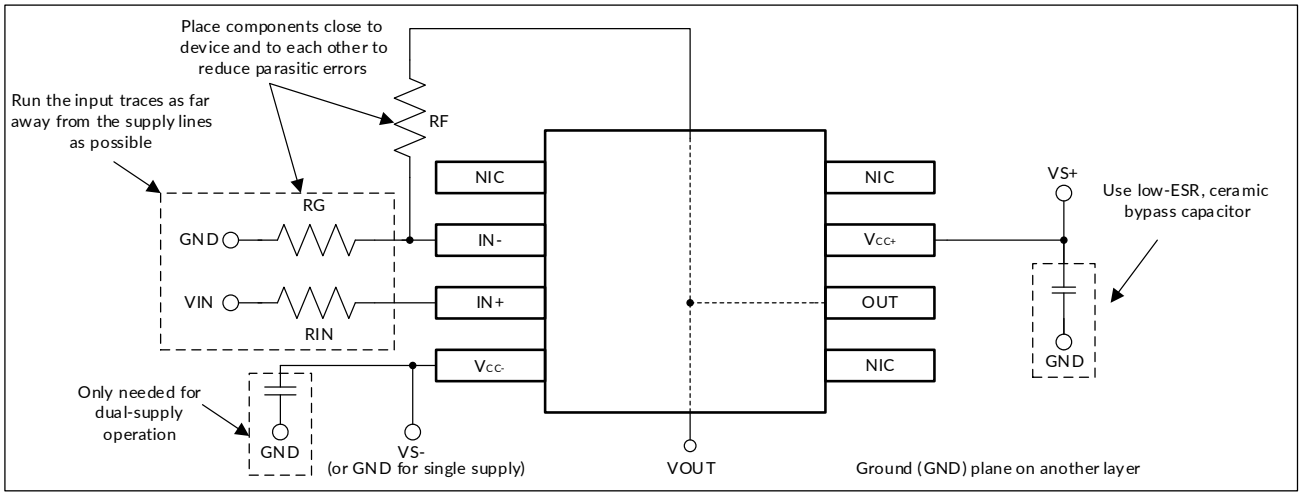
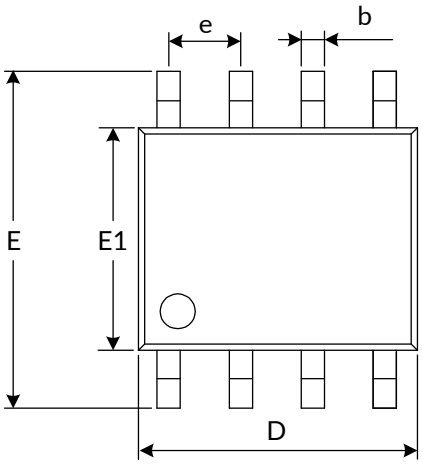
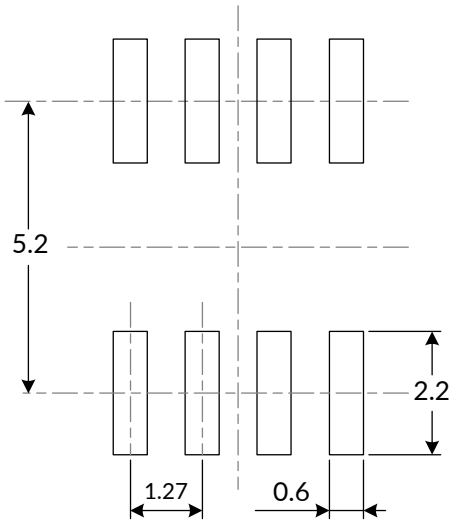


Figure 23. Operational Amplifier Board Layout for Noninverting Configuration

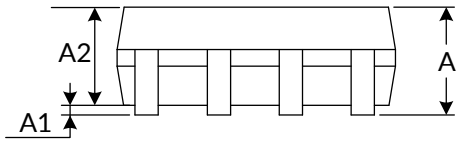
9 PACKAGE OUTLINE DIMENSIONS

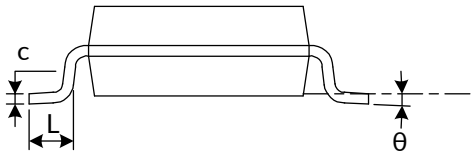
SOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

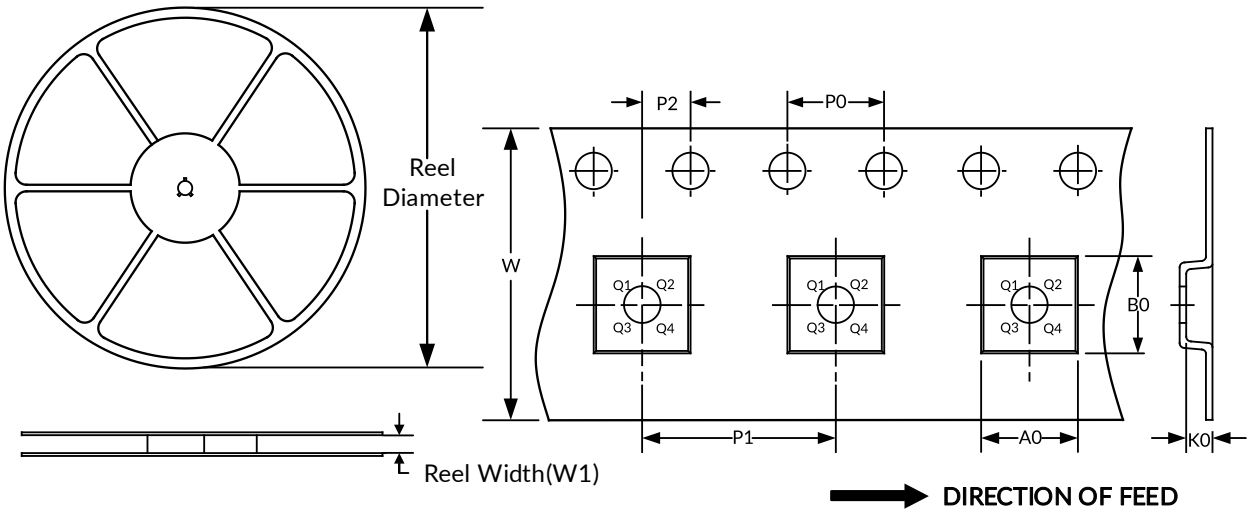
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

10 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOP8	13”	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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