RS1320 12-Bit Micro Power, Digital-to-Analog Converter

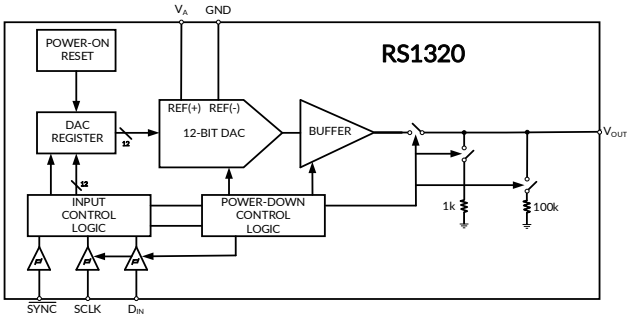
1 FEATURES

- **Ensured Monotonicity**
- **Low Power Operation**
- **Rail-to-Rail Voltage Output**
- **Power-on Reset to Zero Volts Output**
- **Wide Temperature Range of −40°C to +125°C**
- **Wide Power Supply Range of 2.7 V to 5.5 V**
- **Small Packages**
- **Power Down Feature**
- **Resolution: 12 bits**
- **INL: -0.7/1.2 LSB (Typical)**
- **DNL: -0.1/0.2 LSB (Typical)**
- **Zero Code Error: 1.3 mV (Typical)**
- **Full-Scale Error: -0.01 %FS (Typical)**
- **0.48mW (3.6 V) / 1.05mW (5.5 V) Normal Mode Power Consumption (Typical)**
- **0.036 µW (3.6 V) / 0.055 µW (5.5 V) Power-Down Mode (Typical)**

2 APPLICATIONS

- **Battery-Powered Instruments**
- **Digital Gain and Offset Adjustment**
- **Programmable Voltage and Current Sources**
- **Programmable Attenuators**
- **Automotive**

Simplified Block Diagram



3 DESCRIPTIONS

The RS1320 device is a full-featured, general-purpose, 12-bit voltage-output digital-to-analog converter (DAC) that can operate from a single 2.7 V to 5.5 V supply and consumes just 134 µA of current at 3.6 V. The on-chip output amplifier allows rail-to-rail output swing and the three wire serial interface operates at clock rates up to 30 MHz over the specified supply voltage range and is compatible with standard SPI™, QSPI, MICROWIRE and DSP interfaces.

The supply voltage for the RS1320 serves as its voltage reference, providing the widest possible output dynamic range. A power-on reset circuit ensures that the DAC output powers up to zero volts and remains there until there is a valid write to the device. A power-down feature reduces power consumption to less than a microWatt.

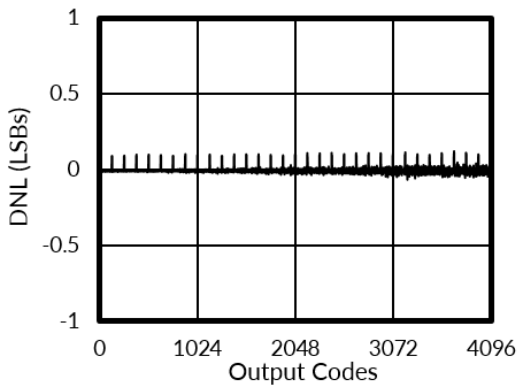
The low power consumption and small packages of the RS1320 make it an excellent choice for use in battery operated equipment.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1320	SOT23-6	1.60 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DNL vs Output Code



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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version

VERSION	Change Date	Change Item
A.0	2025/10/12	Preliminary version completed
A.1	2025/01/14	Initial version completed
A.2	2025/11/18	1、 The upper and lower limits of INL have been changed from ±2.5 to ±3. 2、 The upper and lower limits of DNL have changed from ±0.25 to ±0.4. 3、 The upper and lower limits of FSE have changed from ±0.06 to ±0.09, and the typical values under high and low temperatures have been adjusted from -0.02 to -0.04/+0.02. 4、 The DC Output Impedance has been changed from 1 to 0.5. 5、 The power consumption has been significantly reduced compared to the previous version. 6、 Add specifications for power consumption testing conditions.

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS1320	RS1320XH6	-40°C ~125°C	SOT23-6	1320	MSL1	Tape and Reel, 3000

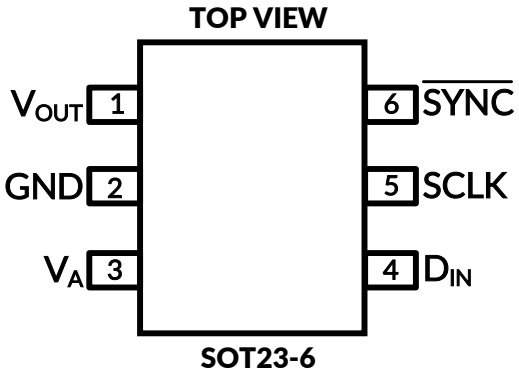
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 PIN CONFIGURATION AND FUNCTIONS



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	SOT NO.		
V_{OUT}	1	Analog Output	Analog Output Voltage
GND	2	Ground	Ground reference for all on-chip circuitry.
V_A	3	Supply	Power supply and Reference input. Should be decoupled to GND.
D_{IN}	4	Digital Input	Serial Data Input. Data is clocked into the 16-bit shift register on the falling edges of SCLK after the fall of $\overline{SYNC}$.
SCLK	5	Digital Input	Serial Clock Input. Data is clocked into the input shift register on the falling edges of this pin.
$\overline{SYNC}$	6	Digital Input	Frame synchronization input for the data input. When this pin goes low, it enables the input shift register and data is transferred on the falling edges of SCLK. The DAC is updated on the 16th clock cycle unless $\overline{SYNC}$ is brought high before the 16th clock, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Supply Voltage, V_A			6.5	V
Voltage on any Input Pin		-0.3	(V_A + 0.3)	V
Input Current at Any Pin (3)			10	mA
Package Input Current (3)			20	mA
Power Consumption at T_A= 25°C		See (4)		
Package thermal impedance, θ_{JA} (5)	SOT23-6		250	°C/W
Storage Temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified

(3) When the input voltage at any pin exceeds the power supplies (that is, less than GND, or greater than V_A), the current at that pin must be limited to 10 mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.

(4) The absolute maximum junction temperature (T_{JMAX}) for this device is 150°C. The maximum allowable power dissipation is dictated by T_{JMAX}, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions must always be avoided.

(5) The package thermal impedance is calculated in accordance with JESD-51.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), ANSI/ESDA/JEDEC JS001-2023	±2000	V
		Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1500	
		Machine Model (MM), JESD22-A115C(2010)	±200	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

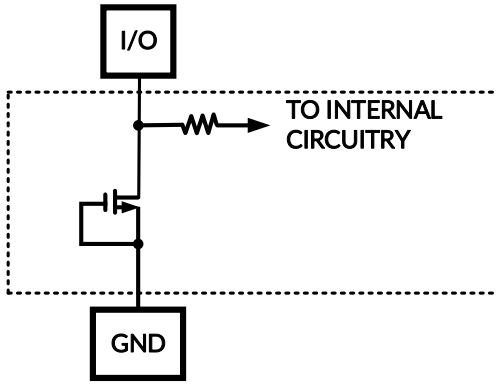
Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating temperature, T_A	−40	125	°C
Supply voltage, V_A	2.7	5.5	V
Any Input Voltage (3)	−0.1	(V_A + 0.1)	V
Output load	0	1500	pF
SCLK Frequency		30	MHz

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified

(3) The analog inputs are protected as shown below. Input voltage magnitudes up to V_A + 300 mV or to 300 mV below GND will not damage this device. However, errors in the conversion result can occur if any input goes above V_A or below GND by more than 100 mV. For example, if V_A is 2.7V_{DC}, ensure that -100mV ≤ input voltages ≤2.8V_{DC} to ensure accurate conversions.



7.4 Electrical Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are for T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(1)	MAX(1)	UNIT
STATIC PERFORMANCE							
Resolution		$T_{MIN} \le T_A \le T_{MAX}$		12			Bits
Monotonicity		$T_{MIN} \le T_A \le T_{MAX}$		12			Bits
INL	Integral Non-Linearity	Over Decimal codes 48 to 4047	T_A = 25°C	-3	-0.7/1.2	3	LSB
			$T_{MIN} \le T_A \le T_{MAX}$		-0.9/1.4		
DNL	Differential Non-Linearity	V_A = 2.7 V to 5.5 V	T_A = 25°C	-0.4	-0.1/0.2	0.4	LSB
			$T_{MIN} \le T_A \le T_{MAX}$		-0.1/0.25		
ZE	Zero Code Error	I_{OUT} = 0	T_A = 25°C		1.3	4	mV
			$T_{MIN} \le T_A \le T_{MAX}$		1.8		
FSE	Full-Scale Error	I_{OUT} = 0	T_A = 25°C	-0.09	-0.01	0.09	%FSR
			$T_{MIN} \le T_A \le T_{MAX}$		-0.04/0.02		
GE	Gain Error	All ones Loaded to DAC register	T_A = 25°C		-0.03		%FSR
			$T_{MIN} \le T_A \le T_{MAX}$		-0.08		
ZCED	Zero Code Error Drift	V_A = 3 V			3.4		µV/°C
		V_A = 5 V			3.7		
TC GE	Gain Error Tempco	V_A = 3 V			-0.6		ppm/°C
		V_A = 5 V			-0.8		
ANALOG OUTPUT CHARACTERISTICS (V_{OUT})							
	Output Voltage Range(2)			0		V_A	V
ZCO	Zero Code Output	V_A = 3 V, I_{OUT} = 10 µA			1.5	3	mV
		V_A = 3 V, I_{OUT} = 100 µA			4	6	
		V_A = 5 V, I_{OUT} = 10 µA			1.6	3	
		V_A = 5 V, I_{OUT} = 100 µA			2.8	6	
FSO	Full Scale Output	V_A = 3 V, I_{OUT} = 10 µA		2.995	2.998		V
		V_A = 3 V, I_{OUT} = 100 µA		2.99	2.994		
		V_A = 5 V, I_{OUT} = 10 µA		4.99	4.998		
		V_A = 5 V, I_{OUT} = 100 µA		4.99	4.996		
Maximum Load Capacitance		R_L = ∞				1500	pF
		R_L = 2 kΩ				1500	
DC Output Impedance					0.5		Ohm
I_{OS}	Output short-circuit current (I_{SOURCE})	V_A = 3 V, V_{OUT} = 0 V, Input Code = FFFh.			-35	-43	mA
		V_A = 5 V, V_{OUT} = 0 V, Input Code = FFFh.			-38	-45	
I_{OS}	Output short-circuit current (I_{SINK})	V_A = 3 V, V_{OUT} = 3 V, Input Code = 000h.			58	71	mA
		V_A = 5 V, V_{OUT} = 5 V, Input Code = 000h.			60	73	
LOGIC INPUT							
I_{IN}	Input Current	$T_{MIN} \le T_A \le T_{MAX}$				±1	µA
V_{IH}	Input High Voltage	V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$		2.1			V
		V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$		2.8			

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are for T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(1)	MAX(1)	UNIT
V_{IL}	Input Low Voltage	V_A = 3 V, $T_{MIN} \le T_A \le T_{MAX}$				0.4	V
		V_A = 5 V, $T_{MIN} \le T_A \le T_{MAX}$				0.6	
C_{IN}	Input Pin Capacitance (2)	$T_{MIN} \le T_A \le T_{MAX}$			4		pF
POWER REQUIREMENTS							
I_A	Supply Current (output unloaded) (3)	Normal Mode V_A = 3.6 V f_{SCLK} = 30 MHz	T_A = 25°C		134		µA
			$T_{MIN} \le T_A \le T_{MAX}$		141		
		Normal Mode V_A = 5.5 V f_{SCLK} = 30 MHz	T_A = 25°C		190		µA
			$T_{MIN} \le T_A \le T_{MAX}$		225		
		Normal Mode V_A = 3.6 V f_{SCLK} = 20 MHz	T_A = 25°C		114		µA
			$T_{MIN} \le T_A \le T_{MAX}$		122		
		Normal Mode V_A = 5.5 V f_{SCLK} = 20 MHz	T_A = 25°C		170		µA
			$T_{MIN} \le T_A \le T_{MAX}$		185		
		Normal Mode f_{SCLK} = 0 MHz	V_A = 3.6 V		93	105	µA
			V_A = 5.5 V		113	131	
		All PD Modes V_A = 3 V f_{SCLK} = 30 MHz	T_A = 25°C		43		µA
			$T_{MIN} \le T_A \le T_{MAX}$		48		
		All PD Modes V_A = 5 V f_{SCLK} = 30 MHz	T_A = 25°C		94		µA
			$T_{MIN} \le T_A \le T_{MAX}$		109		
		All PD Modes V_A = 3 V f_{SCLK} = 20 MHz	T_A = 25°C		29		µA
			$T_{MIN} \le T_A \le T_{MAX}$		32		
		All PD Modes V_A = 5 V f_{SCLK} = 20 MHz	T_A = 25°C		63		µA
			$T_{MIN} \le T_A \le T_{MAX}$		73		
		All PD Modes V_A =3.6 V f_{SCLK} = 0 MHz	T_A = 25°C		0.003		µA
			$T_{MIN} \le T_A \le T_{MAX}$		0.7		
		All PD Modes V_A = 5.5 V f_{SCLK} = 0 MHz	T_A = 25°C		0.006		µA
			$T_{MIN} \le T_A \le T_{MAX}$		1.3		
P_C	Power Consumption (output unloaded) (3)	Normal Mode V_A = 3.6 V f_{SCLK} = 30 MHz	T_A = 25°C		0.48		mW
			$T_{MIN} \le T_A \le T_{MAX}$		0.5		
		Normal Mode V_A = 5.5 V f_{SCLK} = 30 MHz	T_A = 25°C		1.05		mW
			$T_{MIN} \le T_A \le T_{MAX}$		1.24		
		Normal Mode V_A = 3.6 V f_{SCLK} = 20 MHz	T_A = 25°C		0.41		mW
			$T_{MIN} \le T_A \le T_{MAX}$		0.44		
		Normal Mode V_A = 5.5 V f_{SCLK} = 20 MHz	T_A = 25°C		0.93		mW
			$T_{MIN} \le T_A \le T_{MAX}$		1		
		Normal Mode f_{SCLK} = 0 MHz	V_A = 3.6 V		0.34	0.38	mW
			V_A = 5.5 V		0.62	0.72	
		All PD Modes V_A = 3 V f_{SCLK} = 30 MHz	T_A = 25°C		0.13		mW
			$T_{MIN} \le T_A \le T_{MAX}$		0.15		

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are for T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(1)	MAX(1)	UNIT
P_C	Power Consumption (output unloaded) (3)	All PD Modes V_A = 5 V f_{SCLK} = 30 MHz	T_A = 25°C		0.47		mW
			$T_{MIN} \le T_A \le T_{MAX}$		0.54		
		All PD Modes V_A = 3 V f_{SCLK} = 20 MHz	T_A = 25°C		0.09		mW
			$T_{MIN} \le T_A \le T_{MAX}$		0.1		
		All PD Modes V_A = 5 V f_{SCLK} = 20 MHz	T_A = 25°C		0.31		mW
			$T_{MIN} \le T_A \le T_{MAX}$		0.37		
		All PD Modes V_A =3.6 V f_{SCLK} = 0 MHz	T_A = 25°C		0.01	0.42	µW
			$T_{MIN} \le T_A \le T_{MAX}$		2.35		
		All PD Modes V_A = 5.5 V f_{SCLK} = 0 MHz	T_A = 25°C		0.03	0.76	µW
			$T_{MIN} \le T_A \le T_{MAX}$		7		
I_{OUT} / I_A	Power Efficiency	I_{LOAD} = 2 mA	VA = 5 V		95%		
			VA = 3 V		96%		

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(2) This parameter is specified by design and/or characterization and is not tested in production.
(3) The value of this parameter varies with SCLK and $\overline{SYNC}$,The test conditions for this parameter are as follows: when f_{SCLK} = 30 MHz, $f_{\overline{SYNC}}$ = 176 kHz; when f_{SCLK} = 20 MHz, $f_{\overline{SYNC}}$ = 118 KHz.

7.5 AC and Timing Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are for T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK Frequency	$T_{MIN} \le T_A \le T_{MAX}$				30	MHz
ts	Output Voltage Settling Time (1)	400h to C00h code change R_L = 2 kΩ, T_A = 25°C	$C_L \le$ 200 pF		3		µs
			C_L = 500 pF		4		
		00Fh to FF0h code change, R_L = 2 kΩ, T_A = 25°C	$C_L \le$ 200 pF		4		µs
			C_L = 500 pF		6		
SR	Output Slew Rate				1		V/µs
	Glitch Impulse	Code change from 800h to 7FFh			40		nV-sec
	Digital Feedthrough				0.5		nV-sec
t_{WU}	Wake-Up Time	V_A = 3 V			5		µs
		V_A = 5 V			4		
$1/f_{SCLK}$	Serial Clock Frequency	$T_{MIN} \le T_A \le T_{MAX}$		33			ns
t_H	SCLK High time	T_A = 25°C		5			ns
		$T_{MIN} \le T_A \le T_{MAX}$		13			
t_L	SCLK Low Time	T_A = 25°C		5			ns
		$T_{MIN} \le T_A \le T_{MAX}$		13			
t_{SUCL}	Set-up Time $\overline{SYNC}$ to SCLK Rising Edge	T_A = 25°C		-15			ns
		$T_{MIN} \le T_A \le T_{MAX}$		0			

(1) This parameter is specified by design and/or characterization and is not tested in production.

AC and Timing Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, f_{SCLK} = 30 MHz, input code range 48 to 4047. All limits are for T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{SUD}	Data Set-up Time	T_A = 25°C		4			ns
		$T_{MIN} \le T_A \le T_{MAX}$		5			
t_{DHD}	Data Hold Time	T_A = 25°C		4			ns
		$T_{MIN} \le T_A \le T_{MAX}$		5			
t_{CS}	SCLK fall to rise of $\overline{SYNC}$	V_A = 3 V	T_A = 25°C	3			ns
			$T_{MIN} \le T_A \le T_{MAX}$	5			
		V_A = 5 V	T_A = 25°C	3			ns
			$T_{MIN} \le T_A \le T_{MAX}$	5			
$t_{\overline{SYNC}}$	$\overline{SYNC}$ High Time	2.7 ≤ V_A ≤ 3.6	T_A = 25°C	10			ns
			$T_{MIN} \le T_A \le T_{MAX}$	20			
		3.6 ≤ V_A ≤ 5.5	T_A = 25°C	6			ns
			$T_{MIN} \le T_A \le T_{MAX}$	10			

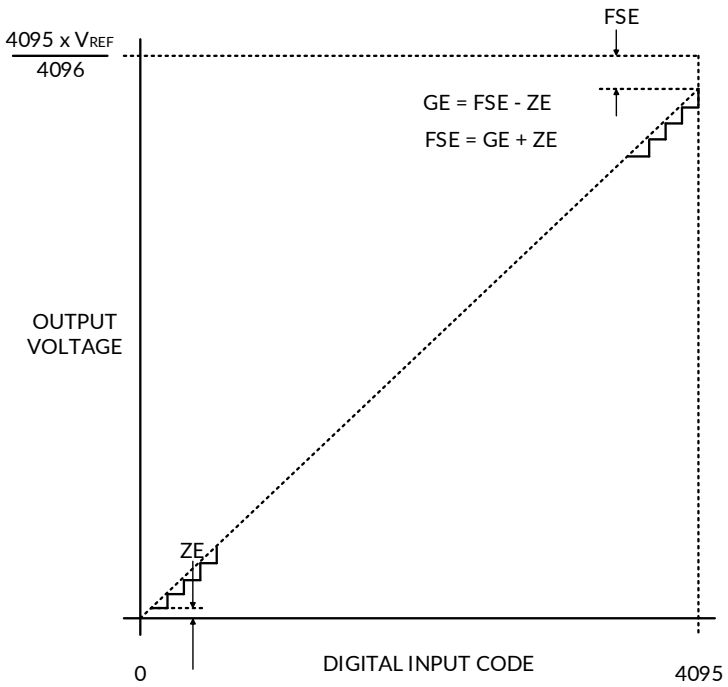


Figure 1. Input / Output Transfer Characteristic

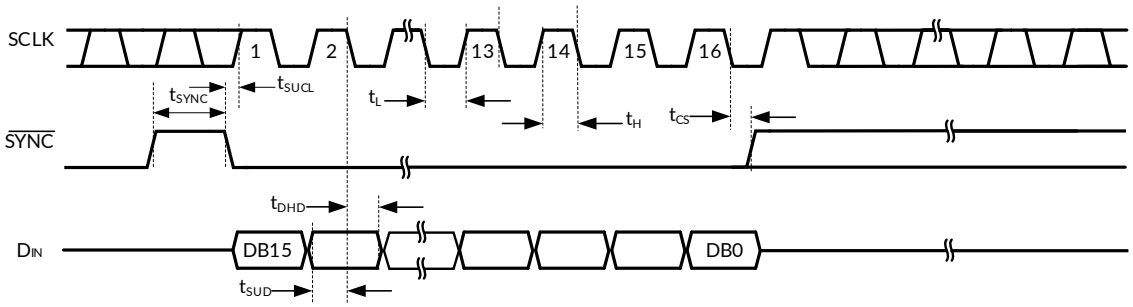


Figure 2. RS1320 Timing

7.6 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

f_{SCLK} = 30 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

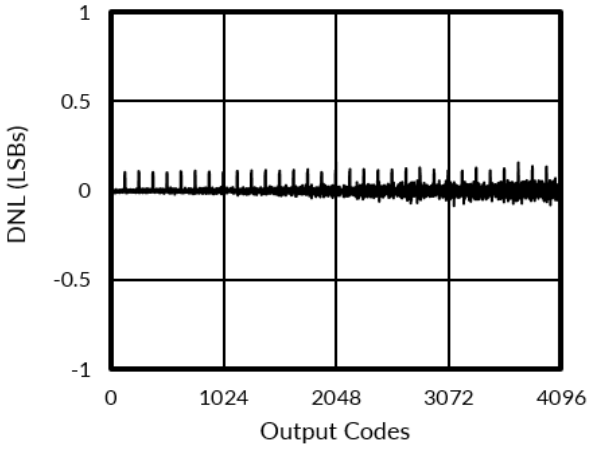


Figure 3. DNL at V_A = 3 V

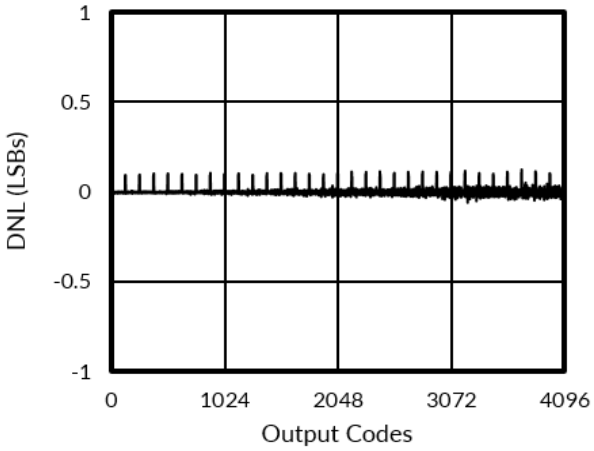


Figure 4. DNL at V_A = 5 V

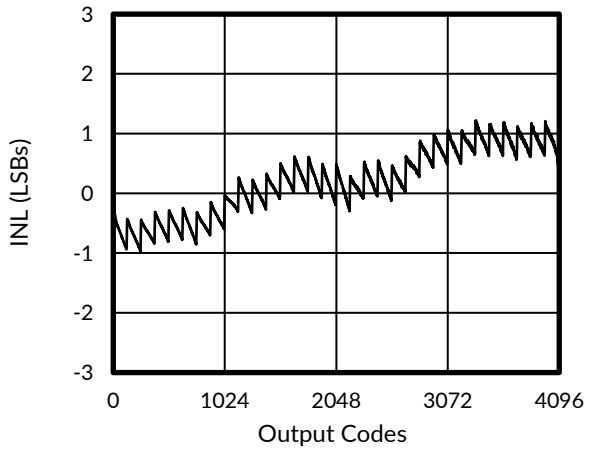


Figure 5. INL at V_A = 3 V

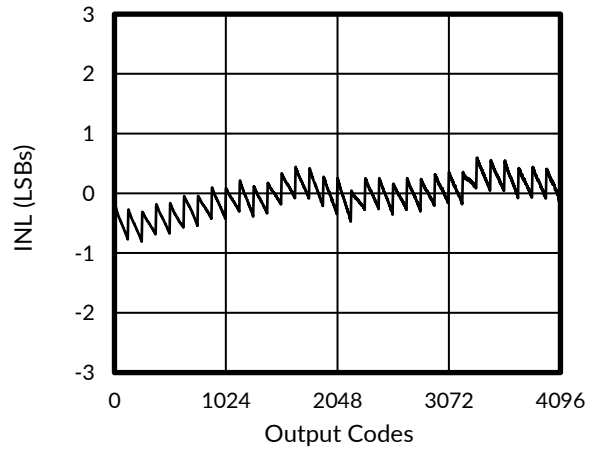


Figure 6. INL at V_A = 5 V

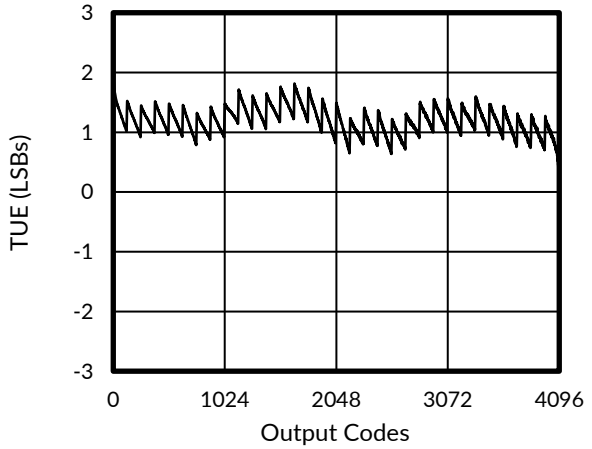


Figure 7. TUE at V_A = 3 V

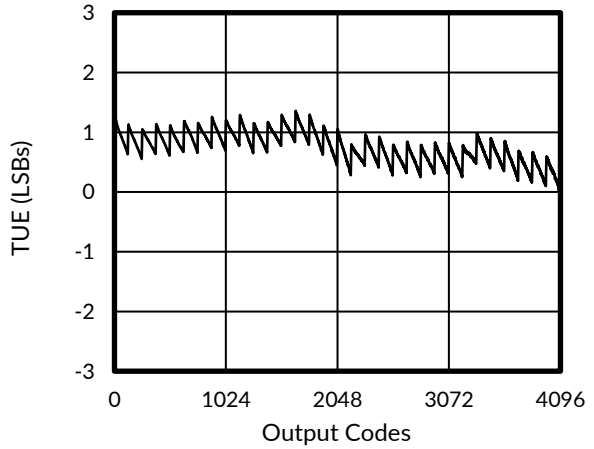


Figure 8. TUE at V_A = 5 V

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

f_{SCLK} = 30 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

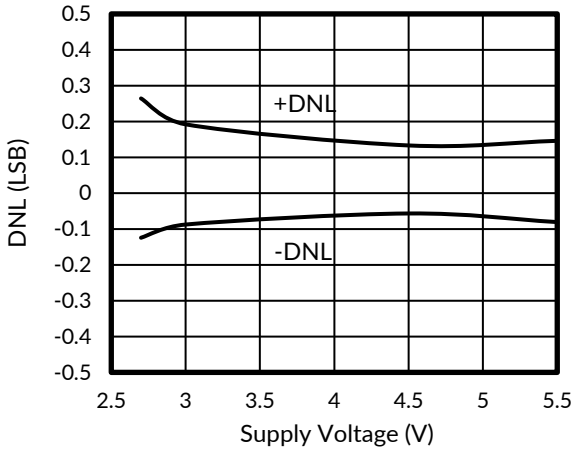


Figure 9. DNL vs V_A

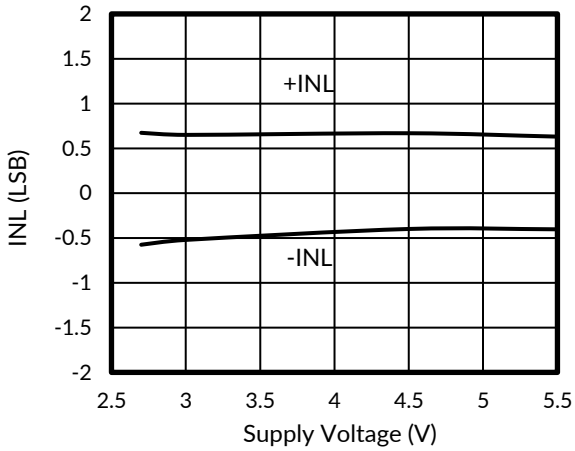


Figure 10. INL vs V_A

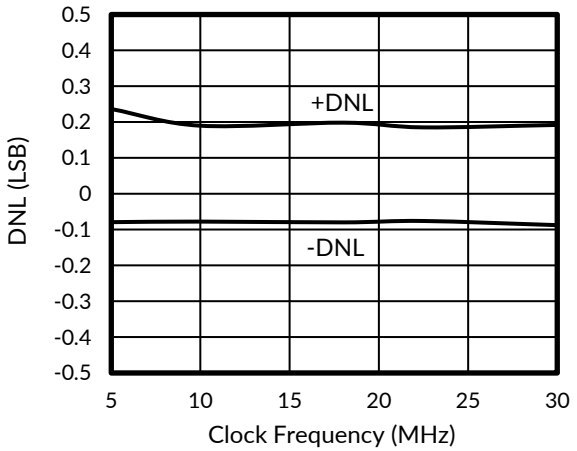


Figure 11. 3V DNL vs f_{SCLK}

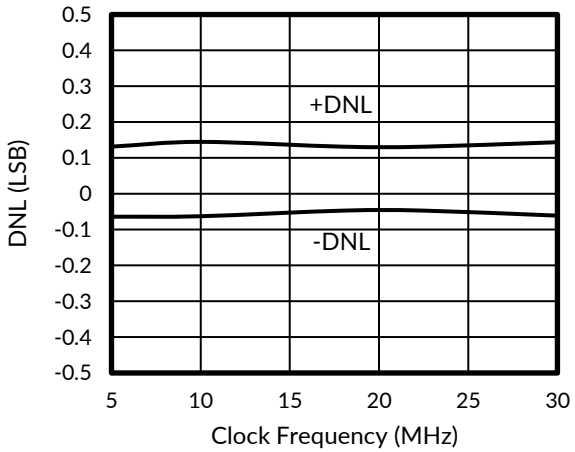


Figure 12. 5V DNL vs f_{SCLK}

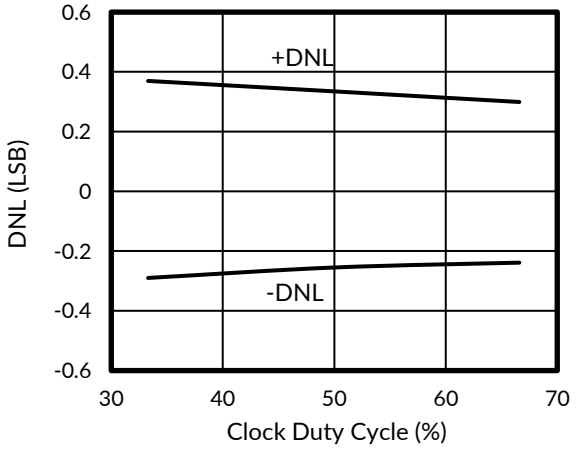


Figure 13. 3V DNL vs Clock Duty Cycle

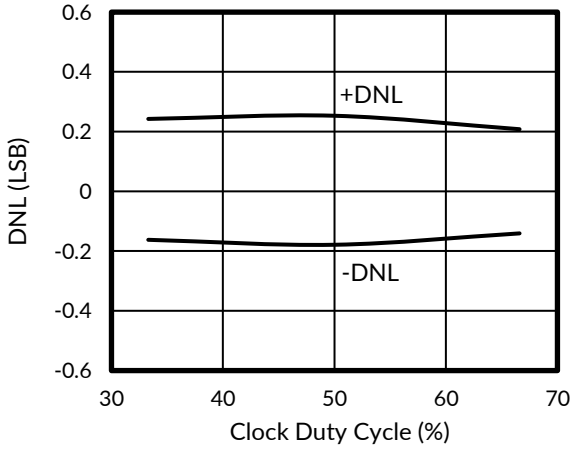


Figure 14. 5V DNL vs Clock Duty Cycle

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

f_{SCLK} = 30 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

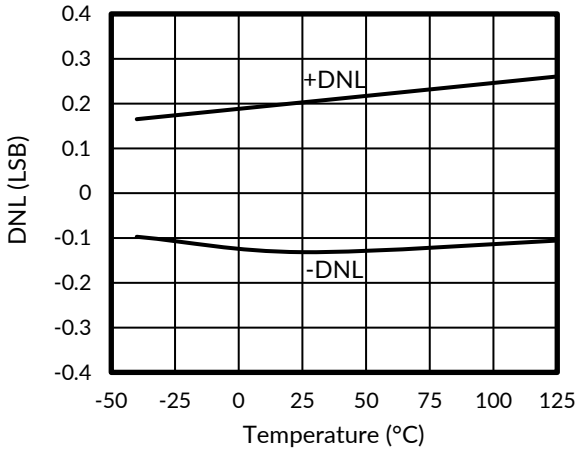


Figure 15. 3V DNL vs Temperature

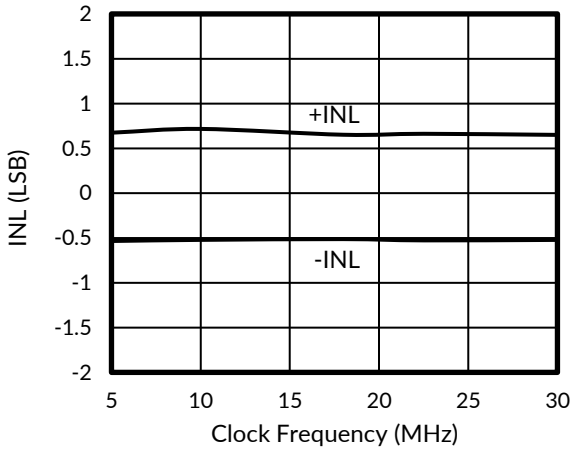


Figure 16. 3V INL at f_{SCLK}

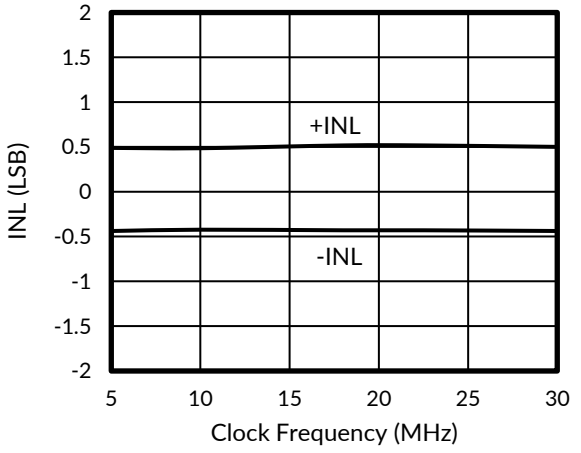


Figure 17. 5V INL at f_{SCLK}

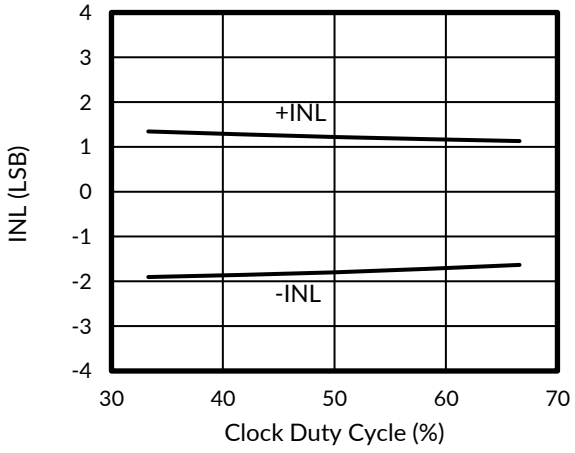


Figure 18. 3V INL at Clock Duty Cycle

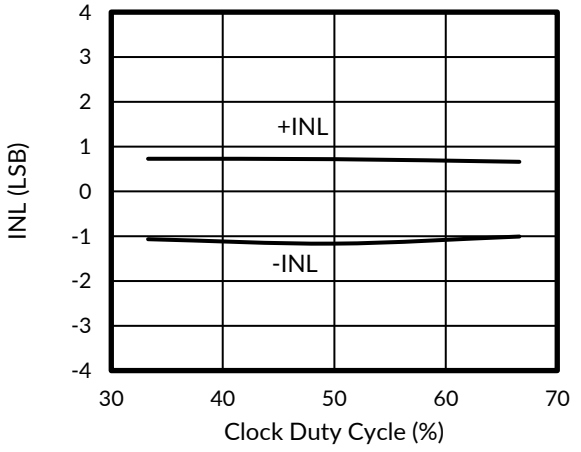


Figure 19. 5V INL vs Clock Duty Cycle

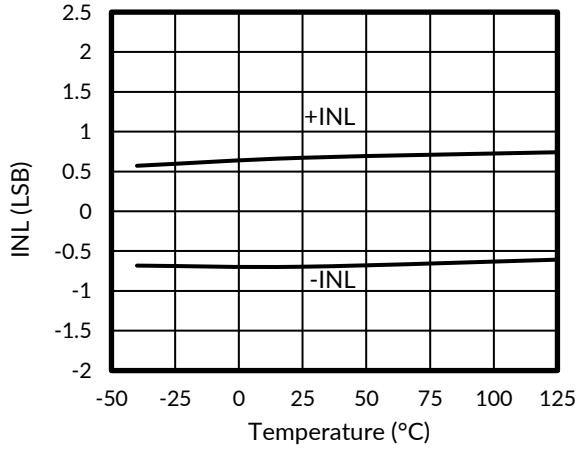


Figure 20. 3V INL vs Temperature

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

f_{SCLK} = 30 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

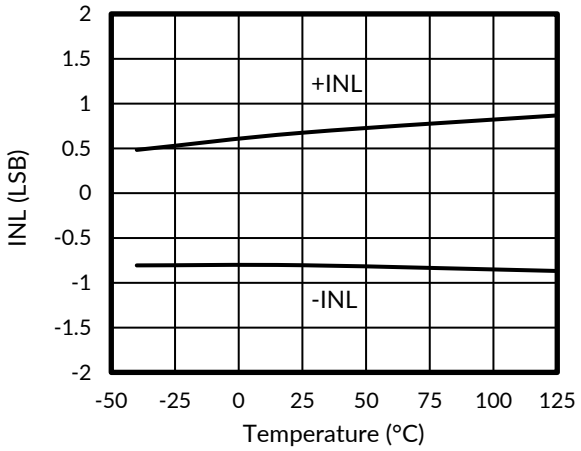


Figure 21. 5V INL vs Temperature

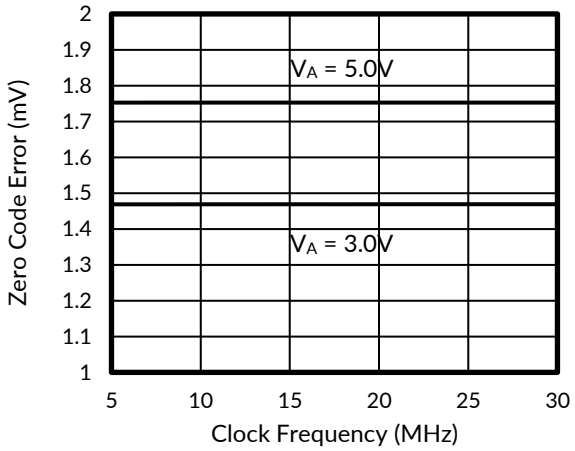


Figure 22. Zero Code Error vs f_{SCLK}

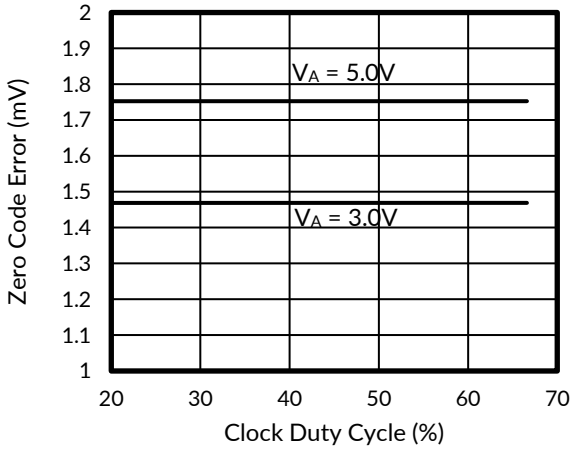


Figure 23. Zero Code Error vs Clock Duty Cycle

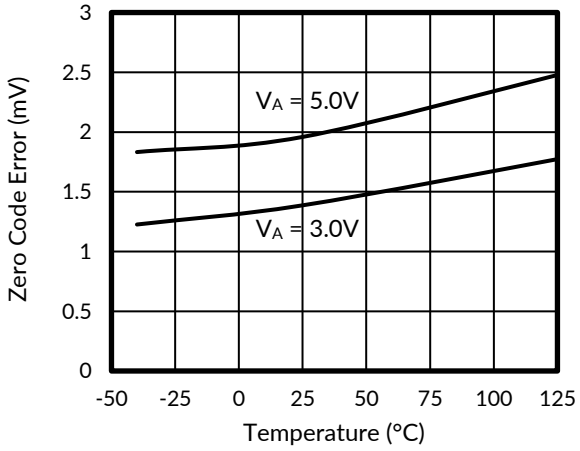


Figure 24. Zero Code Error vs Temperature

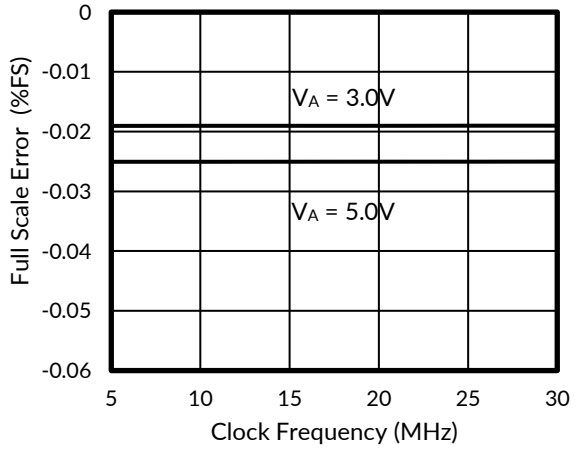


Figure 25. Full-Scale Error vs f_{SCLK}

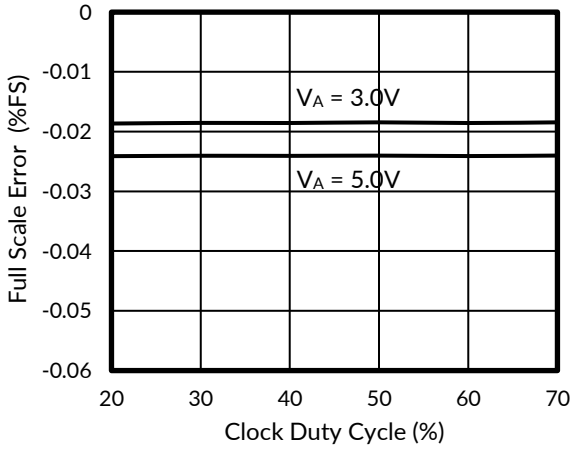


Figure 26. Full-Scale Error vs Clock Duty Cycle

Typical Characteristics (continued)

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

f_{SCLK} = 30 MHz, T_A = 25°C, Input Code Range 48 to 4047, unless otherwise stated.

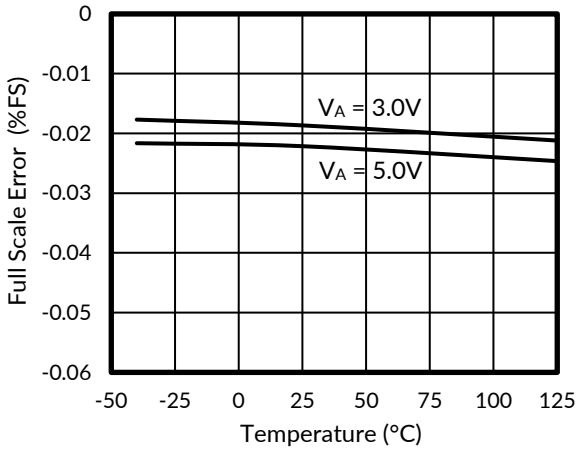


Figure 27. Full-Scale Error vs Temperature

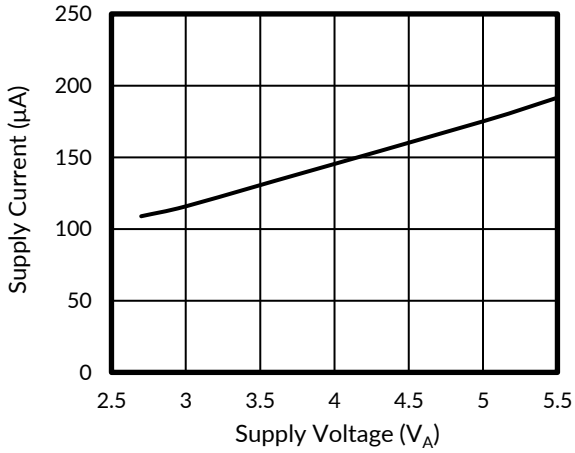


Figure 28. Supply Current vs V_A

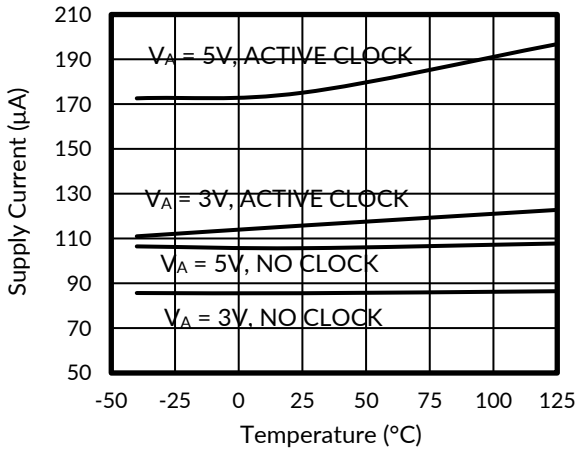


Figure 29. Supply Current vs Temperature

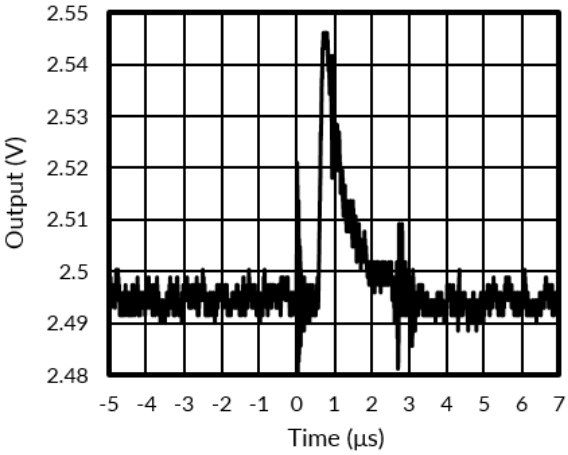


Figure 30. 5V Glitch Response

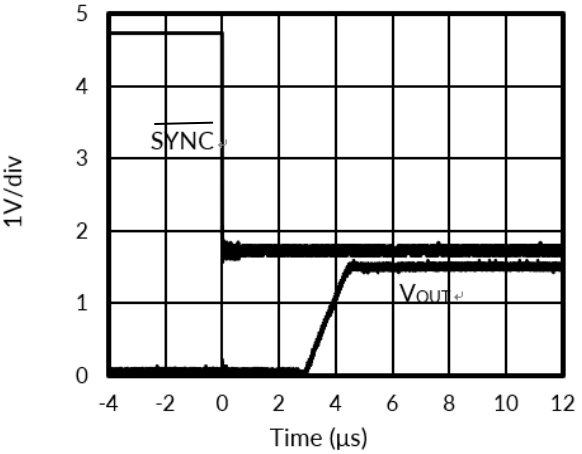


Figure 31. 3V Wake-Up Time

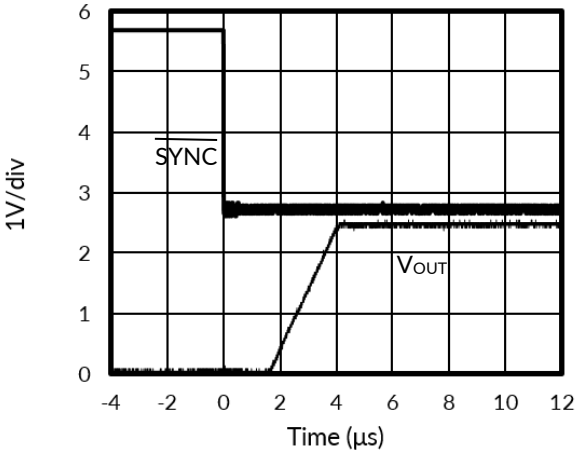


Figure 32. 5V Wake-Up Time

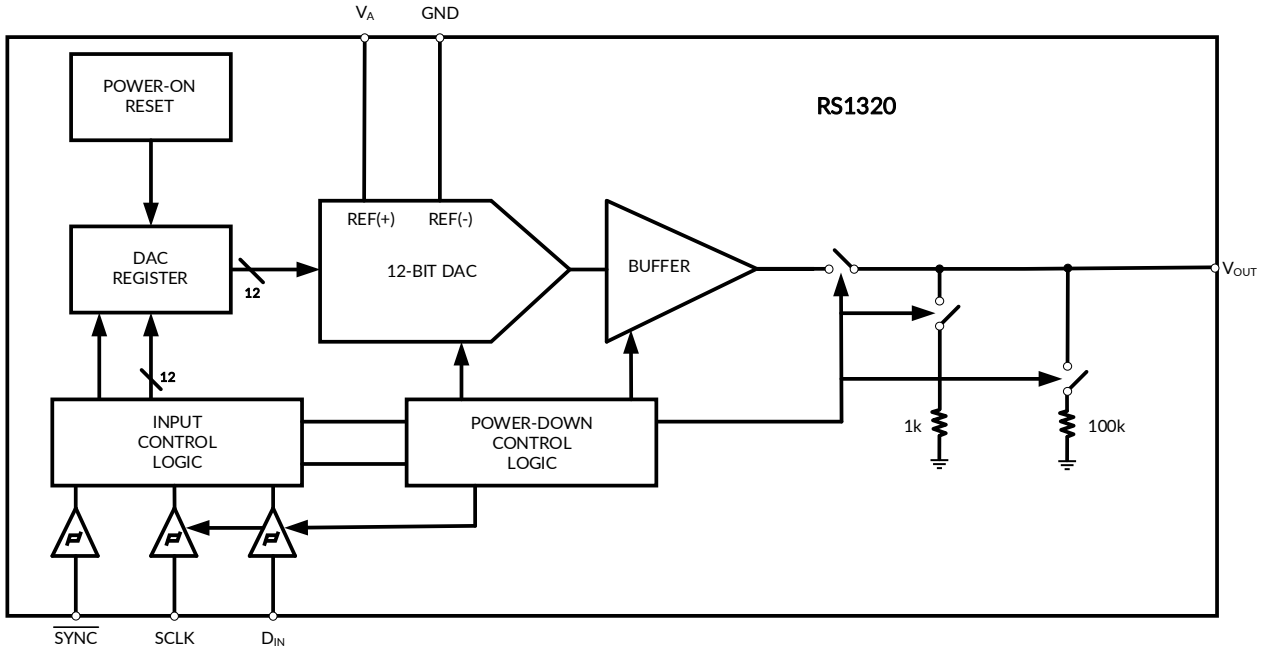
8 DETAILED DESCRIPTION

8.1 Overview

The RS1320 device is a full-featured, general purpose 12-bit voltage-output digital-to-analog converter (DAC) with 6 µs settling time. Control of the output of the DAC is achieved over a 3-wire SPI interface. Once the DAC output has been set, additional communication with the DAC is not required unless the output condition needs to be changed. Likewise, the RS1320 power on state is 0V. The DAC output will remain at 0V until a valid write sequence is made.

A unique benefit of the RS1320 is the logic levels of the SPI™ input pins. The logic levels of SCLK, D_{IN}, and $\overline{SYNC}$ are independent of V_A. This feature is advantageous in applications where the analog circuitry is being run at 5V in order to maximize signal-to-noise ratio and digital logic is running at 3V in order to conserve power.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DAC Section

The RS1320 is fabricated on a CMOS process with an architecture that consists of switches and a resistor string that are followed by an output buffer. The power supply serves as the reference voltage. The input coding is straight binary with an ideal output voltage of:

$$V_{OUT} = V_A \times (D / 4096) \quad (1)$$

where

- D is the decimal equivalent of the binary code that is loaded into the DAC register and can take on any value between 0 and 4095.

8.3.2 Resistor String

The resistor string is shown in Figure 33. This string consists of 4096 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. This configuration ensures that the DAC is monotonic.

Feature Description (continued)

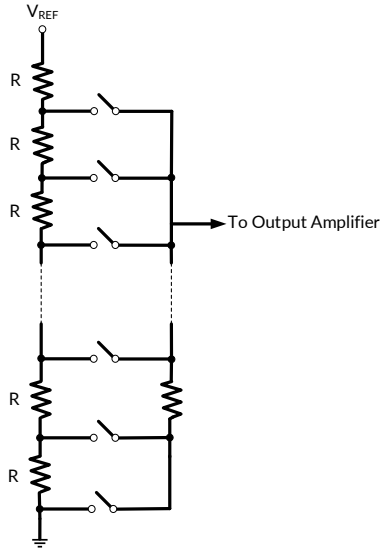


Figure 33. DAC Resistor String

8.3.3 Output Amplifier

The output buffer amplifier is a rail-to-rail type, providing an output voltage range of 0V to V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. The output capabilities of the amplifier are described in the Electrical Characteristics.

8.4 Device Functional Modes

8.4.1 Power-Down Modes

The power-on reset circuit controls the output voltage during power-up. Upon application of power the DAC register is filled with zeros and the output voltage is 0V and remains there until a valid write sequence is made to the DAC.

8.4.2 Power-Down Modes

The RS1320 has four modes of operation. These modes are set with two bits (DB13 and DB12) in the control register.

Table 1. Modes of Operation

DB13	DB12	OPERATING MODE
0	0	Normal Operation
0	1	Power-Down with 1kΩ to GND
1	0	Power-Down with 100kΩ to GND
1	1	Power-Down with Hi-Z

When both DB13 and DB12 are 0, the device operates normally. For the other three possible combinations of these bits the supply current drops to its power-down level and the output are pulled down with either a 1 kΩ or a 100 KΩ resistor, or is in a high-impedance state, as described in Table 1.

The bias generator, output amplifier, the resistor string and other linear circuitry are all shut down in any of the power-down modes. However, the contents of the DAC register are unaffected when in power-down, so when coming out of power down the output voltage returns to the same voltage it was before entering power down.

Minimum power consumption is achieved in the power-down mode with SCLK disabled and $\overline{SYNC}$ and D_{IN} idled low. The time to exit power-down (Wake-Up Time) is typically t_{WU} µsec as stated in the A.C. and Timing Characteristics Table.

8.5 Programming

8.5.1 Serial Interface

The three-wire interface is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs. See the Timing Diagram for information on a write sequence.

A write sequence begins by bringing the $\overline{SYNC}$ line low. Once $\overline{SYNC}$ is low, the data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. On the 16th falling clock edge, the last data bit is clocked in and the programmed function (a change in the mode of operation and/or a change in the DAC register contents) is executed. At this point the $\overline{SYNC}$ line may be kept low or brought high. In either case, it must be brought high for the minimum specified time before the next write sequence as a falling edge of $\overline{SYNC}$ can initiate the next write cycle.

Since the $\overline{SYNC}$ and D_{IN} buffers draw more current when they are high, they must be idled low between write sequences to minimize power consumption.

8.5.2 Input Shift Register

The input shift register, has sixteen bits. The first two bits are don't cares and are followed by two bits that determine the mode of operation (normal mode or one of three power-down modes). The contents of the serial input register are transferred to the DAC register on the sixteenth falling edge of SCLK. See Figure 34.

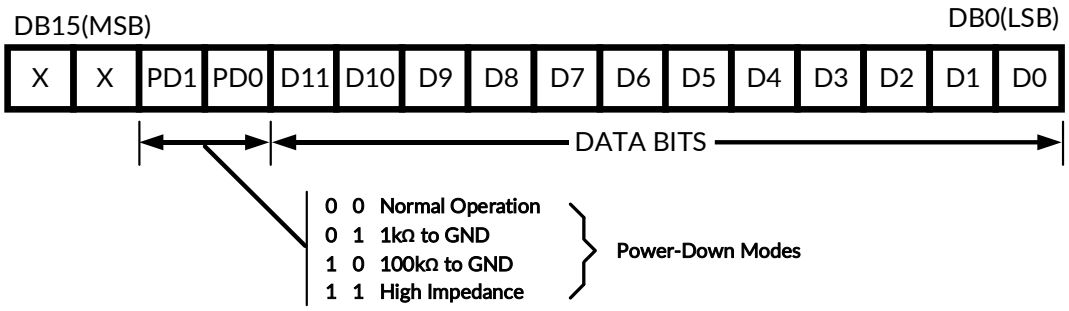


Figure 34. Input Register Contents

Normally, the $\overline{SYNC}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th SCLK falling edge. However, if $\overline{SYNC}$ is brought high before the 16th falling edge, the shift register is reset and the write sequence is invalid. The DAC register is not updated and there is no change in the mode of operation or in the output voltage.

9 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 DSP and Microprocessor Interfacing

The simplicity of the RS1320 implies ease of use. However, it is important to recognize that any data converter that uses its supply voltage as its reference voltage will have essentially zero PSRR (power supply rejection ratio). Therefore, it is necessary to provide a noise-free supply voltage to the device.

Interfacing the RS1320 to microprocessors and DSPs is quite simple. The following guidelines are offered to hasten the design process.

9.1.1.1 ADSP-2101/ADSP-2103 Interfacing

Figure 35 shows a serial interface between the RS1320 and the ADSP-2101/ADSP-2103. The DSP must be set to operate in the SPORT Transmit Alternate Framing Mode. It is programmed through the SPORT control register and must be configured for Internal Clock Operation, Active Low Framing and 16-bit Word Length. Transmission is started by writing a word to the Tx register after the SPORT mode has been enabled.

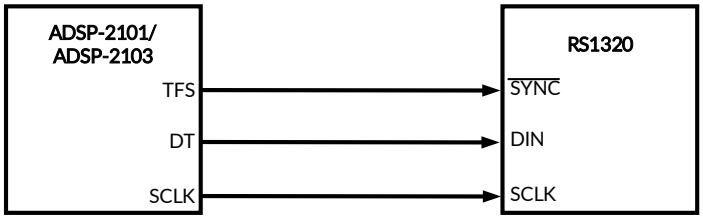


Figure 35. ADSP-2101/2103 Interface

9.1.1.2 80C51/80L51 Interface

A serial interface between the RS1320 and the 80C51/80L51 microcontroller is shown in Figure 36. The $\overline{\text{SYNC}}$ signal comes from a bit-programmable pin on the microcontroller. The example shown here uses port line P3.3. This line is taken low when data is to transmitted to the RS1320. Because the 80C51/80L51 transmits 8-bit bytes, only eight falling clock edges occur in the transmit cycle. To load data into the DAC, the P3.3 line must be left low after the first eight bits are transmitted. A second write cycle is initiated to transmit the second byte of data, after which port line P3.3 is brought high. The 80C51/80L51 transmit routine must recognize that the 80C51/80L51 transmits data with the LSB first while the RS1320 requires data with the MSB first.

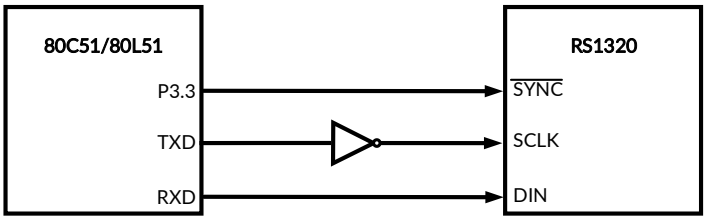


Figure 36. 80C51/80L51 Interface

9.1.2 Bipolar Operation

The RS1320 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in Figure 37. This circuit will provide an output voltage range of ±5 V. A rail-to-rail amplifier must be used if the amplifier supplies are limited to ±5 V.

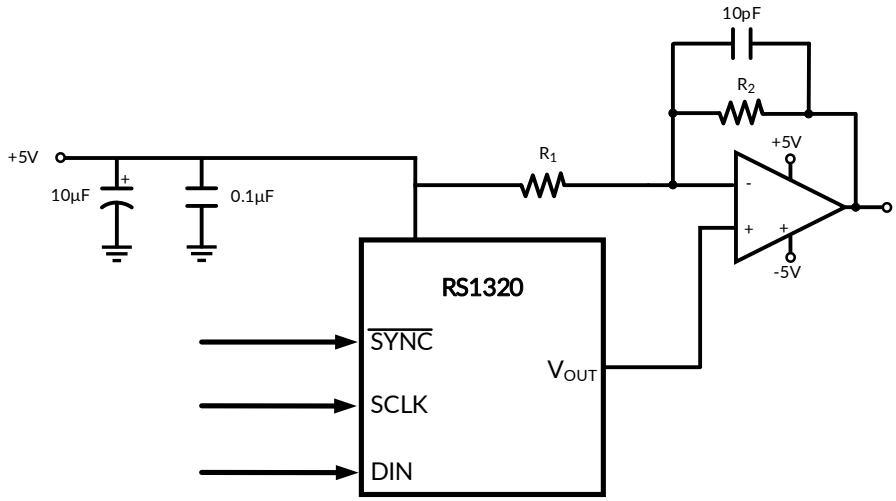


Figure 37. Bipolar Operation

The output voltage of this circuit for any code is found to be

$$V_O = (V_A \times (D / 4096) \times ((R1 + R2) / R1) - V_A \times R2 / R1$$

where

- D is the input code in decimal form. (2)

With V_A = 5 V and R1 = R2,

$$V_O = (10 \times D / 4096) - 5\ V \quad (3)$$

10 LAYOUT

10.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The power applied to V_A must be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. As with the GND connection, V_A must be connected to a power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point.

The RS1320 power supply must be bypassed with a 10 µF and a 0.1 µF capacitor as close as possible to the device with the 0.1 µF right at the device supply pin. The 10 µF capacitor must be a tantalum type and the 0.1 µF capacitor must be a low ESL, low ESR type. The power supply for the RS1320 must only be used for analog circuits.

For best accuracy and minimum noise, the printed-circuit-board containing the RS1320 must have separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes must be located in the same board layer. There must be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will use a fencing technique to prevent the mixing of analog and digital ground current. Separate ground planes must only be used when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the RS1320. Take special care to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. The clock and data lines must have controlled impedances.

10.2 Layout Example

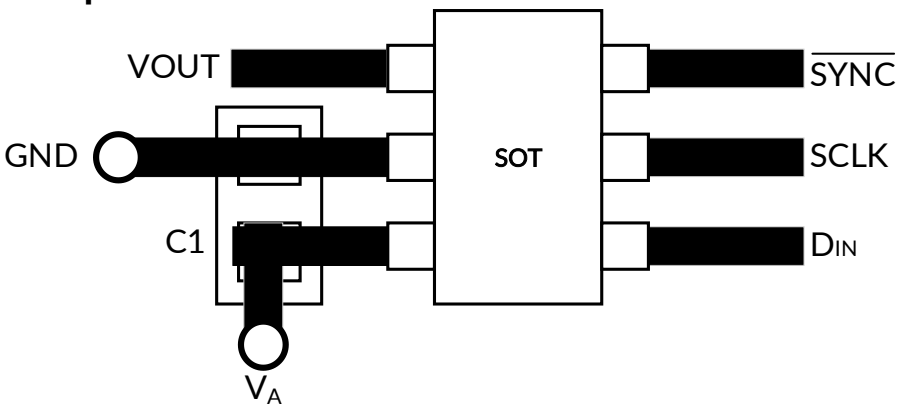
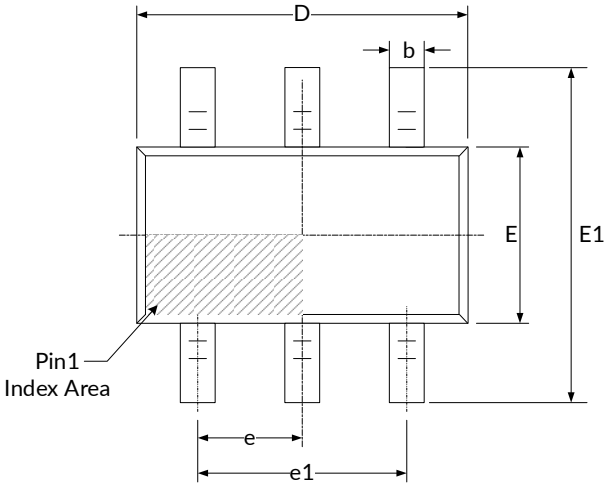
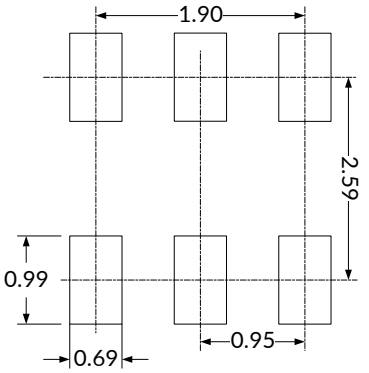


Figure 38. Typical Layout

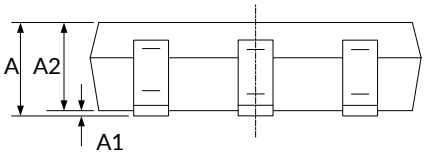
11 PACKAGE OUTLINE DIMENSIONS

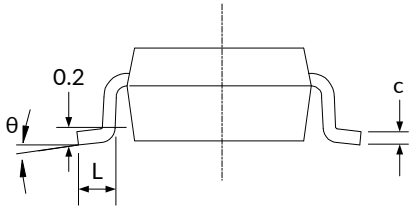
SOT23-6 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

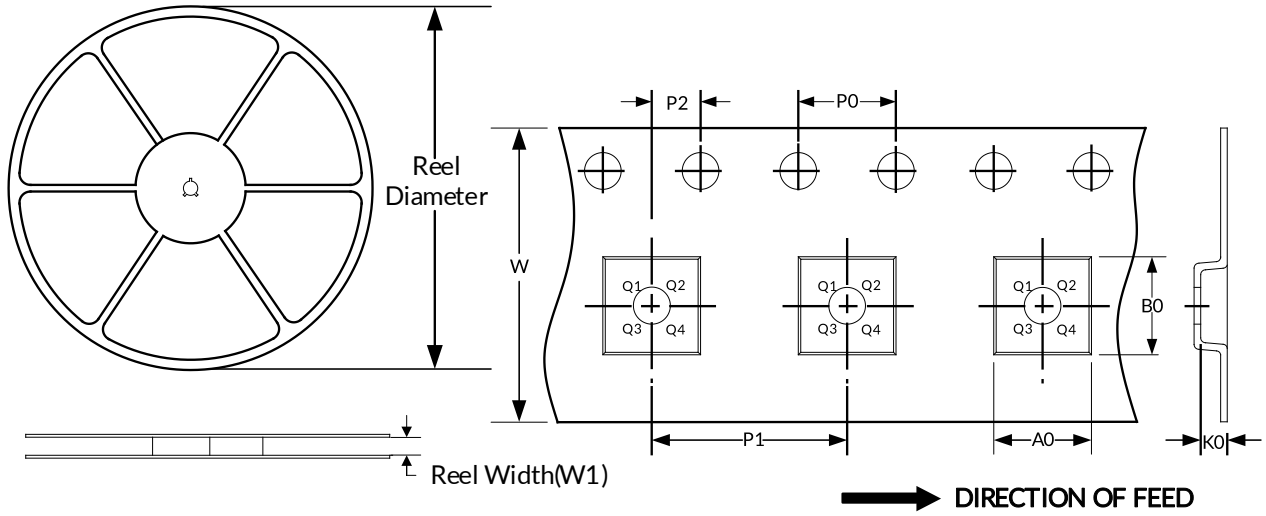
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-6	7”	9.5	3.17	3.23	1.37	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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