12-Bit, 1MSPS, 16-Channel, Single-Ended, Serial Interface ADC

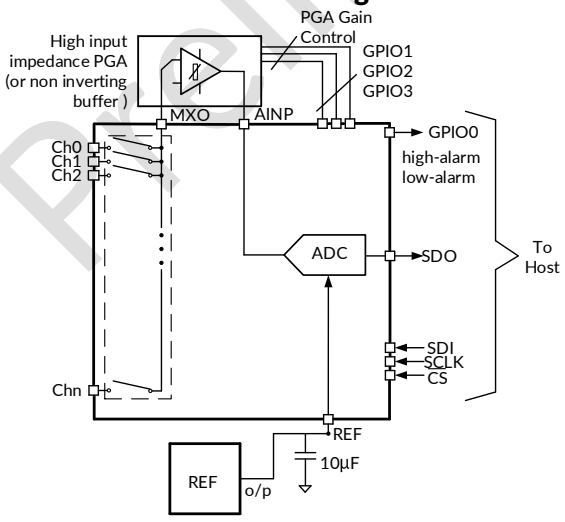
1 FEATURES

- **1MHz Sampling Rate Serial Device**
- **12-bit Resolution Product Series**
- **Zero Latency**
- **20MHz Serial Interface**
- **Analog Power Supply Range: 2.7V to 5.25V**
- **I/O Power Supply Range: 1.7V to 5.25V**
- **Two SW Selectable Unipolar, Input Ranges: 0 to V_{REF} and 0 to 2 x V_{REF}**
- **Auto and Manual Modes for Channel Selection**
- **Two Programmable Alarm Levels per Channel**
- **Four Independently Configurable GPIOs**
- **Power-Down Current: 1μA (TYP)**
- **Input Bandwidth: 20 MHz at -3 dB**

2 APPLICATIONS

- **PLC/IPC**
- **Optical Line Card Monitoring**
- **Medical Instruments**
- **Digital Power Supply**
- **Multi-Channel General Signal Monitoring**
- **High-Speed Data Acquisition System**
- **High-Speed Closed-Loop System**

Detailed Block Diagram



3 DESCRIPTIONS

The RS1467 is a 12-bit multi-channel analog-to-digital converter. The device includes a capacitor based SAR A/D converter with inherent sample and hold.

The RS1467 device accepts a wide analog supply range from 2.7V to 5.25V. Very low power consumption makes the device suitable for battery-powered and isolated power-supply applications.

A wide 1.7V to 5.25V I/O supply range facilitates a glueless interface with the most commonly used digital hosts. The serial interface is controlled by $\overline{CS}$ and SCLK for easy connection with microprocessors and DSP.

The input signal is sampled with the falling edge of $\overline{CS}$. It uses SCLK for conversion, serial data output, and reading serial data in. The device allows auto sequencing of preselected channels or manual selection of a channel for the next conversion cycle.

There are two software selectable input ranges (0 V to V_{REF} and 0 V to 2 × V_{REF}), individually configurable GPIOs (four in case of the TSSOP package devices), and two programmable alarm thresholds per channel. These features make the devices suitable for most data acquisition applications.

This RS1467 offers an attractive power-down feature. This feature is very helpful for energy saving when the device operates at a lower conversion speed.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS1467	TSSOP38	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2025/10/15	Preliminary version completed

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL (3)	PACKAGE OPTION
RS1467	RS1467XTSS38	-40°C ~ 125°C	TSSOP38	RS1467	MSL3	Tape and Reel, 4000

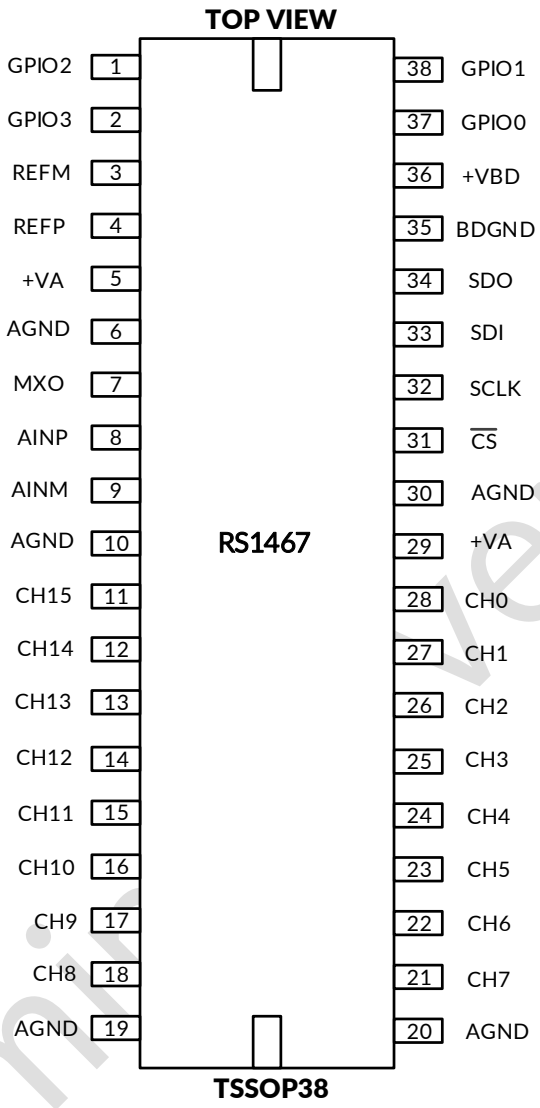
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

6 PIN CONFIGURATION AND FUNCTIONS



Pin Functions

NAME	PIN	I/O	DESCRIPTION
REFERENCE			
REFP	4	Analog input	Reference input
REFM	3	Analog input	Reference ground
ADCANALOGINPUT			
AINP	8	Analog input	ADC input signal
AINM	9	Analog input	ADC input ground
MULTIPLEXER			
MXO	7	Analog output	Multiplexer output
Ch0	28	Analog input	Analog channel for multiplexer
Ch1	27	Analog input	Analog channel for multiplexer
Ch2	26	Analog input	Analog channel for multiplexer
Ch3	25	Analog input	Analog channel for multiplexer

Pin Functions (continued)

NAME	PIN	I/O	DESCRIPTION
MULTIPLEXER			
Ch4	24	Analog input	Analog channel for multiplexer
Ch5	23	Analog input	Analog channel for multiplexer
Ch6	22	Analog input	Analog channel for multiplexer
Ch7	21	Analog input	Analog channel for multiplexer
Ch8	18	Analog input	Analog channel for multiplexer
Ch9	17	Analog input	Analog channel for multiplexer
Ch10	16	Analog input	Analog channel for multiplexer
Ch11	15	Analog input	Analog channel for multiplexer
Ch12	14	Analog input	Analog channel for multiplexer
Ch13	13	Analog input	Analog channel for multiplexer
Ch14	12	Analog input	Analog channel for multiplexer
Ch15	11	Analog input	Analog channel for multiplexer
DIGITAL CONTROL SIGNALS			
$\overline{CS}$	31	Digital input	Chip-select input pin; active low
SCLK	32	Digital input	Serial clock input pin
SDI	33	Digital input	Serial data input pin
SDO	34	Digital output	Serial data output pin
GENERAL-PURPOSE INPUTS/OUTPUTS			
GPIO0	37	Digital I/O	General-purpose input or output
Alarm		Digital output	Active high alarm output. For configuration, see the Programming section.
GPIO1	38	Digital I/O	General-purpose input or output
Low alarm		Digital output	Active high output indicating low alarm
GPIO2	1	Digital I/O	General-purpose input or output
Range		Digital input	Selects ADC input range: High (1)-> Range 2 (0 to $2xV_{REF}$) / Low (0)-> Range 1 (0 to V_{REF})
GPIO3	2	Digital I/O	General-purpose input or output
$\overline{PD}$		Digital input	Active low power-down input
POWERSUPPLY ANDGROUND			
+VA	5,29	—	Analog power supply
AGND	6,10,19, 20,30	—	Analog ground
+VBD	36	—	Digital I/O supply
BDGND	35	—	Digital ground
NC PINS			
—	—	—	Pins internally not connected, do not float these pins, connect these pins to ground

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
+VA to AGND		-0.3	6.5	V
+VBD to BDGND		-0.3	+VA + 0.3	V
AINP or CHn to AGND		-0.3	+VA + 0.3	V
Digital input voltage to BDGND		-0.3	+VBD + 0.3	V
Digital output to BDGND		-0.3	+VBD + 0.3	V
Input current to any pin except supply pins		-10	10	mA
Package thermal impedance, θ_{JA} (2)	TSSOP38		85	°C/W
Operating temperature		-40	125	°C
Junction temperature (T_J Max) (3)			150	°C
Storage temperature (T_{stg})		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD-51.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), JESD22-a114	±4000	V
		Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1000	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{(+VA)}$	Analog power-supply voltage	2.7	3.3	5.25	V
$V_{(+VBD)}$	Digital I/O-supply voltage	1.7	3.3	$V_{(+VA)}$	
$V_{(REF)}$	Reference voltage	2	2.5	3	
$f_{(SCLK)}$	SCLK frequency			20	MHz
T_A	Operating temperature range	-40		125	°C

7.4 Electrical Characteristics

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to +VA, V_{REF} = 2.5 V ± 0.1 V, T_A = – 40°C to 125°C, f_{sample} = 1 MHz, AINP with a 220pF to AGND, typical values are at T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
Full-scale input span (1)		Range 1	0		V_{REF}	V
		Range 2 while 2xV_{REF} ≤ +VA	0		2*V_{REF}	
Absolute input range		Range 1	-0.2		V_{REF}+0.2	V
		Range 2 while 2xV_{REF} ≤ +VA	-0.2		2*V_{REF}+0.2	
Input capacitance				15		pF
Input leakage current		T_A = 125°C		60		nA
SYSTEM PERFORMANCE						
Resolution				12		Bits
NMC	No missing codes		12			Bits
INL	Integral linearity			±0.5		LSB(2)
DNL	Differential linearity			±0.3		LSB
O_E	Offset error (3)			±1		LSB
G_E	Gain error			±1		LSB
Total unadjusted error (TUE)				±2		LSB
SAMPLING DYNAMICS						
Conversion time		20 MHz SCLK		800		ns
Acquisition time				325		ns
Maximum throughput rate		20 MHz SCLK			1	MHz
Aperture delay				8		ns
DYNAMIC CHARACTERISTICS						
Small signal bandwidth		At–3 dB		20		MHz
Channel-to-channel crosstalk		Any off-channel with 100 kHz, Full-scale input to channel being sampled with DC input (isolation crosstalk).		-100		dB
		From previously sampled to channel with 100 kHz, Full-scale input to channel being sampled with DC input (memory crosstalk).		-70		dB

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured relative to an ideal full-scale input.

Electrical Characteristics(continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to +VA, V_{REF} = 2.5 V ± 0.1 V, T_A = – 40°C to 125°C, f_{sample} = 1 MHz, AINP with a 220pF to AGND, typical values are at T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RANGE1, +VA = 2.7 V to 3.3 V						
THD	Total harmonic distortion (4)	Fin=50KHz		-75.5		dB
SNR	Signal-to-noise ratio			71.9		dB
SINAD	Signal-to-noise + distortion			70.4		dB
SFDR	Spurious free dynamic range			76.2		dB
THD	Total harmonic distortion (4)	AINP without 220pF, Fin=100KHz (5)		-80		dB
SNR	Signal-to-noise ratio			72.4		dB
SINAD	Signal-to-noise + distortion			71.7		dB
SFDR	Spurious free dynamic range			82		dB
RANGE1, +VA = 3.3 V to 5.25 V						
THD	Total harmonic distortion (4)	Fin=50KHz		-83		dB
SNR	Signal-to-noise ratio			71.9		dB
SINAD	Signal-to-noise + distortion			71.6		dB
SFDR	Spurious free dynamic range			85		dB
THD	Total harmonic distortion (4)	AINP without 220pF, Fin=100KHz (5)		-83.5		dB
SNR	Signal-to-noise ratio			72.5		dB
SINAD	Signal-to-noise + distortion			72.2		dB
SFDR	Spurious free dynamic range			88		dB
RANGE2, +VA = 5 V to 5.25 V						
THD	Total harmonic distortion (4)	Fin=50KHz		-80		dB
SNR	Signal-to-noise ratio			73		dB
SINAD	Signal-to-noise + distortion			72.4		dB
SFDR	Spurious free dynamic range			82		dB
THD	Total harmonic distortion (4)	AINP without 220pF, Fin=100KHz (5)		-79		dB
SNR	Signal-to-noise ratio			72.8		dB
SINAD	Signal-to-noise + distortion			72		dB
SFDR	Spurious free dynamic range			82		dB
EXTERNAL REFERENCE INPUT						
V_{REF} reference voltage at REFP			2	2.5	3	V
Reference input resistance		At f_{sample} = 1 MHz		100		kΩ
ALARM SETTING						
High threshold range			0		4092	LSB
Low threshold range			0		4092	LSB

(4) Calculated on the first nine harmonics of the input frequency.
(5) CHx with an isolation resistor and a sampling capacitor.

Electrical Characteristics(continued)

+VA = 2.7 V to 5.25 V, +VBD = 1.7 V to +VA, V_{REF} = 2.5 V ± 0.1 V, T_A = – 40°C to 125°C, f_{sample} = 1 MHz, AINP with a 220pF to AGND, typical values are at T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
Logic family		CMOS				
Logic level	V_{IH}		0.7*(+VBD)			V
	V_{IL}	+VBD = 5 V			0.8	
	V_{IL}	+VBD = 3 V			0.4	
	V_{OH}	At Isource = 200 µA	+VBD-0.2			
	V_{OL}	At Isink = 200 µA	0.4			
Data format MSB first			MSB First			
POWERSUPPLY REQUIREMENTS						
+VA supply voltage			2.7	3.3	5.25	V
+VBD supply voltage			1.7	3.3	+ VA	V
Supply current (normal mode)		At +VA = 2.7 to 3.6V and 1MHz throughput		2.4		mA
		At +VA = 2.7 to 3.6V static state		1		
		At +VA = 4.5 to 5.25V and 1MHz throughput		3.4		
		At +VA = 4.5 to 5.25V static state		1.1		
Power-down state supply current				1		µA
+VBD supply current		+VA = +VBD=5.25V, fs = 1MHz		1.2		mA
Power-up time				1		µs
Invalid conversions after power up or reset				1		Conversion

7.5 Timing Requirements

(+VA = 2.7V to 5.25V, Full = -40°C to 125°C, unless otherwise noted.) (1)(2) (see Figure 1, Figure 2)

			MIN	NOM	MAX	UNIT
t_{conv}	Conversion time	+VBD = 1.8 V			16	SCLK
		+VBD = 3 V			16	
		+VBD = 5 V			16	
t_q	Minimum quiet sampling time needed from bus 3 state to start of next conversion	+VBD = 1.8 V	40			ns
		+VBD = 3 V	40			
		+VBD = 5 V	40			
t_{d1}	Delay time, $\overline{CS}$ low to first data (DO–15) out	+VBD = 1.8 V			38	ns
		+VBD = 3 V			27	
		+VBD = 5 V			17	
t_{su1}	Setup time, $\overline{CS}$ low to first rising edge of SCLK	+VBD = 1.8 V	8			ns
		+VBD = 3 V	6			
		+VBD = 5 V	4			
t_{d2}	Delay time, SCLK falling to SDO next data bit valid	+VBD = 1.8 V			35	ns
		+VBD = 3 V			27	
		+VBD = 5 V			17	
t_{h1}	Hold time, SCLK falling to SDO data bit valid	+VBD = 1.8 V	7			ns
		+VBD = 3 V	5			
		+VBD = 5 V	3			
t_{d3}	Delay time, 16th SCLK falling edge to SDO 3-state	+VBD = 1.8 V			30	ns
		+VBD = 3 V			28	
		+VBD = 5 V			16	
t_{su2}	Setup time, SDI valid to rising edge of SCLK	+VBD = 1.8 V	2			ns
		+VBD = 3 V	3			
		+VBD = 5 V	4			
t_{h2}	Hold time, rising edge of SCLK to SDI valid	+VBD = 1.8 V	12			ns
		+VBD = 3 V	10			
		+VBD = 5 V	6			
t_{w1}	Pulse duration $\overline{CS}$ high	+VBD = 1.8 V	20			ns
		+VBD = 3 V	20			
		+VBD = 5 V	20			
t_{d4}	Delay time $\overline{CS}$ high to SDO 3-state	+VBD = 1.8 V			30	ns
		+VBD = 3 V			28	
		+VBD = 5 V			16	
t_{wh}	Pulse duration SCLK high	+VBD = 1.8 V	20			ns
		+VBD = 3 V	20			
		+VBD = 5 V	20			
t_{wl}	Pulse duration SCLK low	+VBD = 1.8 V	20			ns
		+VBD = 3 V	20			
		+VBD = 5 V	20			
	Frequency SCLK	+VBD = 1.8 V			20	MHz
		+VBD = 3 V			20	
		+VBD = 5 V			20	

(1) 1.8V specifications apply from 1.7V to 1.V, 3V specifications apply from 2.7V to 3.6V, 5V specifications apply from 4.75V to 5.25V.
(2) With 50-pF load.

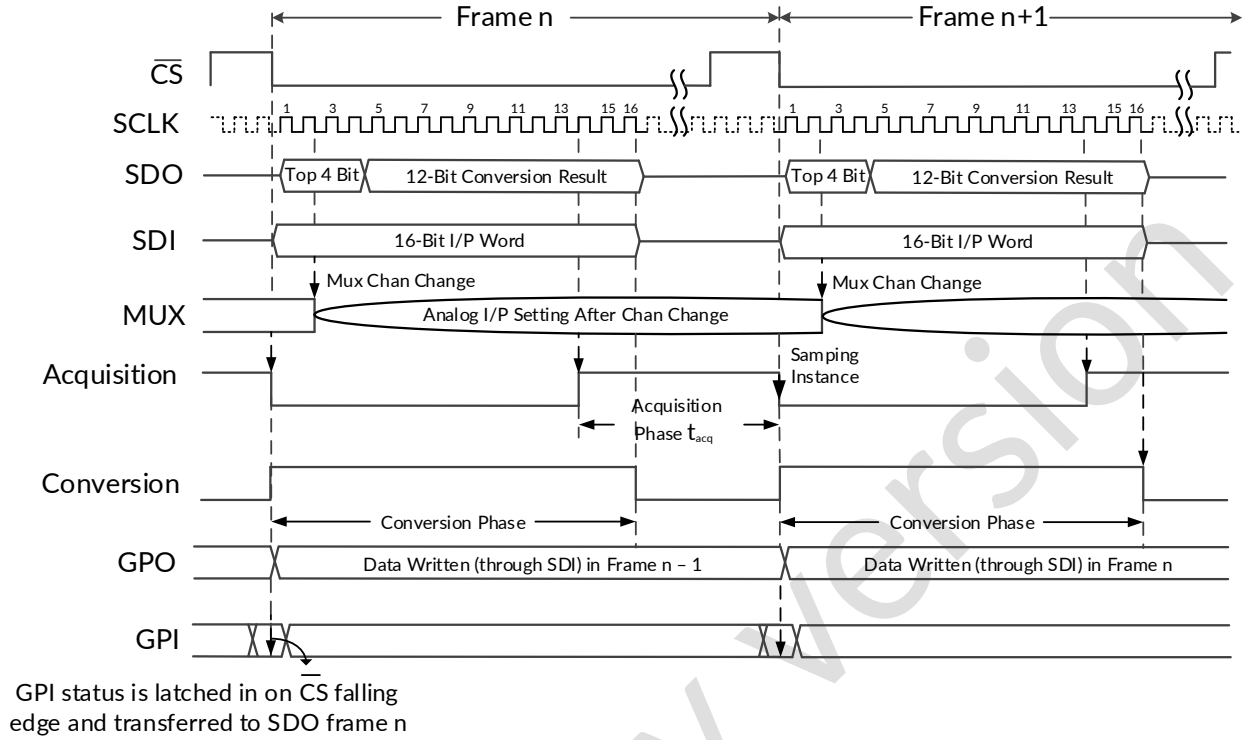


Figure 1. Device Operation Timing Diagram

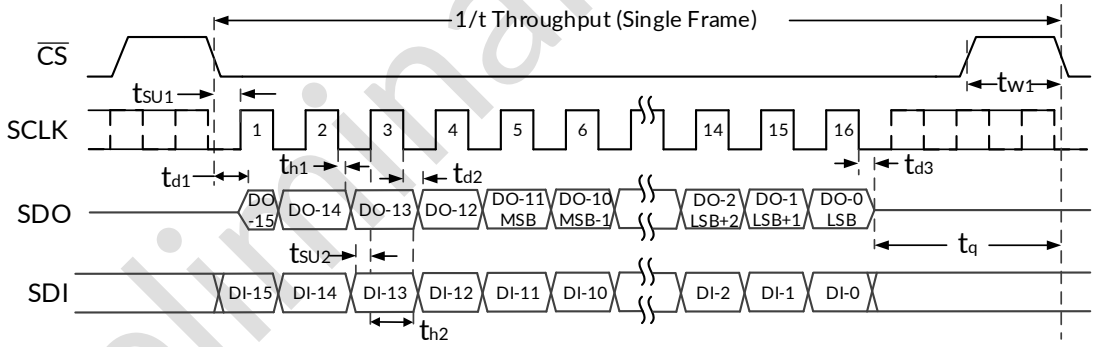


Figure 2. Serial Interface Timing Diagram

7.6 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

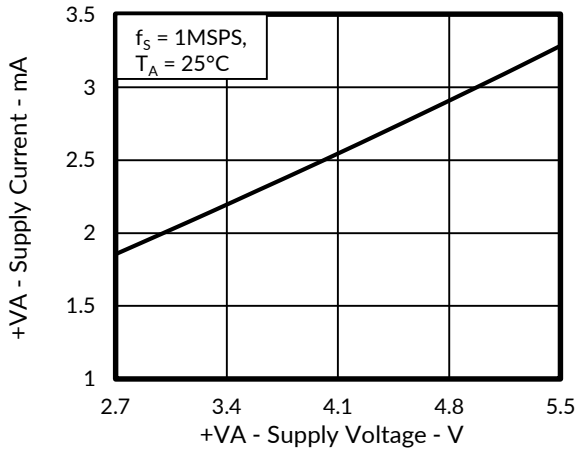


Figure 3. Supply Current vs Supply Voltage

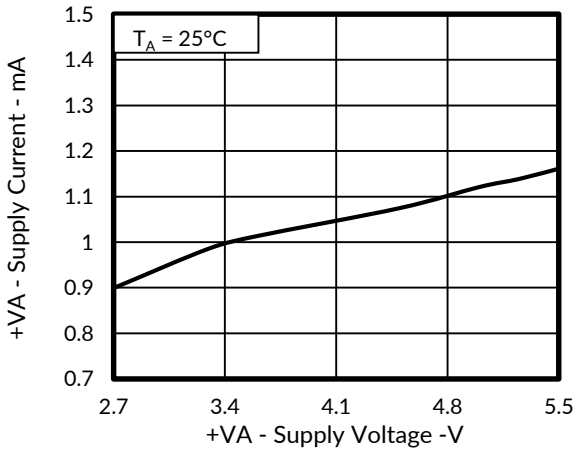


Figure 4. Static Supply Current vs Supply Voltage

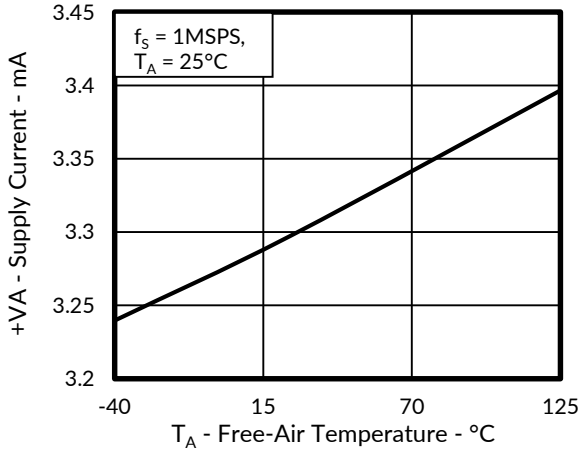


Figure 5. Supply Current vs Free-Air Temperature

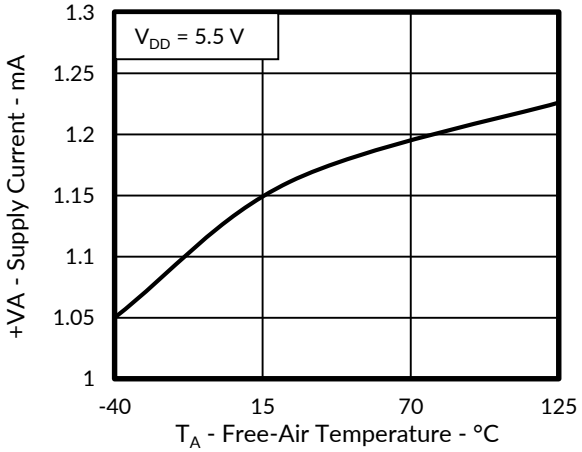


Figure 6. Static Supply Current vs Free-Air Temperature

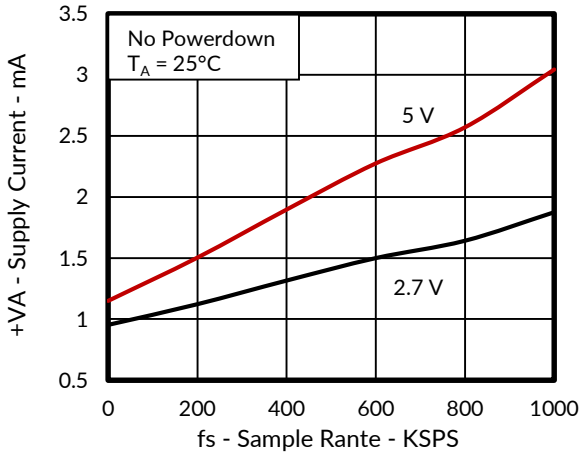


Figure 7. Supply Current vs Sample Rate

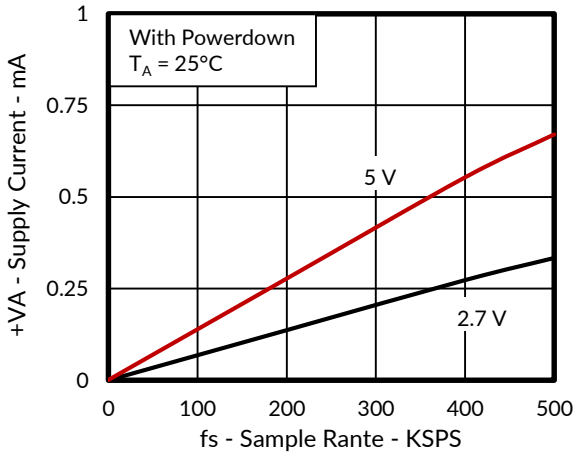


Figure 8. Supply Current vs Sample Rate

Typical Characteristics

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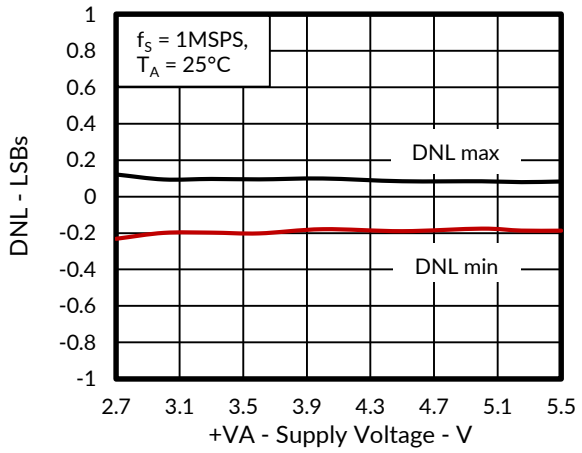

Figure 9. Differential Nonlinearity vs Supply Voltage

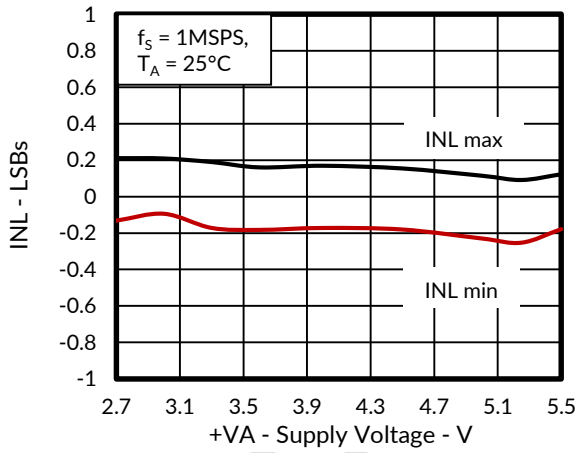

Figure 10. Integral Nonlinearity vs Supply Voltage

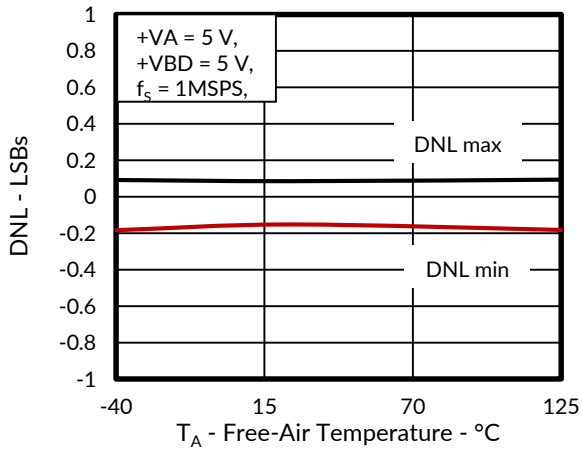

Figure 11. Differential Nonlinearity vs Free-Air Temperature

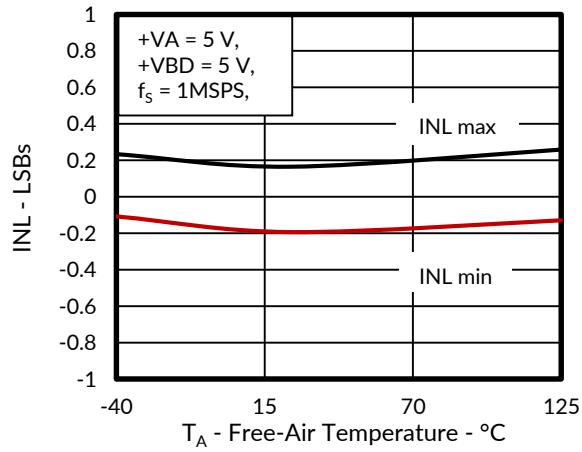

Figure 12. Integral Nonlinearity vs Free-Air Temperature

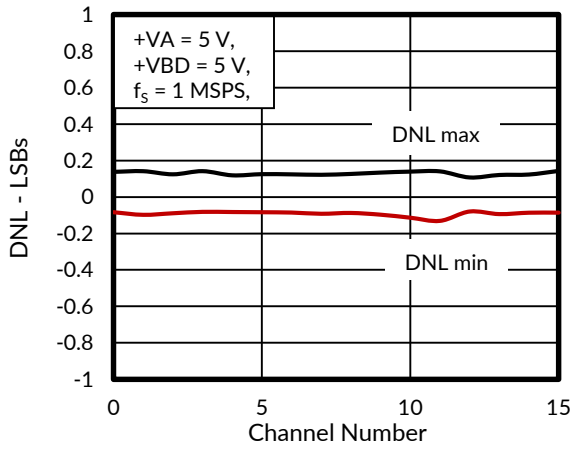

Figure 13. Differential Nonlinearity Variation Across Channels

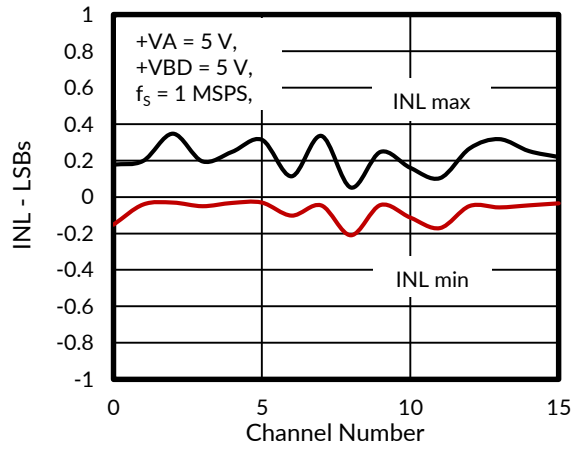

Figure 14. Integral Nonlinearity Variation Across Channels

Typical Characteristics

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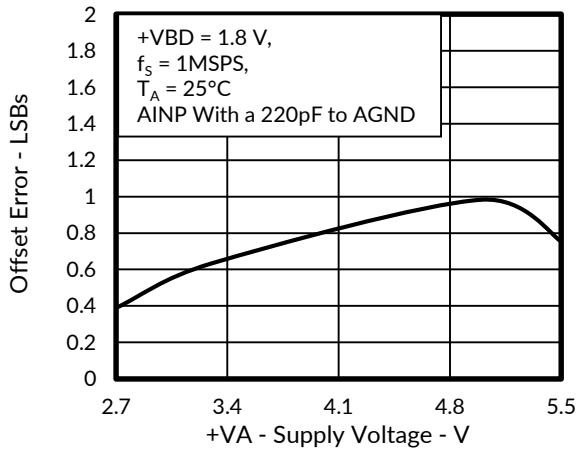


Figure 15. Offset Error vs Supply Voltage

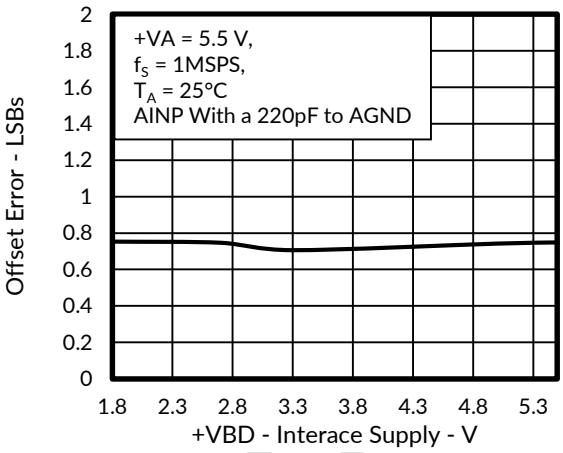


Figure 16. Offset Error vs Interface Supply Voltage

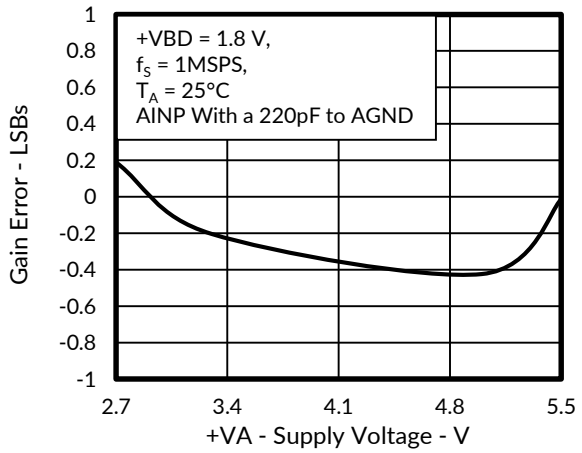


Figure 17. Gain Error vs Supply Voltage

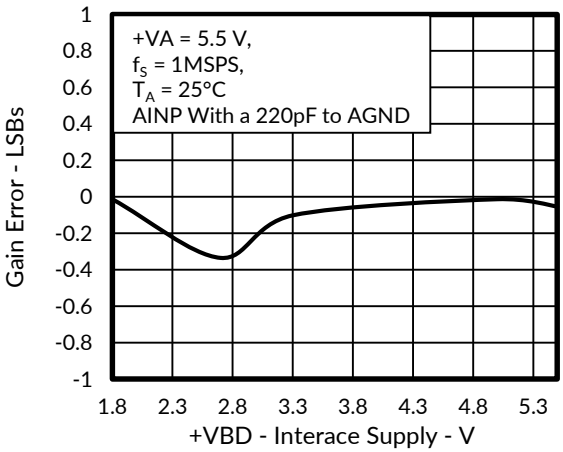


Figure 18. Gain Error vs Interface Supply Voltage

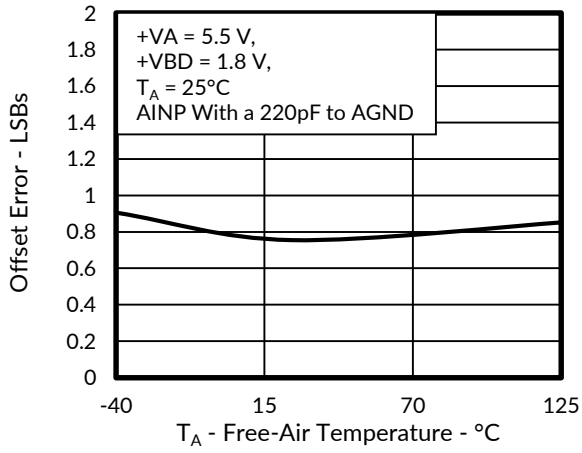


Figure 19. Offset Error vs Free-Air Temperature

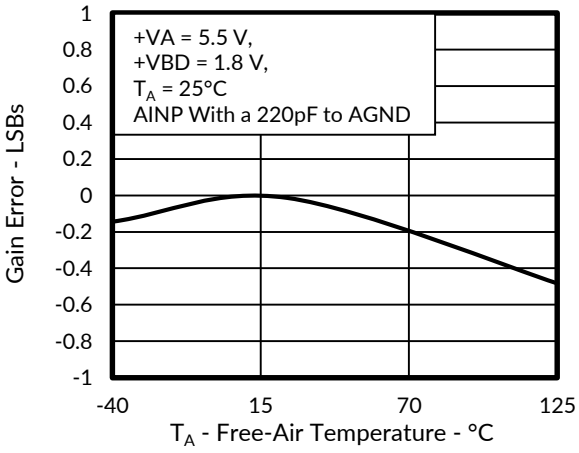


Figure 20. Gain Error vs Free-Air Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

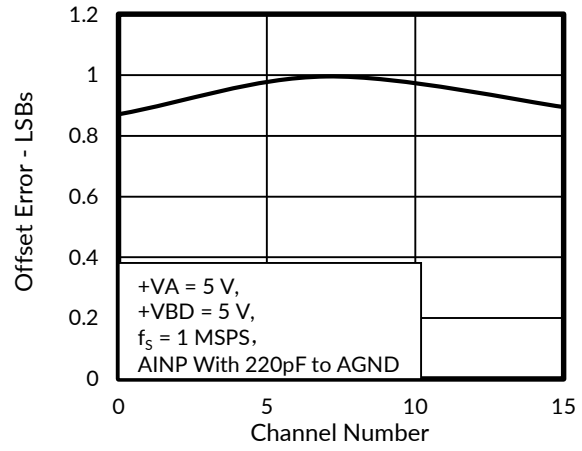


Figure 21. Offset Error Variation Across Channels

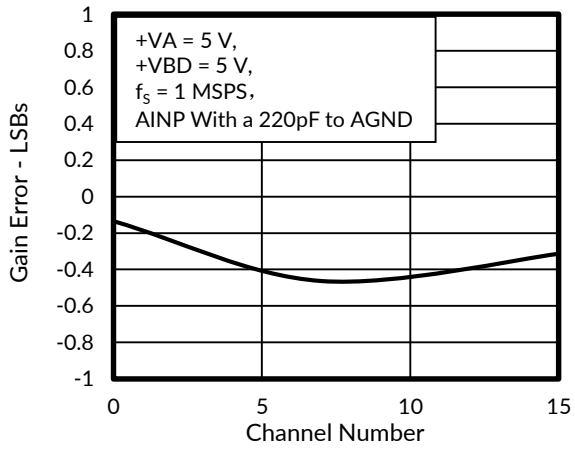


Figure 22. Gain Error Across Channels

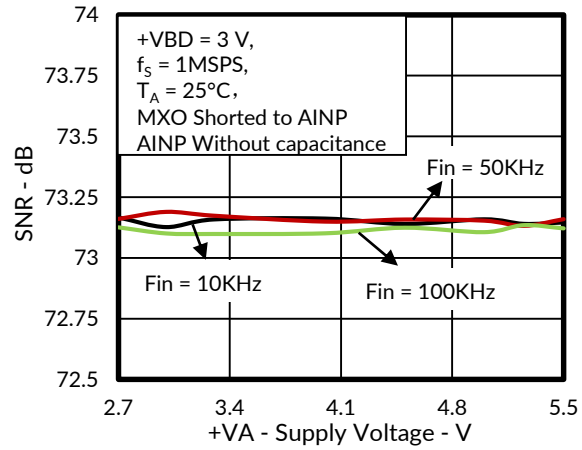


Figure 23. Signal-to-Noise Ratio vs Supply Voltage

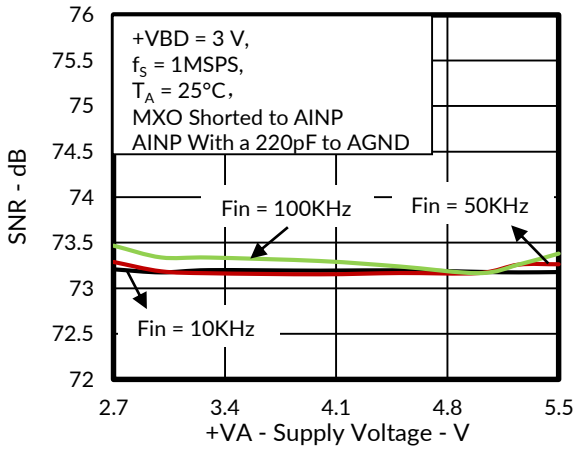


Figure 24. Signal-to-Noise Ratio vs Supply Voltage

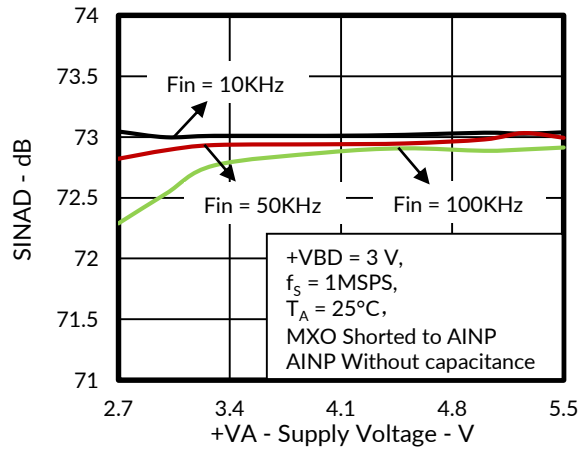


Figure 25. Signal-to-Noise + Distortion vs Supply Voltage

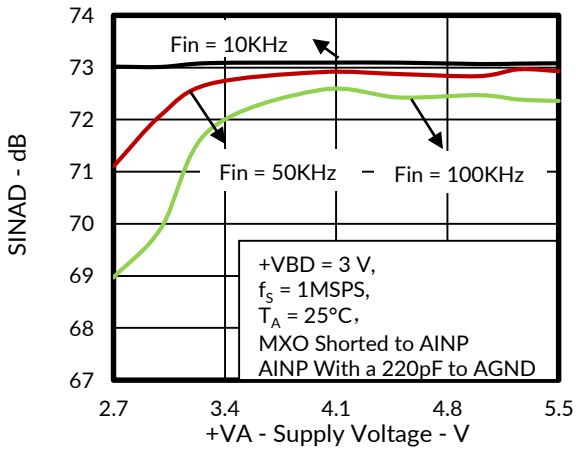


Figure 26. Signal-to-Noise + Distortion vs Supply Voltage

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

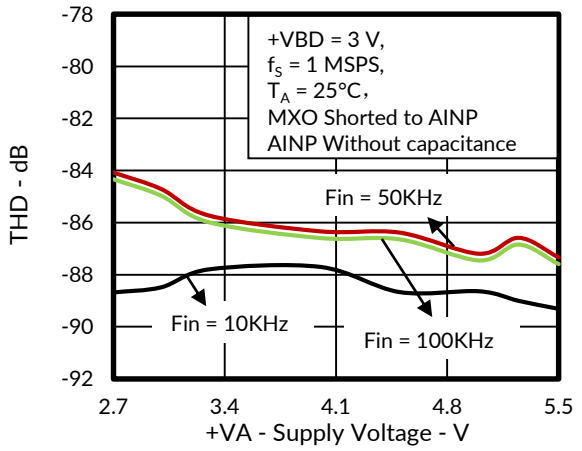


Figure 27. Total Harmonic Distortion vs Supply Voltage

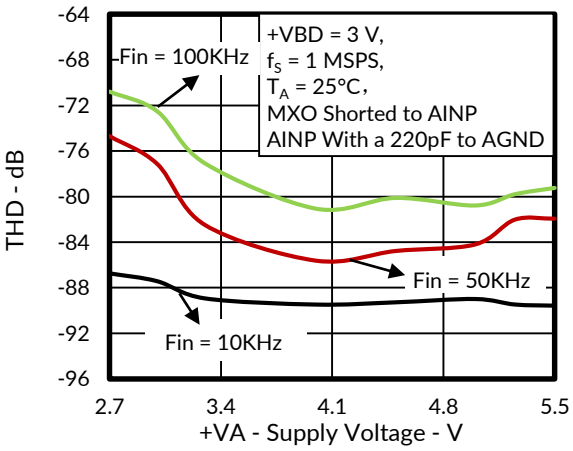


Figure 28. Total Harmonic Distortion vs Supply Voltage

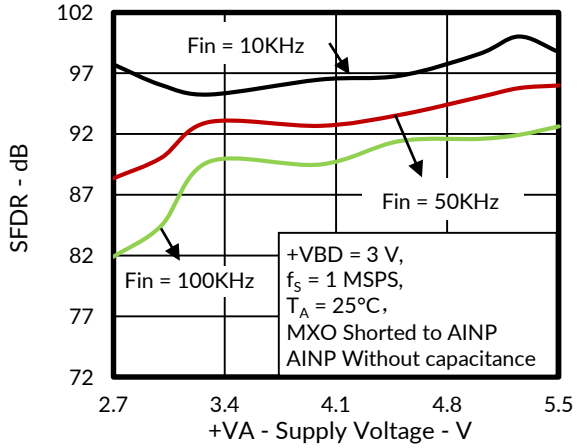


Figure 29. Spurious Free Dynamic Range vs Supply Voltage

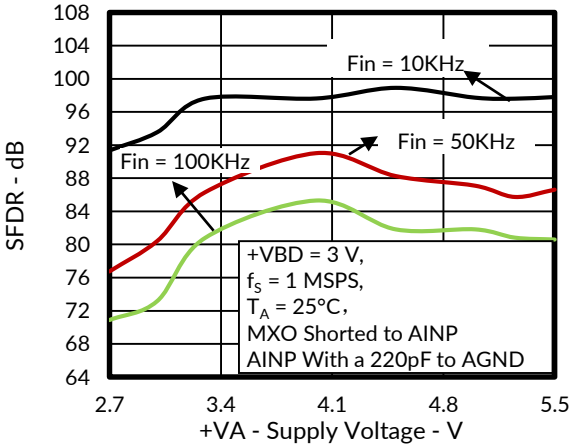


Figure 30. Spurious Free Dynamic Range vs Supply Voltage

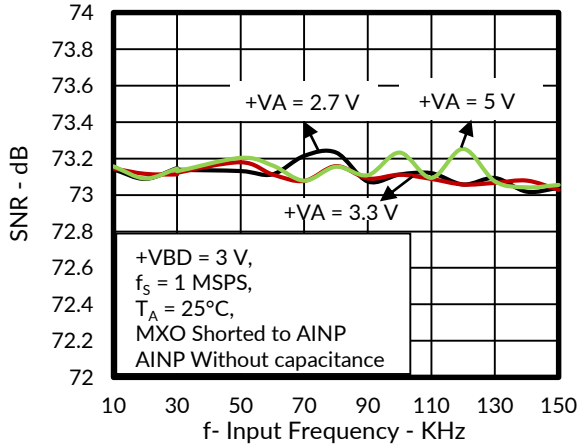


Figure 31. Signal-to-Noise Ratio vs Input Frequency

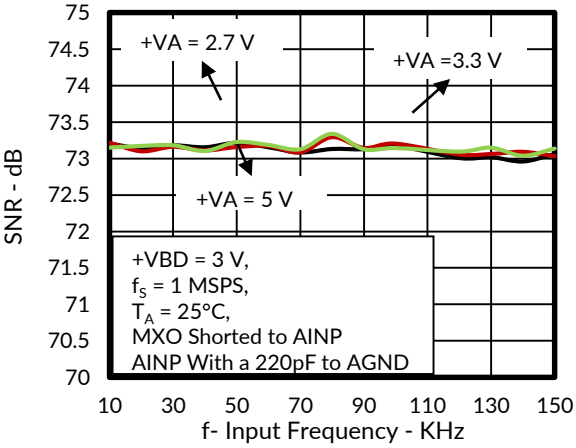


Figure 32. Signal-to-Noise Ratio vs Input Frequency

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

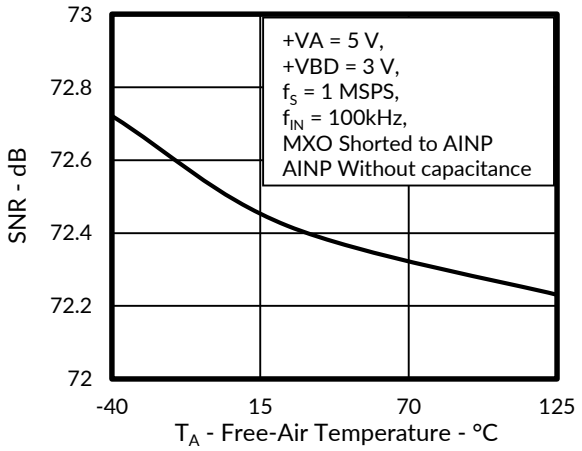


Figure 33. Signal-to-Noise Ratio vs Free-Air Temperature

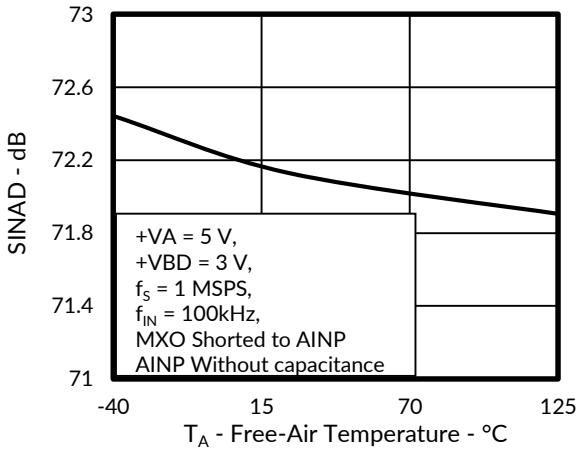


Figure 34. Signal-to-Noise + Distortion vs Free-Air Temperature

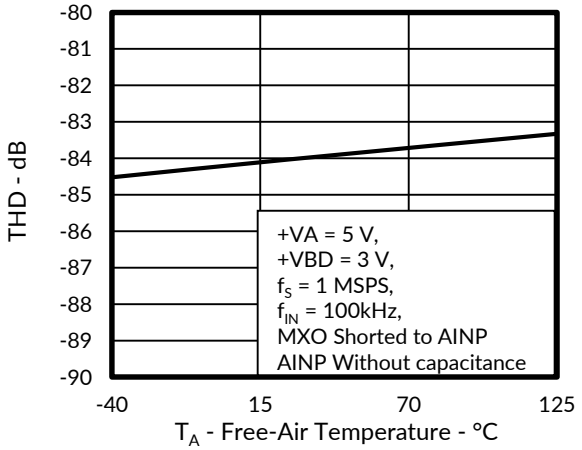


Figure 35. Total Harmonic Distortion vs Free-Air Temperature

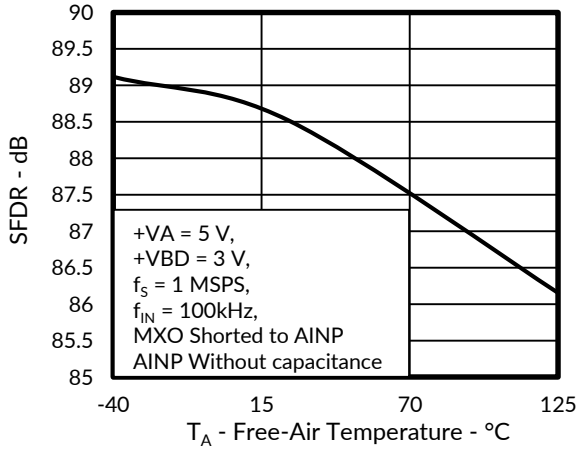


Figure 36. Spurious Free Dynamic Range vs Free-Air Temperature

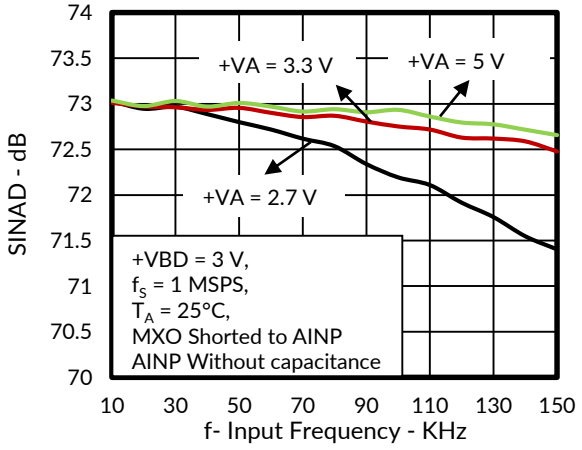


Figure 37. Signal-to-Noise + Distortion vs Input Frequency

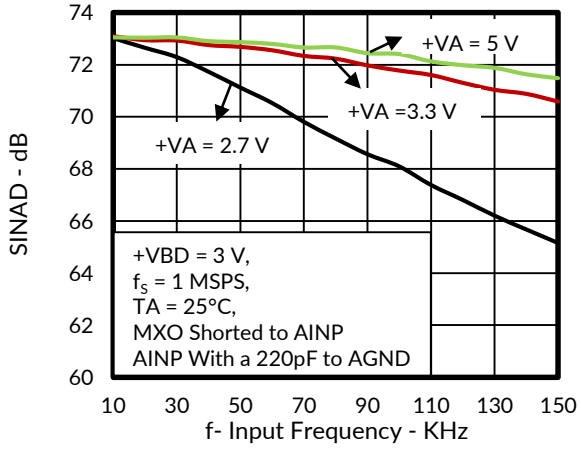


Figure 38. Signal-to-Noise + Distortion vs Input Frequency

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

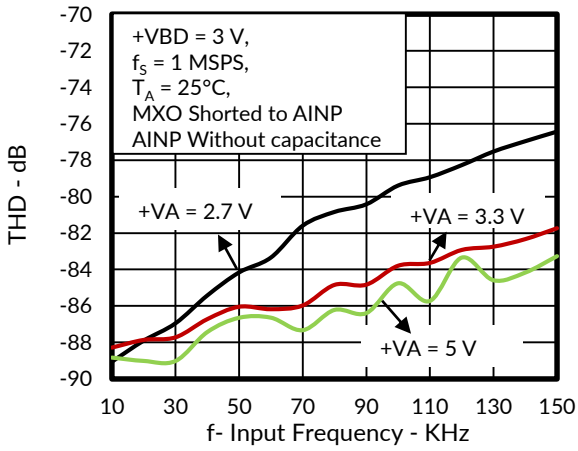


Figure 39. Total Harmonic Distortion vs Input Frequency

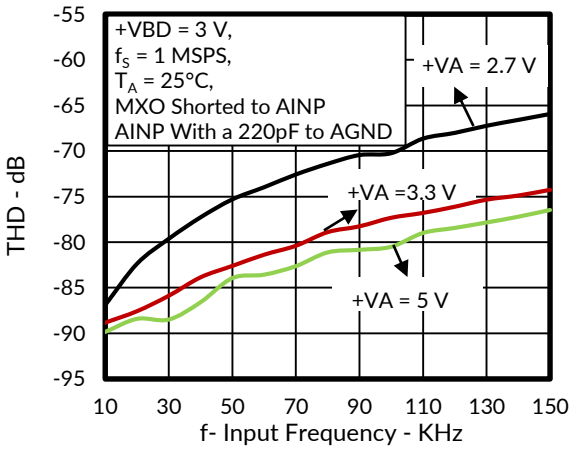


Figure 40. Total Harmonic Distortion vs Input Frequency

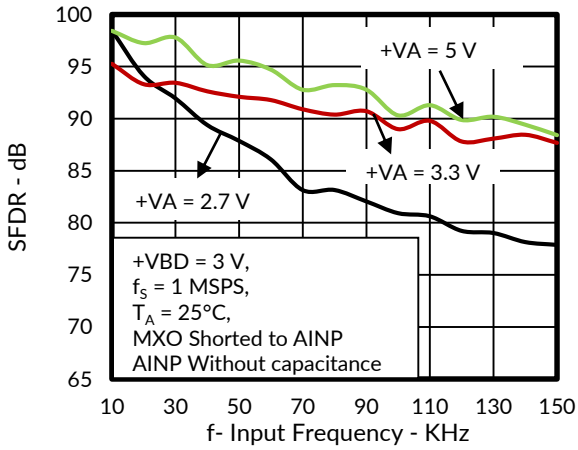


Figure 41. Spurious Free Dynamic Range vs Input Frequency

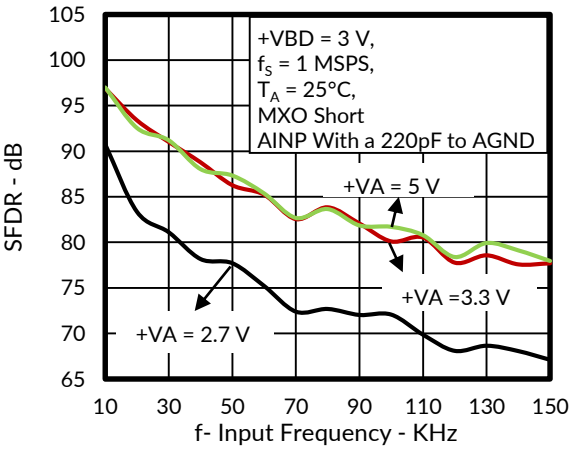


Figure 42. Spurious Free Dynamic Range vs Input Frequency

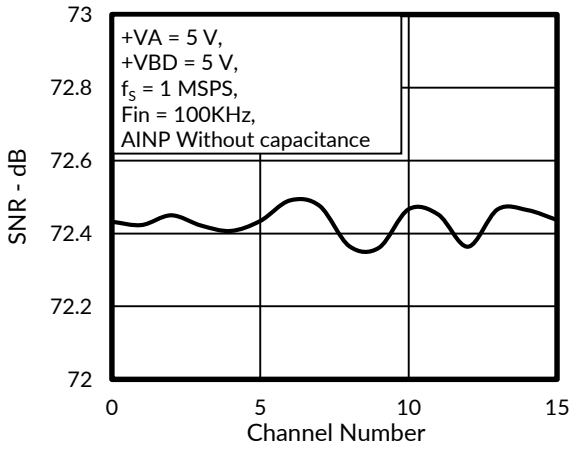


Figure 43. Signal-to-Noise Ratio Variation Across Channels

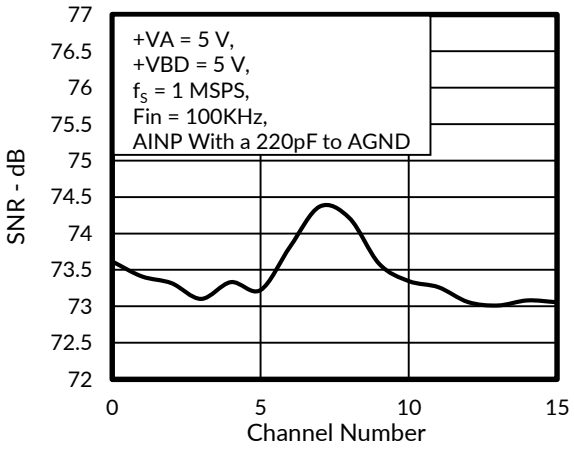


Figure 44. Signal-to-Noise Ratio Variation Across Channels

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

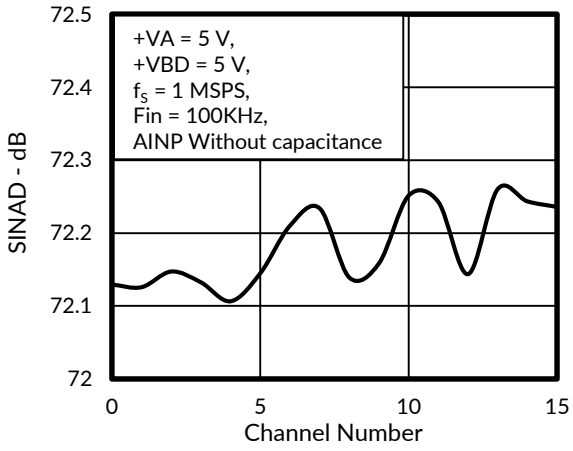


Figure 45. Signal-to-Noise + Distortion Variation Across Channels

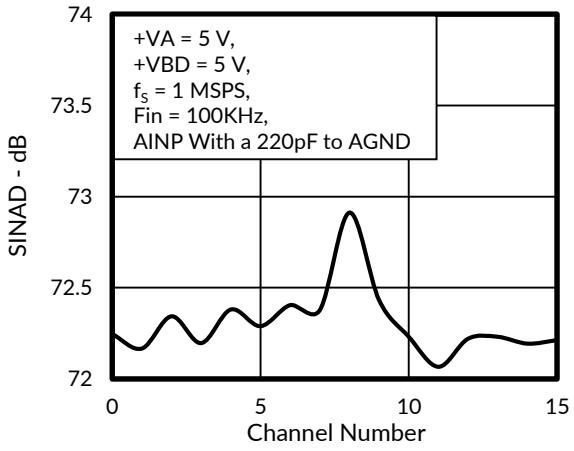


Figure 46. Signal-to-Noise + Distortion Variation Across Channels

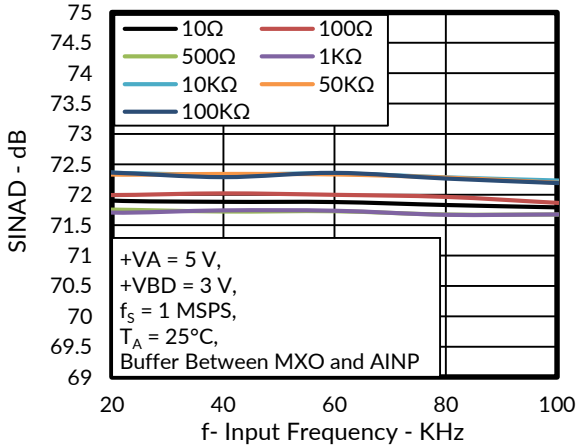


Figure 47. Signal-to-Noise + Distortion vs Input Frequency (Across Different Source Resistance Values)

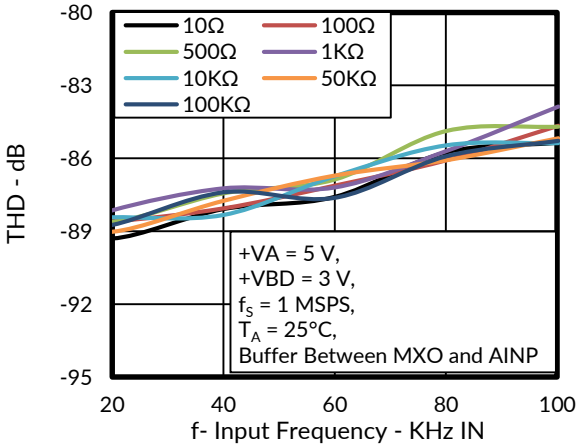


Figure 48. Total Harmonic Distortion vs Input Frequency (Across Different Source Resistance Values)

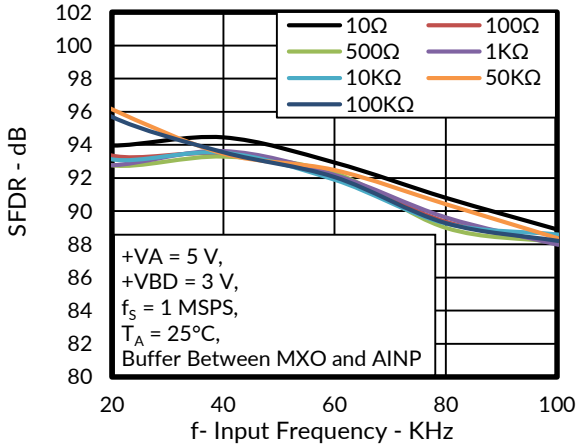


Figure 49. Spurious Free Dynamic Range vs Input Frequency (Across Different Source Resistance Values)

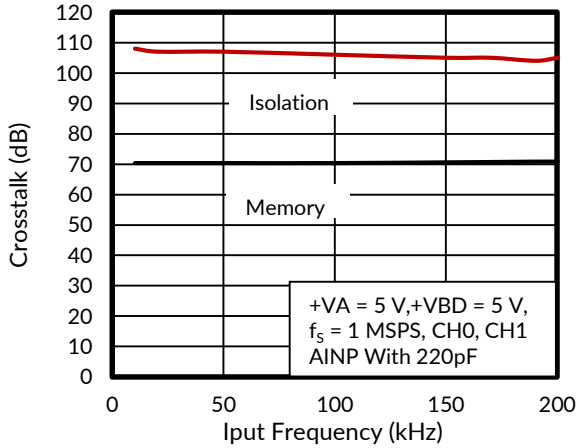


Figure 50. Crosstalk vs Input Frequency

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

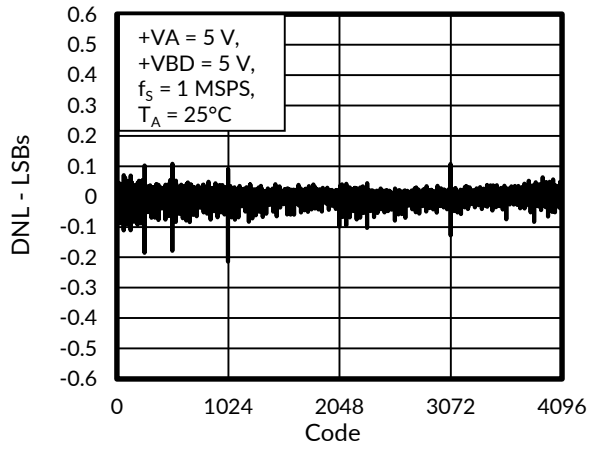


Figure 51. Typical DNL for All Codes

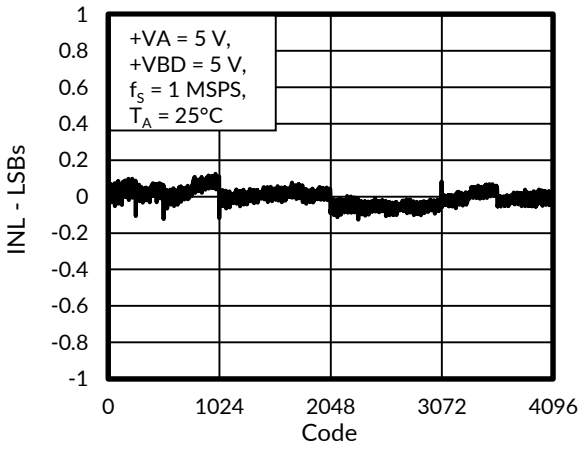


Figure 52. Typical INL for All Codes

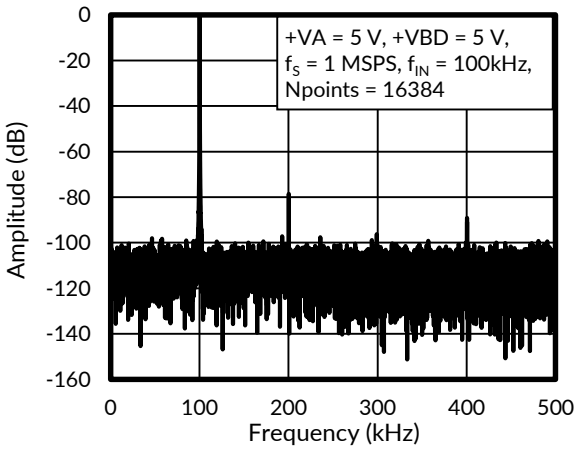


Figure 53. Typical FFT Plot

8 DETAILED DESCRIPTION

8.1 Overview

The device is a 12-bit, high-speed, low-power, successive approximation register (SAR) analog-to-digital converter (ADC) that uses an external reference. The architecture is based on charge redistribution, which inherently includes a sample/hold function. The analog inputs to the RS1467 are provided to CHX input channels. All input channels share a common analog ground AGND. RS1467 has multiplexer breakout feature which allows user to connect the signal conditioning circuit between multiplexer output (MXO) and ADC input (AINP). This feature enables use of common signal conditioning block for the input signal which exhibit similar performance characteristics. RS1467 can be programmed to select a channel manually or can be programmed into the auto channel select mode to sweep through the input channels automatically.

Figure 1, Figure 2 show device operation timing. Device operation is controlled with $\overline{CS}$, SCLK, and SDI. The device outputs its data on SDO.

Each frame begins with the falling edge of $\overline{CS}$. With the falling edge of $\overline{CS}$, the input signal from the selected channel is sampled, and the conversion process is initiated. The device outputs data while the conversion is in progress. The 16-bit data word contains a 4-bit channel address, followed by a 12-bit conversion result in MSB first format. There is an option to read the GPIO status instead of the channel address. (Refer to Table 1, Table 2, and Table 5 for more details.)

The device selects a new multiplexer channel on the second SCLK falling edge. The acquisition phase starts on the fourteenth SCLK rising edge. On the next $\overline{CS}$ falling edge the acquisition phase will end, and the device starts a new frame.

The TSSOP packaged device has four General Purpose IO (GPIO) pins. These four pins can be individually programmed as GPO or GPI. It is also possible to use them for preassigned functions, refer to Table 9. GPO data can be written into the device through the SDI line. The device refreshes the GPO data on the $\overline{CS}$ falling edge as per the SDI data written in previous frame.

Similarly the device latches GPI status on the $\overline{CS}$ falling edge and outputs the GPI data on the SDO line (if GPI read is enabled by writing DI04=1 in the previous frame) in the same frame starting with the $\overline{CS}$ falling edge.

The falling edge of $\overline{CS}$ clocks out DO15 (first bit of the four bit channel address), and remaining address bits are clocked out on every falling edge of SCLK until the third falling edge. The conversion result MSB is clocked out on the 4th SCLK falling edge and LSB on the 15th falling edge respectively for 12-bit devices. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 16th falling edge of SCLK. $\overline{CS}$ can be asserted (pulled high) only after 16 clocks have elapsed.

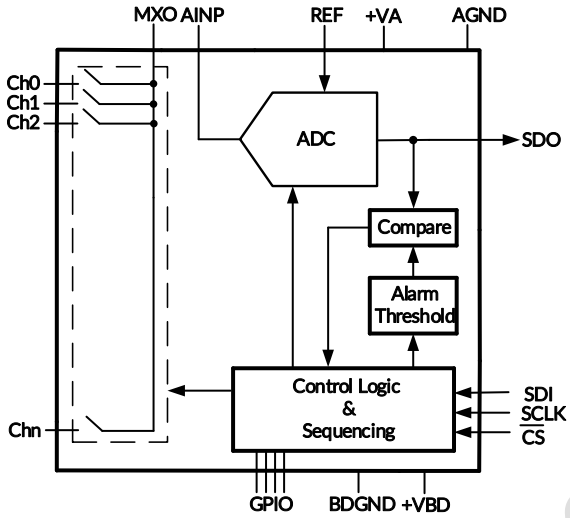
The device reads a sixteen bit word on the SDI pin while it outputs the data on the SDO pin. SDI data is latched on every rising edge of SCLK starting with the 1st clock as shown in Figure 2.

$\overline{CS}$ can be asserted (pulled high) only after 16 clocks have elapsed.

The device has two (high and low) programmable alarm thresholds per channel. If the input crosses these limits; the device flags out an alarm on GPIO0/GPIO1 depending on the GPIO program register settings (refer to Table 9). The alarm is asserted (under the alarm conditions) on the 12th falling edge of SCLK in the same frame when a data conversion is in progress. The alarm output is reset on the 10th falling edge of SCLK in the next frame.

The device offers a power-down feature to save power when not in use. There are two ways to power down the device. It can be powered down by writing DI05 = 1 in the mode control register (refer to Table 1, Table 2, and Table 5); in this case the device powers down on the 16th falling edge of SCLK in the next data frame. Another way to power down the device is through GPIO in the case of the TSSOP packaged devices. GPIO3 can act as the $\overline{PD}$ input (refer to Table 9 to assign this functionality to GPIO3). This is an asynchronous and active low input. The device powers down instantaneously after GPIO3 ($\overline{PD}$) = 0. The device will power up again on the $\overline{CS}$ falling edge with DI05 = 0 in the mode control register and GPIO3 ($\overline{PD}$) = 1.

8.2 Functional Block Diagram



NOTE: n is number of channels
NOTE: There are 4 GPIOs in this package

8.3 Feature Description

8.3.1 Reference

The RS1467 can operate with an external 2.5-V ± 10-mV reference. A clean, low noise, well-decoupled reference voltage on the REFP pin is required to ensure good performance of the converter. A low noise bandgap reference like the RS5025 can be used to drive this pin. A 10-µF ceramic decoupling capacitor is required between the REFP and REFM pins of the converter. The capacitor should be placed as close as possible to the pins of the device.

8.3.2 Power Saving

RS1467 offers a power-down feature to save power when not in use. There are two ways to power down the device. It can be powered down by writing DI05 = 1 in the Mode Control register (refer to Table 1, Table 2 and Table 5); in this case the device powers down on the 16th falling edge of SCLK in the next data frame. Another way to power down the device is through GPIO. GPIO3 can act as a PD input (refer to Table 9, for assigning this functionality to GPIO3). This is an asynchronous and active low input. The device powers down instantaneously after GPIO3 ($\overline{PD}$) = 0. The device will powerup again on the $\overline{CS}$ falling edge while DI05 = 0 in the Mode Control register and GPIO3 ($\overline{PD}$) = 1.

8.4 Device Functional Modes

8.4.1 Channel Sequencing Modes

There are three modes for channel sequencing, namely Manual mode, Auto-1 mode, Auto-2 mode. Mode selection is done by writing into the Mode Control Register (refer to Table 1, Table 2, and Table 5). A new multiplexer channel is selected on the second falling edge of SCLK (as shown in Figure 1) in all three modes.

Manual mode: When configured to operate in Manual mode, the next channel to be selected is programmed in each frame and the device selects the programmed channel in the next frame. On powerup or after reset the default channel is 'Channel-0' and the device is in Manual mode.

Auto-1 mode: In this mode the device scans pre-programmed channels in ascending order. A new multiplexer channel is selected every frame on the second falling edge of SCLK. There is a separate Program Register for pre-programming the channel sequence. Table 3 and Table 4 show Auto-1 'program register' settings.

Device Functional Modes (continued)

Once programmed the device retains 'Program Register settings until the device is powered down, reset, or reprogrammed. It is allowed to exit and re-enter the Auto-1 mode any number of times without disturbing 'program register' settings.

The Auto-1 program register is reset to FFFF hex upon device powerup or reset; implying the device scans all channels in ascending order.

Auto-2 mode: In this mode the user can configure the program register to select the last channel in the scan sequence. The device scans all channels from channel 0 up to and including the last channel in ascending order. The multiplexer channel is selected every frame on the second falling edge of SCLK. There is a separate 'program register' for pre-programming of the last channel in the sequence (multiplexer depth). Table 6 lists the 'Auto-2 prog' register settings for selection of the last channel in the sequence.

Once programmed the device retains program register settings until the device is powered down, reset, or reprogrammed. It is allowed to exit and re-enter Auto-2 mode any number of times, without disturbing the 'program register' settings.

On powerup or reset the bits D9-D6 of the Auto-2 program register are reset to F hex; implying the device scans all channels in ascending order.

8.4.2 Device Programming and Mode Control

The following section describes device programming and mode control. The RS1467 features two types of registers to configure and operate the device in different modes. These registers are referred as 'Configuration Registers'. There are two types of 'Configuration Registers' namely 'Mode Control Registers' and 'Program Registers'.

8.4.2.1 Mode Control Register

A 'Mode Control Register' is configured to operate the device in one of three channel sequencing modes, namely Manual mode, Auto-1 Mode, Auto-2 Mode. It is also used to control user programmable features like range selection, device power-down control, GPIO read control, and writing output data into the GPIO.

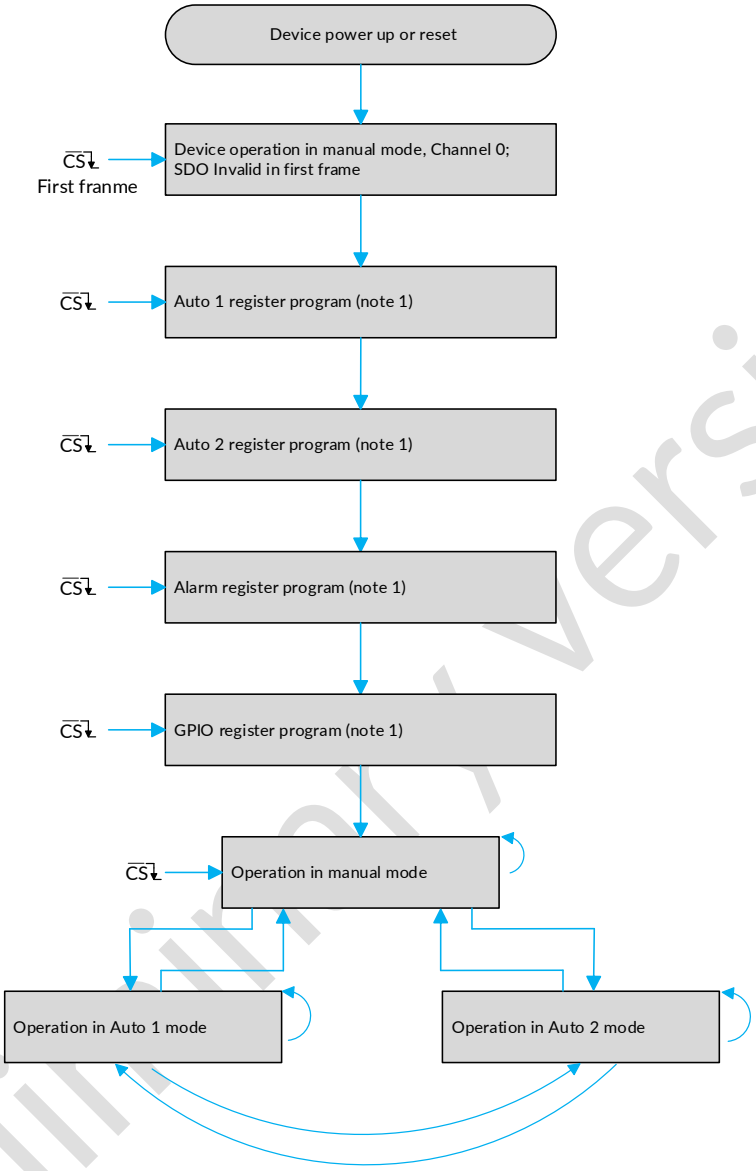
8.4.2.2 Program Registers

The 'Program Registers' are used for device configuration settings and are typically programmed once on powerup or after device reset. There are different program registers such as 'Auto-1 mode programming' for pre-programming the channel sequence, 'Auto-2 mode programming' for selection of the last channel in the sequence, 'Alarm programming' for all 16 channels and GPIO for individual pin configuration as GPI or GPO or a pre-assigned function.

8.4.3 Device Power-Up Sequence

The device power-up sequence is shown in Figure 54. By default, the Mode Control Register is configured for manual mode and the default channel is channel 0. As explained previously, the device offers Program Registers to configure user programmable features like GPIOs, Alarms, and to pre-program the channel sequence for Auto modes. At 'power up or on reset' these registers are set to the default values listed in Table 1 to Table 9. On power up or after reset It is required to program Mode Control Register and Program Register to required mode of operation. Once configured; the device is ready to use in any of the three channel sequencing modes namely Manual, Auto-1, and Auto-2.

Device Functional Modes (continued)



(1) The device continues its operation in manual mode channel 0 throughout the programming sequence and outputs valid conversion results. It is possible to change channel, range, GPIO by inserting extra frames in between two programming blocks. It is also possible to bypass any programming block if the user does not intend to use that feature.

(2) It is possible to reprogram the device at any time during operation, regardless of what mode the device is in. During programming the device continues its operation in whatever mode it is in and outputs valid data.

Figure 54. Device Power-Up Sequence

8.4.4 Operating in Manual Mode

The flowchart in Figure 55 illustrates the steps involved in operating in manual channel sequencing mode. Table 1 lists the mode control register settings for manual mode. There are no program registers in manual mode.

Device Functional Modes (continued)

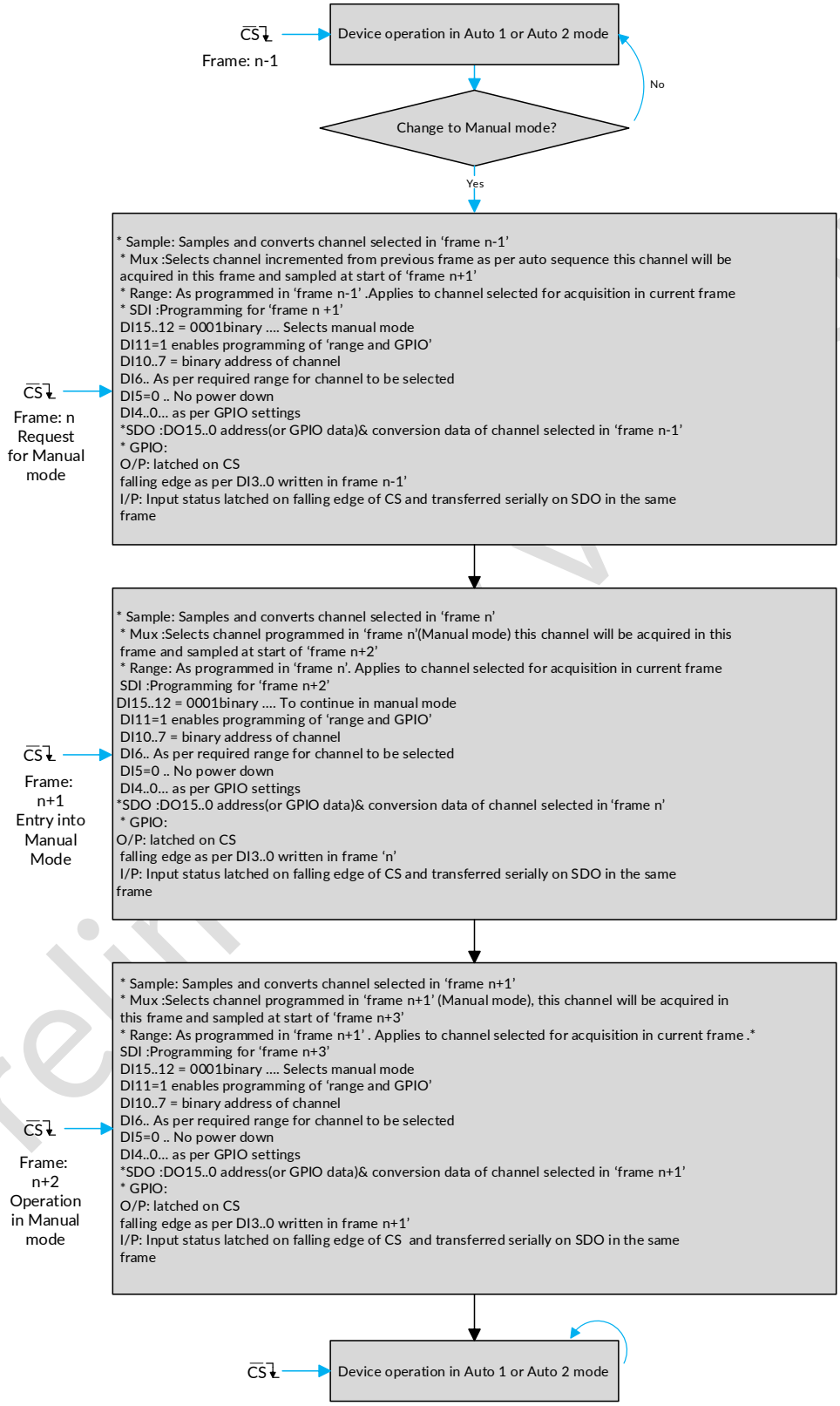


Figure 55. Entering and Running in Manual Channel Sequencing Mode

Device Functional Modes (continued)

Figure 56 shows an example in which manual mode is used to scan channels 4, 7, and 9. The command to select channel 4 (CH4) is issued in the Nth frame and the data corresponding to CH4 is available in the (N + 2)th frame. Internally, the SDI command is parsed and on the rising edge of $\overline{CS}$ of the (N+1)th frame and the MUX switches accordingly on the second falling edge of SCLK in this frame. On the rising edge of $\overline{CS}$ of the (N+2)th frame, the input signal for CH4 is sampled and the ADC sends the conversion data in this third frame. The device follows the same steps and the ADC sends the conversion data for CH7 and CH9 in the subsequent two frames.

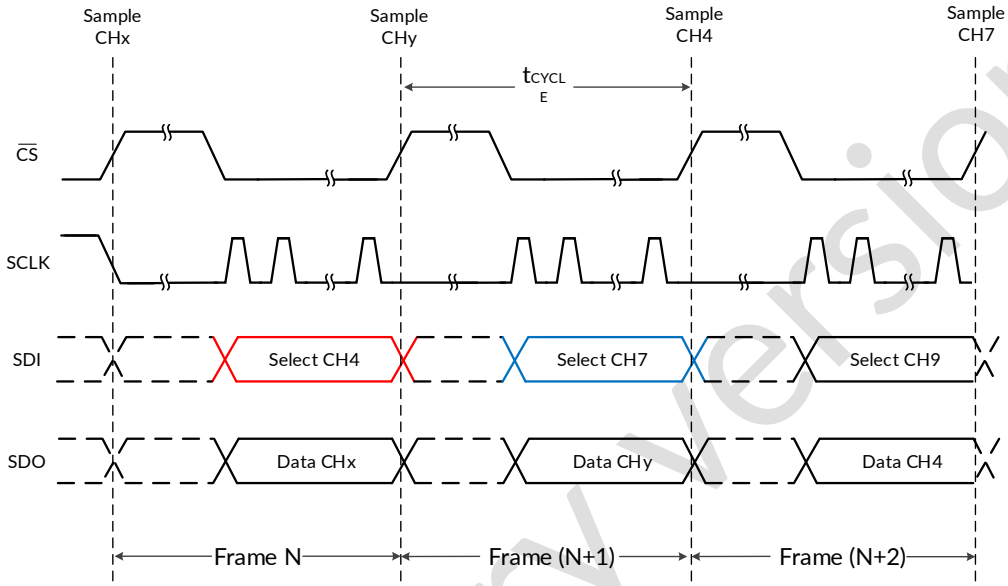


Figure 56. Entering and Running in Manual Channel Sequencing Mode

Table 1. Mode Control Register Settings for Manual Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION			
DI15-12	0001	0001	Selects Manual Mode			
DI11	0	1	Enables programming of bits DI06-00.			
		0	Device retains values of DI06-00 from the previous frame.			
DI10-07	0	This four bit data represents the address of the next channel to be selected in the next frame. DI10: MSB and DI07: LSB. For example, 0000 represents channel- 0, 0001 represents channel-1 and so forth.				
DI06	0	0	Selects 0 to VREF input range (Range 1)			
		1	Selects 0 to 2xVREF input range (Range 2)			
DI05	0	0	Device normal operation (no power down)			
		1	Device powers down on 16th SCLK falling edge			
DI04	0	0	SDO outputs current channel address of the channel on DO15..12 followed by 12 bit conversion result on DO11..00.			
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent 12-bit conversion result of the current channel.			
			DOI5	DOI4	DOI3	DOI2
			GPIO3	GPIO2	GPIO1	GPIO0
DI03-00	0000	GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below				
			DI03	DI02	DI01	DI00
			GPIO3	GPIO2	GPIO1	GPIO0

8.4.5 Operating in Auto-1 Mode

Figure 57 illustrates the steps involved in entering and operating in Auto-1 Channel Sequencing mode. Table 2 lists the Mode Control Register settings for Auto-1 mode.

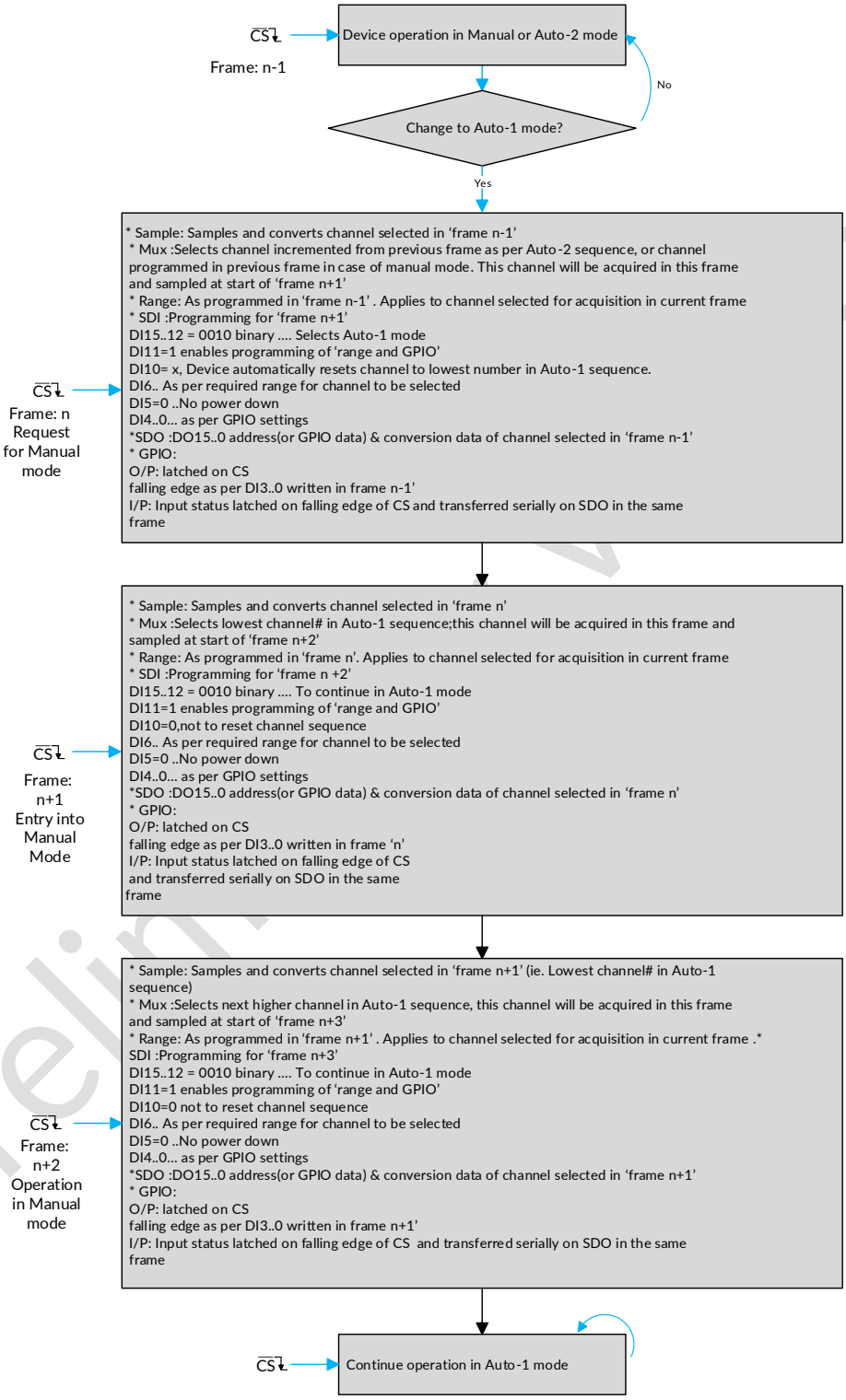


Figure 57. Entering and Running in Auto-1 Channel Sequencing Mode

Consider a case where Auto-1 mode is selected to scan channels 2 (CH2), 5 (CH5), and 6 (CH6) as represented in Figure 58. The program register for Auto-1 mode must be programmed as described in Figure 58 before entering into this auto sequencing mode. The device enters into Auto-1 mode on receiving the Auto-1 mode command in the Nth frame. This step causes the device to find the first enabled channel in ascending order and switch the MUX for CH2 in the (N+1)th frame. In the (N+2)th frame, the ADC samples the signal on CH2, shifts out the conversion results, and the MUX also internally switches to CH5. In the (N+3)th frame, the ADC samples and shifts out the conversion result for CH5 and the MUX also internally switches to CH6. This process repeats until the last enabled channel is reached, in which case the process loops back to the first enabled channel. Entering Auto-1 mode from any other mode also causes the device to restart from the first enabled channel. However, modifying the contents of the Auto-1 mode program register while operating in Auto-1 mode causes the device to scan for the next enabled channel.

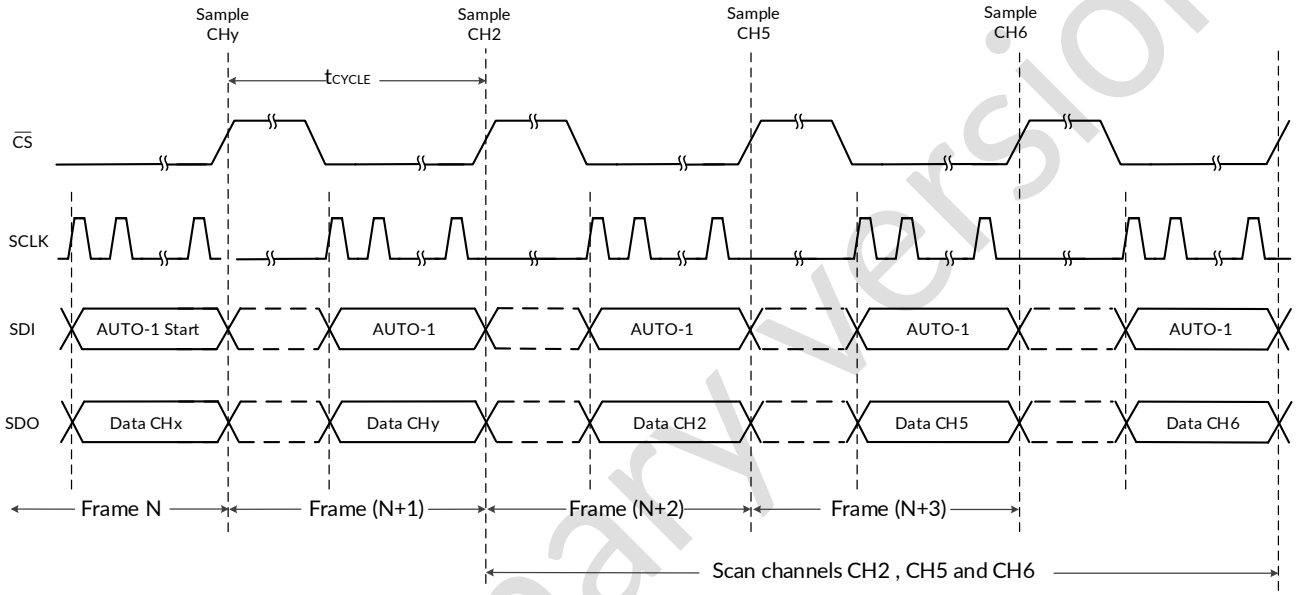
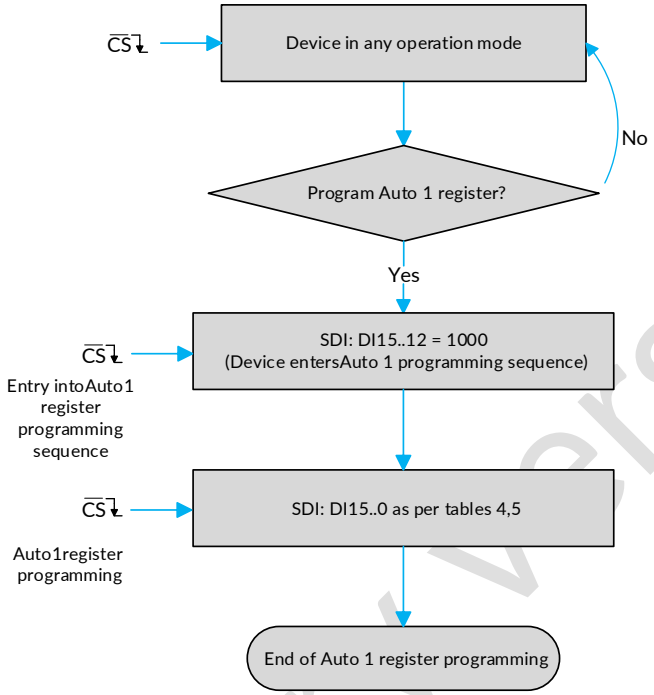


Figure 58. Example Auto-1 Mode Timing Diagram

Table 2. Mode Control Register Settings for Auto-1 Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION			
DI15-12	0001	0010	Selects Auto-1 Mode			
DI11	0	1	Enables programming of bits DI10-00.			
		0	Device retains values of DI10-00 from previous frame.			
DI10	0	1	The channel counter is reset to the lowest programmed channel in the Auto-1 Program Register			
		0	The channel counter increments every conversion (No reset)			
DI09-07	000	xxx	Do not care			
DI06	0	0	Selects 0 to VREF input range (Range 1)			
		1	Selects 0 to 2xVREF input range (Range 2)			
DI05	0	0	Device normal operation (no power down)			
		1	Device powers down on 16th SCLK falling edge			
DI04	0	0	SDO outputs current channel address of the channel on DO15..12 followed by 12 bit conversion result on DO11..00.			
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent 12-bit conversion result of the current channel.			
			DOI5	DOI4	DOI3	DOI2
			GPIO3	GPIO2	GPIO1	GPIO0
DI03-00	0000	GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below				
			DI03	DI02	DI01	DI00
			GPIO3	GPIO2	GPIO1	GPIO0

The Auto-1 Program Register is programmed (once on power up or reset) to pre-select the channels for the Auto 1 sequence. Auto-1 Program Register programming requires two $\overline{CS}$ frames for complete programming. In the first $\overline{CS}$ frame the device enters the Auto-1 register programming sequence and in the second frame it programs the Auto-1 Program Register. Refer to Table 2 for complete details.



NOTE: The device continues its operation in selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 59. Auto-1 Register Programming Flowchart

Table 3. Program Register Settings for Auto-1 Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION
FRAME 1			
DI15-12	NA	1000	Device enters Auto-1 program sequence. Device programming is done in the next frame.
DI11-00	NA	Do not care	
FRAME 2			
DI15-00	All 1s	1 (individual bit)	A particular channel is programmed to be selected in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; for example, DI15→Ch15,DI14→Ch14...DI00→Ch00
		0 (individual bit)	A particular channel is programmed to be skipped in the channel scanning sequence. The channel numbers are mapped one-to-one with respect to the SDI bits; for example, DI15→Ch15,DI14→Ch14...DI00→Ch00

Table 4. Mapping of Channels to SDI Bits

Device(1)	SDI BITS															
	DI15	DI14	DI13	DI12	DI11	DI10	DI09	DI08	DI07	DI06	DI05	DI04	DI03	DI02	DI01	DI00
16 Chan	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

(1) When operating in Auto-1 mode, the device only scans the channels programmed to be selected.

8.4.6 Operating in Auto-2 Mode

Figure 60 illustrates the steps involved in entering and operating in Auto-2 channel sequencing mode. Table 5 lists the mode control register settings for Auto-2 mode.

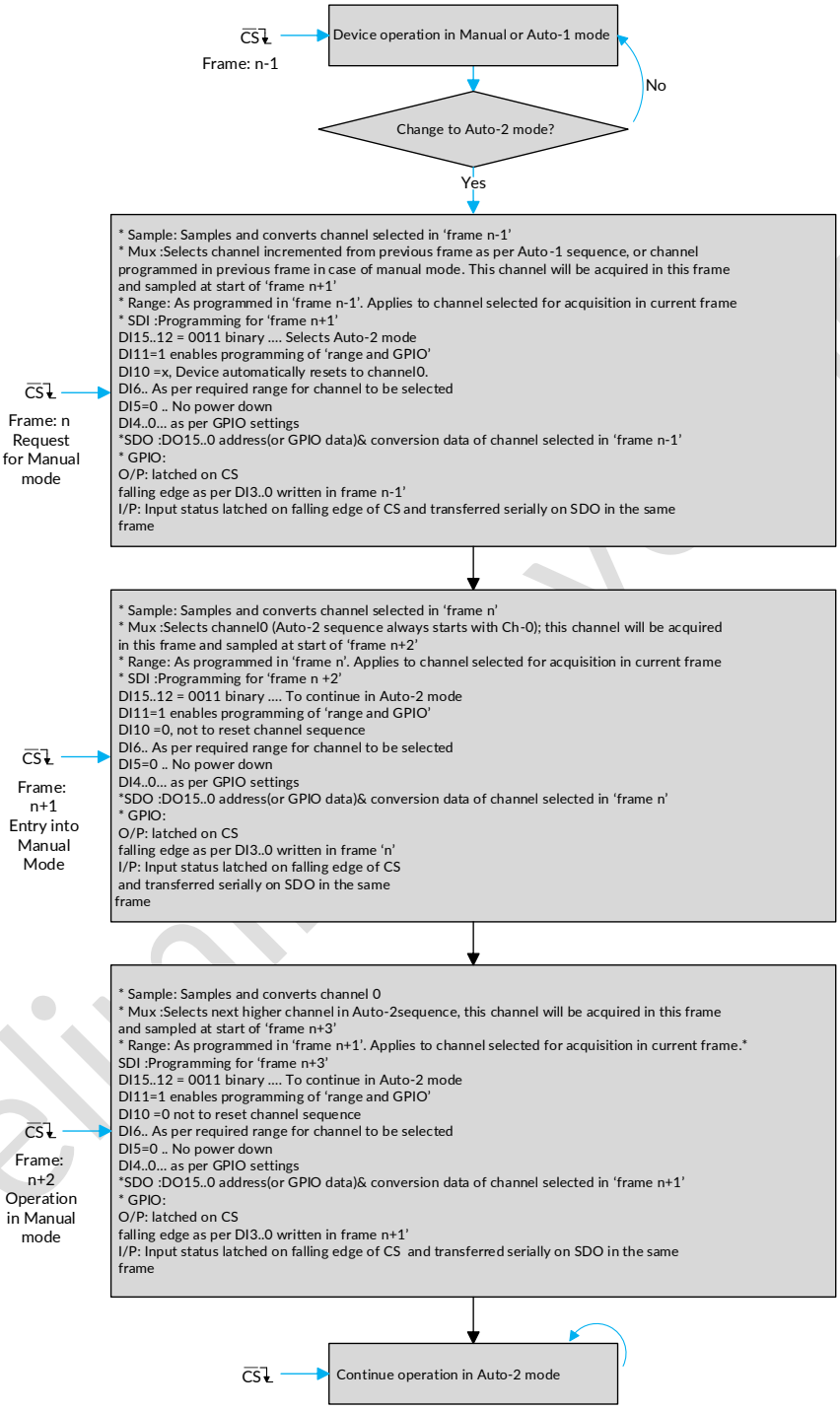


Figure 60. Entering and Running in Auto-2 Channel Sequencing Mode

Figure 61 shows an example in which Auto-2 mode is used to scan channels 0, 1, and 2. Auto-2 mode is selected to scan all channels until channel 2 (CH2) in ascending order by programming the Auto-2 register as described in Figure 61. The device enters Auto-2 mode on receiving the Auto-2 mode command in the Nth frame. This step causes the MUX to switch to CH0 in the (N+1)th frame. In the (N+2)th frame, the ADC samples and shifts out the conversion results for CH0 because the MUX internally switches to CH1. In the (N+3)th frame, the ADC samples and the shifts out the conversion result for CH1 and the MUX also switches to CH2, and so on. When this process reaches the maximum selected channel, CH2 in this case, the device returns to CH0 and repeats the cycle as long as the device remains in Auto-2 mode. Entering Auto-2 mode from any other mode also causes the device to restart from CH0. Additionally, modifying the contents of the for Auto-2 program register while operating in Auto-2 also causes the device to scan for restart from CH0.

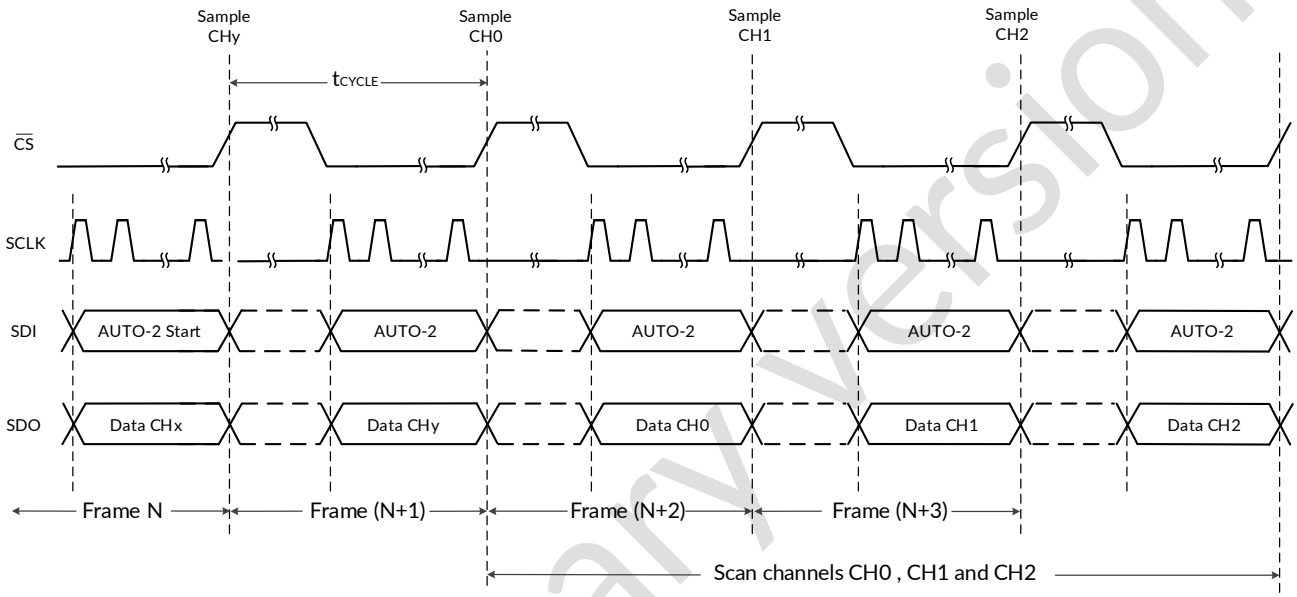
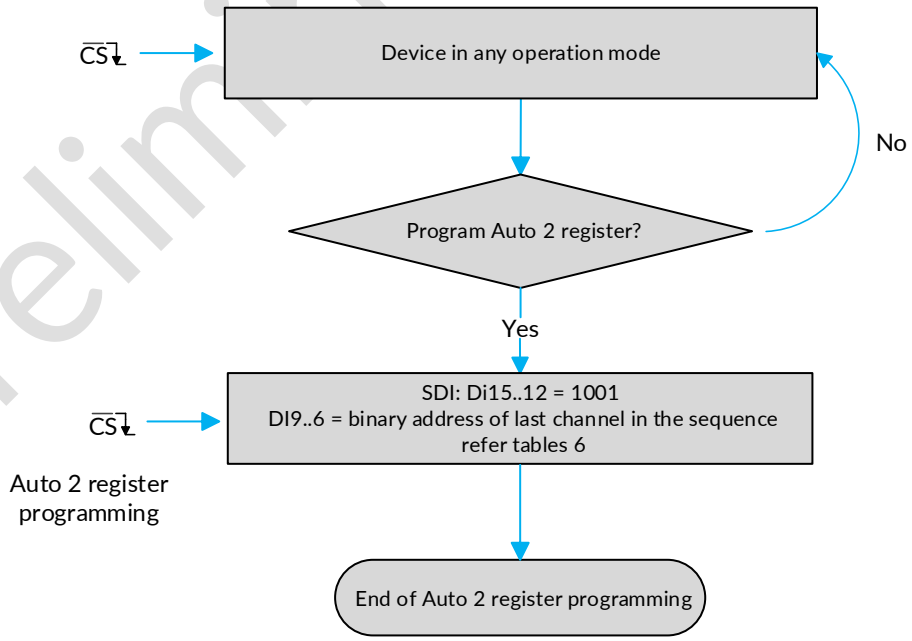


Figure 61. Example Auto-2 Mode Timing Diagram

Table 5. Mode Control Register Settings for Auto-2 Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION			
DI15-12	0001	0011	Selects Auto-2 Mode			
DI11	0	1	Enables programming of bits DI10-00.			
		0	Device retains values of DI10-00 from the previous frame.			
DI10	0	1	Channel number is reset to Ch-00.			
		0	Channel counter increments every conversion.(No reset).			
DI09-07	000	xxx	Do not care			
DI06	0	0	Selects VREF i/p range (Range 1)			
		1	Selects 2xVREF i/p range (Range 2)			
DI05	0	0	Device normal operation (no power down)			
		1	Device powers down on 16th SCLK falling edge			
DI04	0	0	SDO outputs current channel address of the channel on DO15..12 followed by 12 bit conversion result on DO11..00.			
		1	GPIO3-GPIO0 data (both input and output) is mapped onto DO15-DO12 in the order shown below. Lower data bits DO11-DO00 represent 12-bit conversion result of the current channel.			
			DOI5	DOI4	DOI3	DOI2
			GPIO3	GPIO2	GPIO1	GPIO0
DI03-00	0000	GPIO data for the channels configured as output. Device will ignore the data for the channel which is configured as input. SDI bit and corresponding GPIO information is given below				
			DI03	DI02	DI01	DI00
			GPIO3	GPIO2	GPIO1	GPIO0

The Auto-2 Program Register is programmed (once on powerup or reset) to pre-select the last channel (or sequence depth) in the Auto-2 sequence. Unlike Auto-1 Program Register programming, Auto-2 Program Register programming requires only 1 $\overline{CS}$ frame for complete programming. See Figure 62 and Table 6 for complete details.



NOTE: The device continues its operation in the selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 62. Auto-2 Register Programming Flowchart

Table 6. Program Register Settings for Auto-2 Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION
DI15-12	NA	1001	Auto-2 program register is selected for programming
DI11-10	NA	Do not care	
DI09-06	NA	aaaa	This 4-bit data represents the address of the last channel in the scanning sequence. During device operation in Auto-2 mode, the channel counter starts at CH-00 and increments every frame until it equals “aaaa”. The channel counter roles over to CH-00 in the next frame.
DI05-00	NA	Do not care	

8.4.7 Continued Operation in a Selected Mode

Once a device is programmed to operate in one of the modes, the user may want to continue operating in the same mode. Mode Control Register settings to continue operating in a selected mode are detailed in Table 7.

Table 7. Continued Operation in a Selected Mode

BITS	RESET STATE	LOGIC STATE	FUNCTION
DI15-12	0001	0000	The device continues to operate in the selected mode. In Auto-1 and Auto-2 modes the channel counter increments normally, whereas in the Manual mode it continues with the last selected channel. The device ignores data on DI11-DI00 and continues operating as per the previous settings. This feature is provided so that SDI can be held low when no changes are required in the Mode Control Register settings.
DI11-10	All ‘0’	Device ignores these bits when DI15-12 is set to 0000 logic state	

8.5 Programming

8.5.1 Digital Output

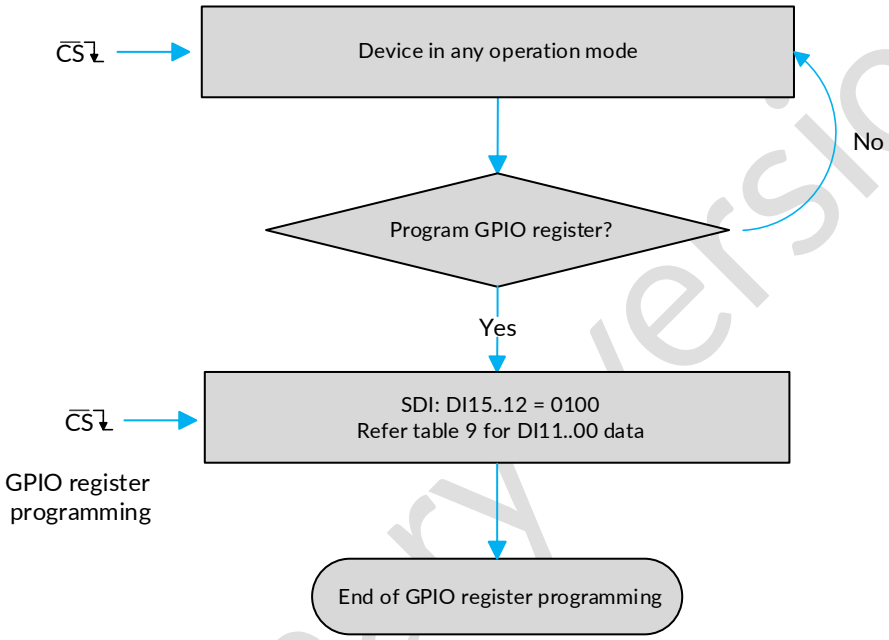
As discussed previously in Overview, the digital output of the RS1467 is SPI compatible. The following tables list the output codes corresponding to various analog input voltages.

Table 8. Ideal Input Voltages and Output Codes

DESCRIPTION		ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
Full scale range	Range 1 → V_{REF}	Range 2 → 2xV_{REF}		
Least significant bit (LSB)	V_{REF} / 4096	2V_{REF} / 4096	BINARY CODE	HEX CODE
Full scale	V_{REF} – 1LSB	2V_{REF} – 1LSB	1111 1111 1111	FFF
Midscale	V_{REF} / 2	V_{REF}	1000 0000 0000	800
Midscale– 1 LSB	V_{REF} / 2 – 2LSB	V_{REF} – 2LSB	0 111 1111 1111	7FF
Zero	0 V	0 V	0000 0000 0000	000

8.5.2 GPIO Registers

The device has four general purpose input and output (GPIO) pins. Each of the four pins can be independently programmed as general purpose output (GPO) or general purpose input (GPI). It is also possible to use the GPIOs for some pre-assigned functions (refer to Table 9 for details). GPO data can be written into the device through the SDI line. The device refreshes the GPO data on every $\overline{CS}$ falling edge as per the SDI data written in the previous frame. Similarly, the device latches GPI status on the $\overline{CS}$ falling edge and outputs it on SDO (if GPI is read enabled by writing DI04 = 1 during the previous frame) in the same frame starting on the $\overline{CS}$ falling edge. The details regarding programming the GPIO registers are illustrated in the flowchart in Figure 63. Table 9 lists the details regarding GPIO Register programming settings.



NOTE: The device continues its operation in the selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 63. GPIO Program Register Programming Flowchart

Table 9. GPIO Program Register Settings

BITS	RESET STATE	LOGIC STATE	FUNCTION
DI15-12	NA	0100	Device selects GPIO Program Registers for programming.
DI11-10	00	00	Do not program these bits to any logic state other than '00'
DI09		1	Device resets all registers in the next $\overline{CS}$ frame to the reset state shown in the corresponding tables (it also resets itself).
		0	Device normal operation
DI08		1	Device configures GPIO3 as the device power-down input.
		0	GPIO3 remains general purpose I or O.
DI07		1	Device configures GPIO2 as device range input.
		0	GPIO2 remains general purpose I or O.
DI06-04	000	000	GPIO1 and GPIO0 remain general purpose I or O.
		xx1	Device configures GPIO0 as 'high or low' alarm output. This is an active high output. GPIO1 remains general purpose I or O.
		010	Device configures GPIO0 as high alarm output. This is an active high output. GPIO1 remains general purpose I or O.
		100	Device configures GPIO1 as low alarm output. This is an active high output. GPIO0 remains general purpose I or O.
		110	Device configures GPIO1 as low alarm output and GPIO0 as a high alarm output. These are active high outputs.
Note: The following settings are valid for GPIO which are not assigned a specific function through bits DI08..04			
DI03	0	1	GPIO3 pin is configured as general purpose output.
		0	GPIO3 pin is configured as general purpose input.
DI03	0	1	GPIO2 pin is configured as general purpose output.
		0	GPIO2 pin is configured as general purpose input.
DI03	0	1	GPIO1 pin is configured as general purpose output.
		0	GPIO1 pin is configured as general purpose input.
DI03	0	1	GPIO0 pin is configured as general purpose output.
		0	GPIO0 pin is configured as general purpose input.

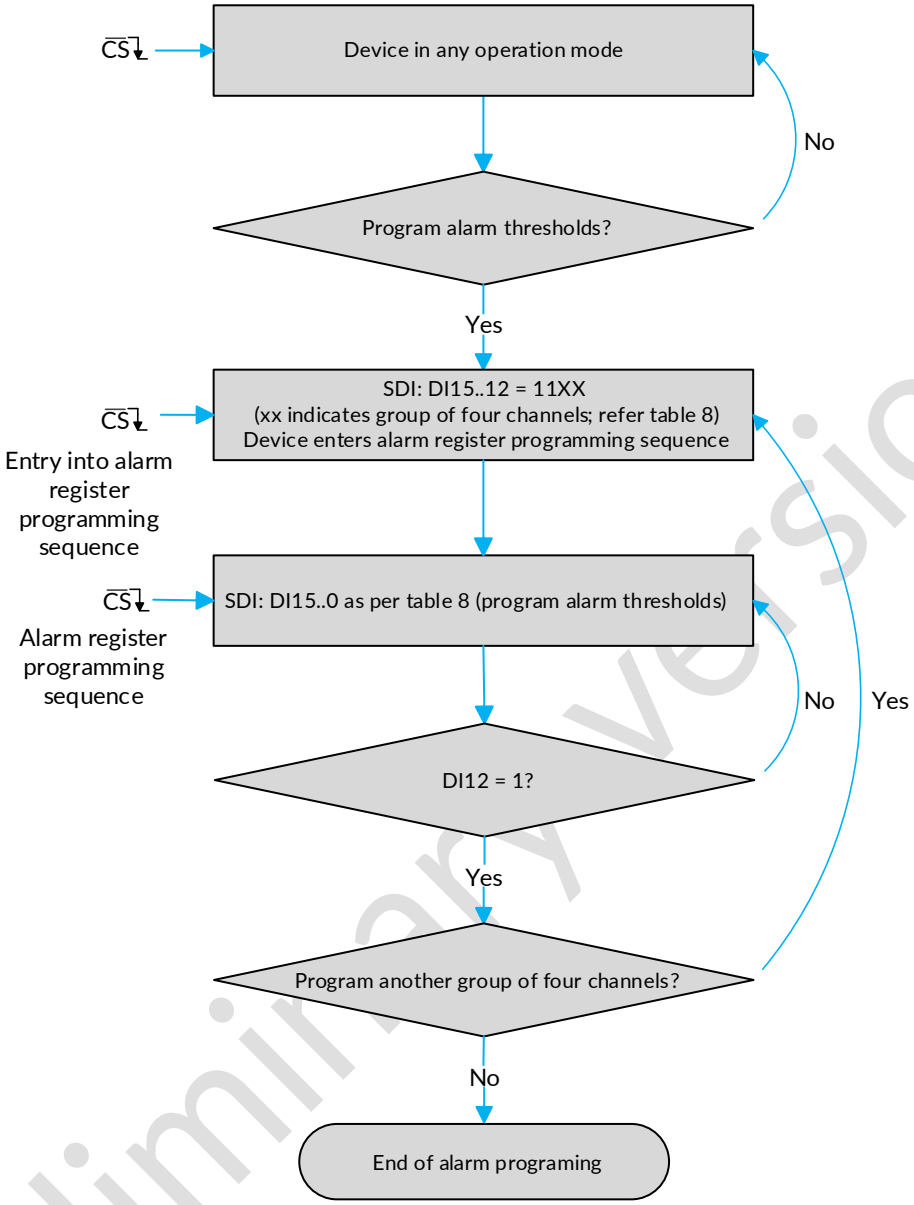
8.5.3 Alarm Thresholds for GPIO Pins

Each channel has two alarm program registers, one for setting the high alarm threshold and the other for setting the low alarm threshold. For ease of programming, two alarm programming registers per channel, corresponding to four consecutive channels, are assembled into one group (a total eight registers). There are four such groups for the device. The grouping of the various channels for the RS1467 is listed in Table 10. The details regarding programming the alarm thresholds are illustrated in the flowchart in Figure 64. Table 11 lists the details regarding the Alarm Program Register settings.

Table 10. Grouping of Alarm Program Registers

GROUP NO.	REGISTERS
0	High and low alarm for channel 0, 1, 2, and 3
1	High and low alarm for channel 4, 5, 6, and 7
2	High and low alarm for channel 8, 9, 10, and 11
3	High and low alarm for channel 12, 13, 14, and 15

Each alarm group requires 9 $\overline{CS}$ frames for programming their respective alarm thresholds. In the first frame the device enters the programming sequence and in each subsequent frame it programs one of the registers from the group. The device offers a feature to program less than eight registers in one programming sequence. The device exits the alarm threshold programming sequence in the next frame after it encounters the first 'Exit Alarm Program' bit high.



NOTE: The device continues its operation in the selected mode during programming. SDO is valid, however it is not possible to change the range or write GPIO data into the device during programming.

Figure 64. Alarm Program Register Programming Flowchart

Table 11. Alarm Program Register Settings

BITS	RESET STATE	LOGIC STATE	FUNCTION
FRAME1			
DI15-12	NA	1100	Device enters 'alarm programming sequence' for group 0
		1101	Device enters 'alarm programming sequence' for group 1
		1110	Device enters 'alarm programming sequence' for group 2
		1111	Device enters 'alarm programming sequence' for group 3
Note: DI15-12 = 11bb is the alarm programming request for group bb. Here 'bb' represents the alarm programming group number in binary format.			
DI11-00	NA	Do not care	
FRAME 2 ANDONWARDS			
DI15-14	NA	cc	Where "cc" represents the lower two bits of the channel number in binary format. The device programs the alarm for the channel represented by the binary number "bbcc". "bb" is programmed in the first frame.
DI13	NA	1	High alarm register selection
		0	Low alarm register selection
DI12	NA	1	Continue alarm programming sequence in next frame
		0	Exit Alarm Programming in the next frame. Note: If the alarm programming sequence is not terminated using this feature then the device will remain in the alarm programming sequence state and all SDI data will be treated as alarm thresholds.
DI11-10	NA	xx	Do not care
DI09-00	All ones for high alarm register and all zeros for low alarm register	This 10-bit data represents the alarm threshold. The 10-bit alarm threshold is compared with the upper 10-bit word of the 12-bit conversion result. The device sets off an alarm when the conversion result is higher (High Alarm) or lower (Low Alarm) than this number.	

9 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RS component specification, and RS does not warrant its accuracy or completeness. RS's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Applications

9.1.1 Unbuffered Multiplexer Output (MXO)

This application is the most typical application. In this application, a 220pF capacitor needs to be connected between AINP and AGND to achieve excellent offset performance.

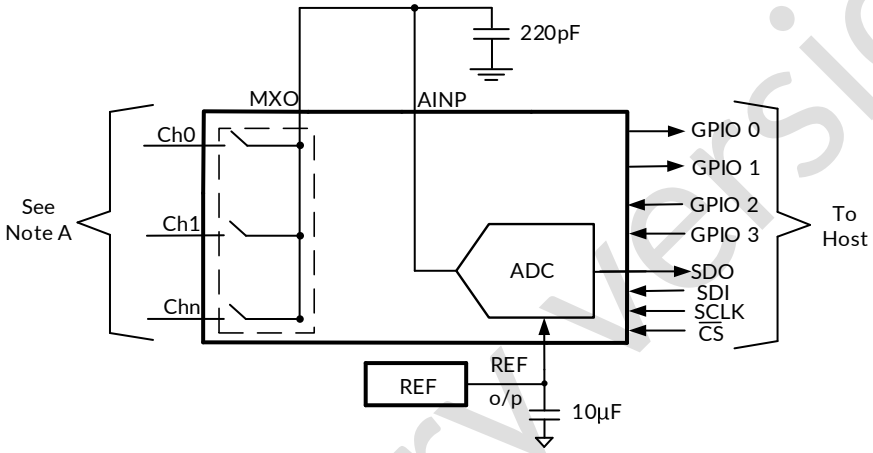


Figure 65. Application Diagram for an Unbuffered MXO

9.1.2 RS8701 Buffered Multiplexer Output (MXO)

The use of a buffer relaxes the R_{SOURCE} requirements to an extent. Charge from the sample-and-hold capacitor no longer dominates as a residual charge from a previous channel. Although having good performance is possible with a larger impedance using the RS8701, the output capacitance of the MXO also holds the previous channel charge and cannot be isolated, which limits how large the input impedance can finally be for good performance. In this configuration, the $1xV_{REF}$ range allows slightly higher impedance because the RS8701 slews approximately 2.5 V in contrast to the $2xV_{REF}$ range that requires the RS8701 to slew approximately 5 V.

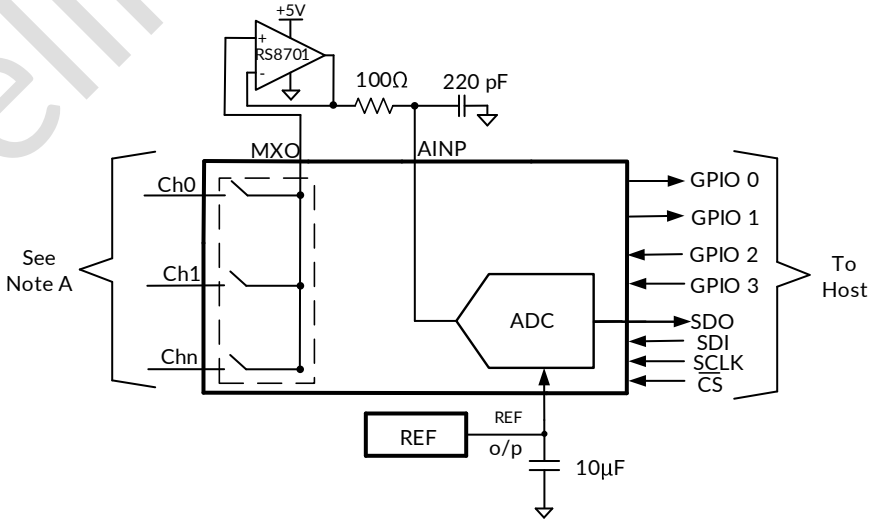


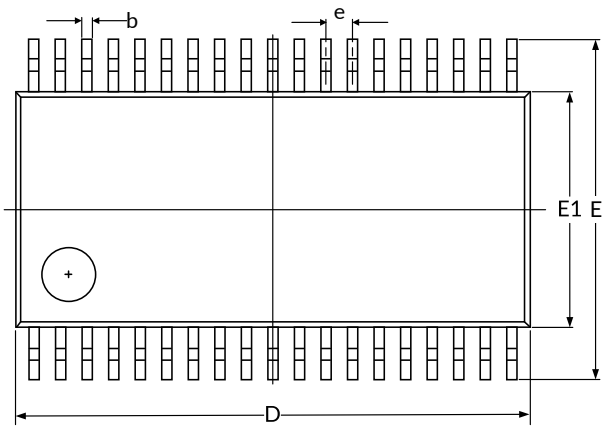
Figure 66. Application Diagram for a RS8701 Buffered MXO

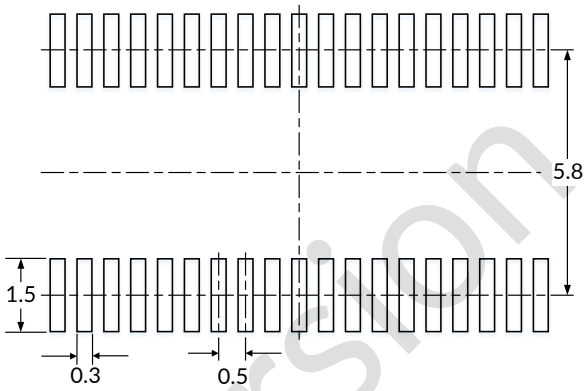
10 POWER SUPPLY RECOMMENDATIONS

The devices are designed to operate from an analog supply voltage (+VA) range from 2.7 V to 5.25 V and a digital supply voltage (+VBD) range from 1.7 V to 5.25 V. Both supplies must be well regulated. The analog supply is always greater than or equal to the digital supply. A 1-µF ceramic decoupling capacitor is required at each supply pin and must be placed as close as possible to the device.

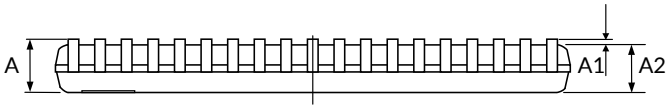
11 PACKAGE OUTLINE DIMENSIONS

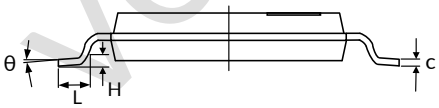
TSSOP38 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.170	0.270	0.007	0.011
c	0.090	0.200	0.004	0.008
D (1)	9.600	9.800	0.378	0.386
E	6.250	6.550	0.246	0.258
E1 (1)	4.300	4.500	0.169	0.177
e	0.500 (BSC) (2)		0.020 (BSC) (2)	
L	0.500	0.700	0.020	0.028
H	0.250 (TYP)		0.010 (TYP)	
θ	1°	7°	1°	7°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

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