RS74HC74-Q1 Dual Positive-Edge-Triggered D-Type Flip-Flop with set and reset

1 FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the Grade 1**
- **Operating Voltage Range: 1.65V to 5.5V**
- **Low Power Consumption: 10μA (Max)**
- **Operating Temperature Range: -40°C to 125°C**
- **Inputs Accept Voltage to 5.5V**
- **High Output Drive: ±24mA at V_{CC}=3.0V**
- **I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection**
- **Micro SIZE PACKAGES: TSSOP14**

2 APPLICATIONS

- **Network Switch**
- **Telecom Infrastructure**
- **Servers**
- **I/O Expanders**
- **LED Displays**

3 DESCRIPTIONS

The RS74HC74-Q1 dual positive-edge-triggered D-type flipflop is designed for 1.65V to 5.5V V_{CC} operation.

The RS74HC74-Q1 have individual data (nD), clock (nCP), set (n $\overline{S}$ D) and reset (n $\overline{R}$ D) inputs, and complementary nQ and n$\overline{Q}$ outputs. Data at the nD-input, that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition, is stored in the flip-flop and appears at the nQ output.

The RS74HC74-Q1 is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

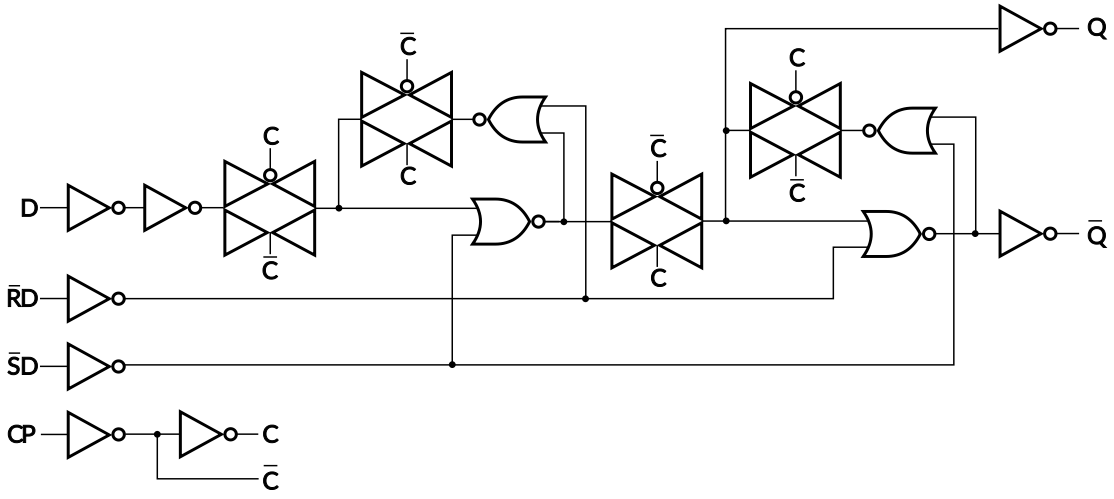
This device available in Green TSSOP14 packages. It operates over an ambient temperature range of -40°C to 125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS74HC74-Q1	TSSOP14	5.00mm×4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2025/04/14	Preliminary version completed
A.1	2025/09/01	Initial version completed

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	Lead finish/Ball material (2)	MSL Peak Temp (3)	PACKAGE MARKING (4)	PACKAGE OPTION
RS74HC74-Q1	RS74HC74XQ-Q1	-40°C ~125°C	TSSOP14	SN	MSL1-260°-Unlimited	RS74HC74	Tape and Reel,4000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

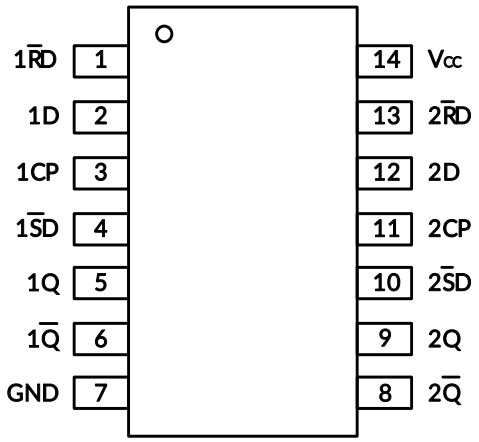
(2) There may be additional marking, which relates to the lot trace code information(data code and vendor code)， the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

(4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

6 PIN CONFIGURATIONS

TOP VIEW



TSSOP14

6.1 PIN DESCRIPTION

PIN	NAME	I/O TYPE (1)	FUNCTION
TSSOP14			
1	1R̄D	I	Asynchronous reset-direct input (active LOW)
2	1D	I	Data Input
3	1CP	I	Clock Input
4	1S̄D	I	Asynchronous set-direct input (active LOW)
5	1Q	O	Output
6	1Q̄	O	complement output
7	GND	-	Ground
8	2Q̄	O	complement output
9	2Q	O	Output
10	2S̄D	I	Asynchronous set-direct input (active LOW)
11	2CP	I	Clock Input
12	2D	I	Data Input
13	2R̄D	I	Asynchronous reset-direct input (active LOW)
14	V_{CC}	P	Supply

(1) I=input, O=output, P=power.

6.2 FUNCTION TABLE

INPUTS				OUTPUT	
nS̄D	nR̄D	nCP	nD	nQ	nQ̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (1)	H (1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

(1) This configuration is non-stable, that is, it does not persist when nS̄D or nR̄D returns to its inactive (high) level.
(2) H=High Voltage Level
L=Low Voltage Level
X=Don't Care

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high-impedance or power-off state (2)		-0.5	6.5	V
Vo	Voltage range applied to any output in the high or low state (2) (3)		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-50	mA
I_{OK}	Output clamp current	V_O<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance (4)	TSSOP14		90	°C/W
T_J	Junction temperature (5)		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 (1)	±4000	V
		Charged-Device Model (CDM), per AEC Q100-011	±1500	
		Latch-Up (LU), per AEC Q100-004	±200	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full=-40°C to 125°C, unless otherwise noted.) (1)

8.1 Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC}	Operating	1.65	5.5	V
High-level input voltage	V_{IH}	V_{CC}=1.65V to 1.95V	0.75×V_{CC}		V
		V_{CC}=2.3V to 2.7V	1.7		
		V_{CC}=3V to 3.6V	2		
		V_{CC}=4.5V to 5.5V	0.7×V_{CC}		
Low-level input voltage	V_{IL}	V_{CC}=1.65V to 1.95V		0.25×V_{CC}	V
		V_{CC}=2.3V to 2.7V		0.7	
		V_{CC}=3V to 3.6V		0.8	
		V_{CC}=4.5V to 5.5V		0.3×V_{CC}	
Input voltage	V_I		0	5.5	V
Output voltage	V_O		0	V_{CC}	V
High-level output current	I_{OH}	V_{CC}=1.65V		-4	mA
		V_{CC}=2.3V		-8	
		V_{CC}=3V		-16	
				-24	
		V_{CC}=4.5V		-32	
Low-level output current	I_{OL}	V_{CC}=1.65V		4	mA
		V_{CC}=2.3V		8	
		V_{CC}=3V		16	
				24	
		V_{CC}=4.5V		32	
Input transition rise or fall	Δt / Δv	V_{CC}=1.8V± 0.15V, 2.5V ± 0.2V		20	ns/V
		V_{CC}=3.3V± 0.3V		10	
		V_{CC}=5V± 0.5V		10	
Operating temperature	T_A		-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

8.2 DC Characteristics

PARAMETER		TEST CONDITIONS	V_{CC}	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OH}		I_{OH} = -100μA	1.65V to 5.5V	Full	V_{CC}-0.1			V
		I_{OH} = -4mA	1.65V		1.2			
		I_{OH} = -8mA	2.3V		1.9			
		I_{OH} = -16mA	3V		2.4			
		I_{OH} = -24mA			2.3			
		I_{OH} = -32mA	4.5V		3.8			
V_{OL}		I_{OL} = 100μA	1.65V to 5.5V	Full			0.1	V
		I_{OL} = 4mA	1.65V				0.45	
		I_{OL} = 8mA	2.3V				0.3	
		I_{OL} = 16mA	3V				0.4	
		I_{OL} = 24mA					0.55	
		I_{OL} = 32mA	4.5V				0.55	
I_I	All inputs	V_I=5.5V or GND	0V to 5.5V	+25°C		±0.1	±1	μA
				Full			±5	
I_{off}		V_I or V_O=5.5V	0	+25°C		±0.1	±1	μA
				Full			±10	
I_{CC}		V_I=5.5V or GND, I_O=0	1.65V to 5.5V	+25°C		0.1	1	μA
				Full			10	
ΔI_{CC}		One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND	3V to 5.5V	Full			500	μA
C_i (Input Capacitance)		V_I = V_{CC} or GND	3.3V	+25°C		3		pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

8.3 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	V_{CC}=1.8V		V_{CC}=2.5V		V_{CC}=3.3V		V_{CC}=5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			-40°C to 85°C		30		65		100		155	MHz
			-40°C to 125°C						100		155	
t_{pd}	nCP	nQ	-40°C to 85°C	4.8	23.5	2.2	15.5	2.2	11.5	1.4	9.2	ns
			-40°C to 125°C					2.2	12.5	1.4	9.5	
		$n\bar{Q}$	-40°C to 85°C	6	25.5	3	17	2.6	12.5	1.6	9.6	
			-40°C to 125°C					2.6	13.5	1.6	10	
	$n\bar{S}D$ or $n\bar{R}D$	nQ or $n\bar{Q}$	-40°C to 85°C	4.4	27	2.3	16	1.7	12	1.6	9.4	
			-40°C to 125°C					1.7	13	1.6	9.8	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

8.4 Operating Characteristics

T_A = +25°C

PARAMETER	TEST CONDITIONS	V_{CC} = 1.8V	V_{CC} = 2.5V	V_{CC} = 3.3V	V_{CC} = 5V	UNIT
		TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	f = 10 MHz	22	25	32	40	pF

8.5 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, V_{CC}=3.3V, unless otherwise noted.

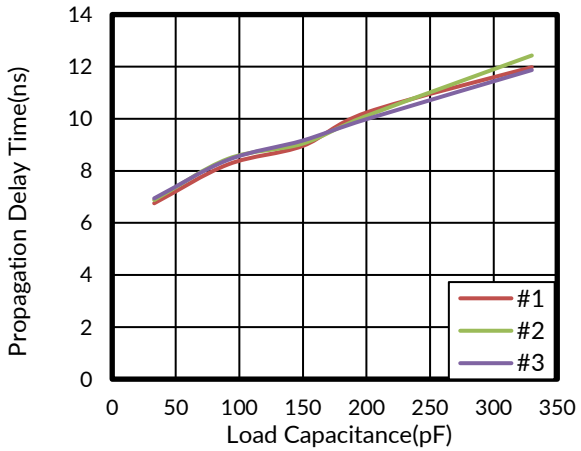


Figure 1. Propagation Delay (Low to High Transition) vs Load Capacitance

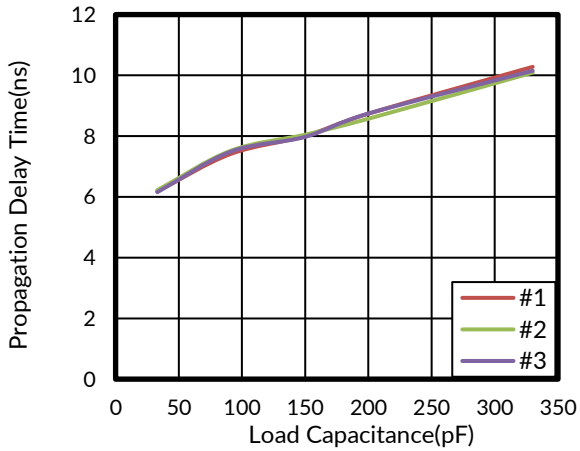
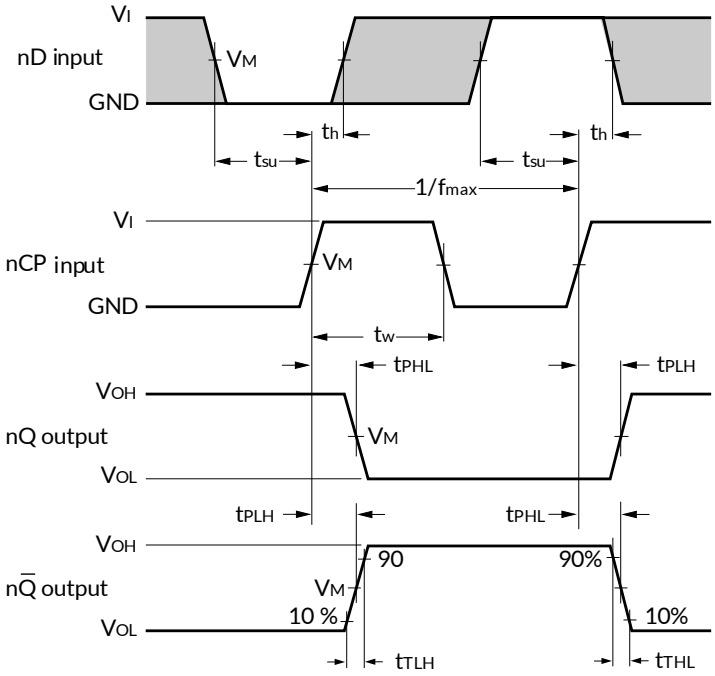


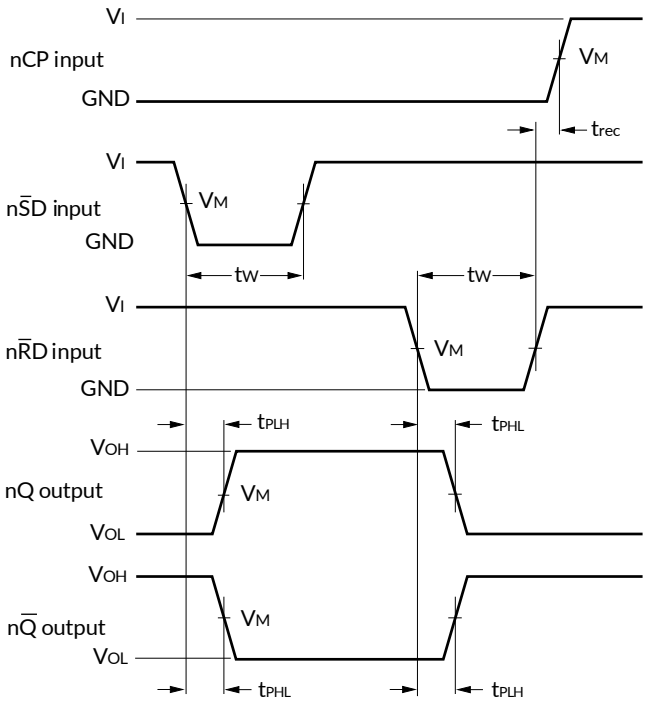
Figure 2. Propagation Delay (High to Low Transition) vs Load Capacitance

9 TEST CIRCUITS AND WAVEFORMS



Measurement points are given in Table 1.
V_{OL} and V_{OH} are typical output levels that occur with the output load.

Figure 3. Propagation delay input (CP) to output (Qn), output transition time, clock input (CP) pulse width and the maximum frequency (CP)

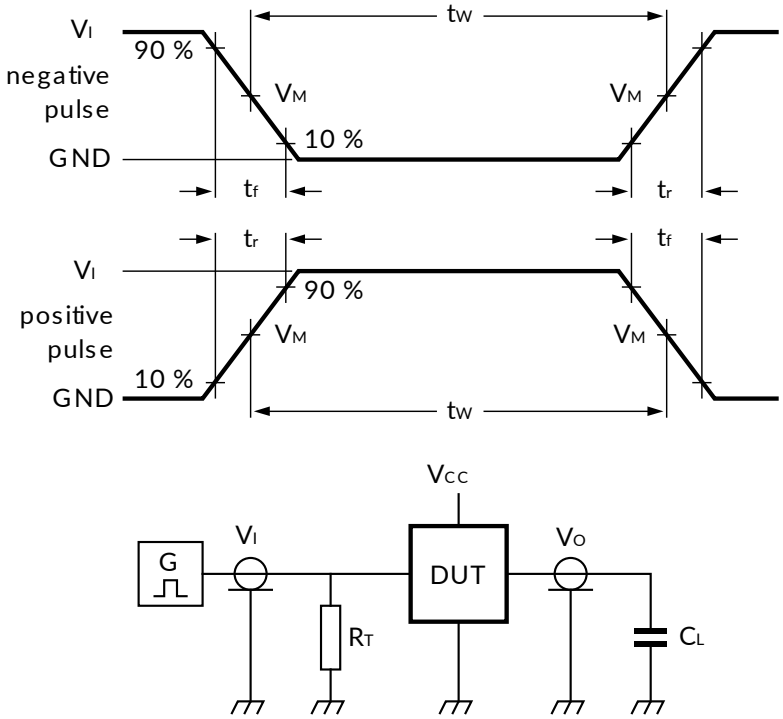


Measurement points are given in Table 1.
V_{OL} and V_{OH} are typical output levels that occur with the output load.

Figure 4. The set (nS̄D) and reset (nR̄D) input to output (nQ, nQ̄) propagation delays, set and reset pulse widths and the nS̄D, nR̄D to nCP recovery time

Table 1. Measurement points

Input	Output
V_M	V_M
$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 2.
Definitions test circuit:
R_T = Termination resistance should be equal to output impedance Z_O of the pulse generator.
C_L = Load capacitance including jig and probe capacitance.
R_L = Load resistance.
S1 = Test selection switch

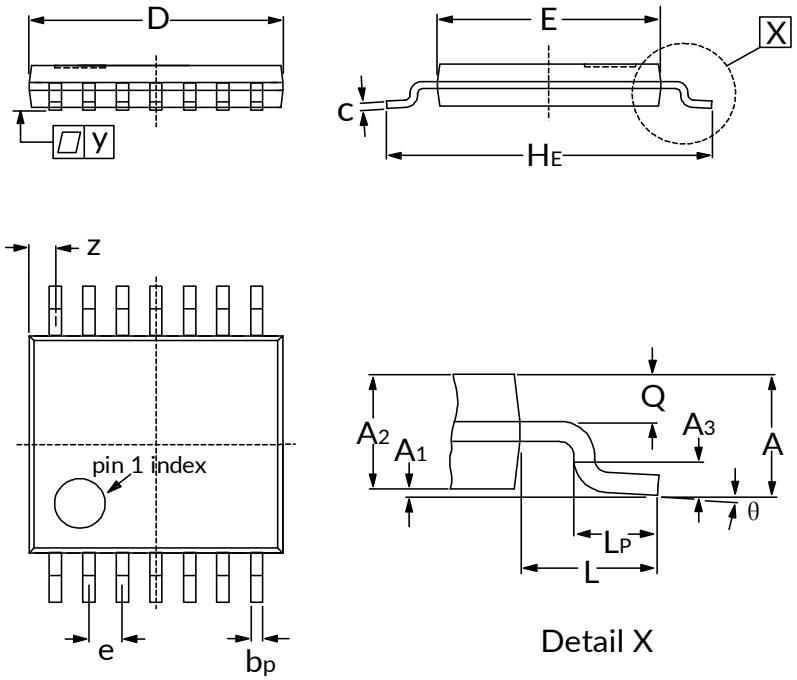
Figure 5. Test circuit for measuring switching times

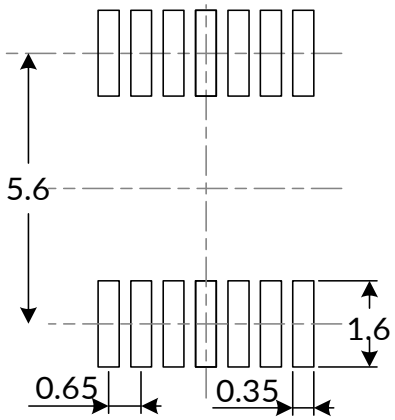
Table 2. Test data

Input		Load		Test
V_I	t_r, t_f	C_L	R_L	
V_{CC}	6ns	15pF, 50pF	1kΩ	t_{PHL}, t_{PLH}

10 PACKAGE OUTLINE DIMENSIONS

TSSOP14 (2)





RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A_1	0.050	0.150	0.002	0.006
A_2	0.800	1.050	0.031	0.041
A_3	0.25		0.010	
b_p	0.190	0.300	0.007	0.012
c	0.100	0.200	0.004	0.008
D (1)	4.900	5.100	0.193	0.201
E (1)	4.300	4.500	0.169	0.177
H_E	6.200	6.600	0.244	0.260
e	0.650		0.026	
L	1		0.039	
L_P	0.450	0.750	0.017	0.030
Q	0.300	0.490	0.012	0.019
Z	0.380	0.720	0.015	0.028
y	0.1		0.004	
θ	0°	8°	0°	8°

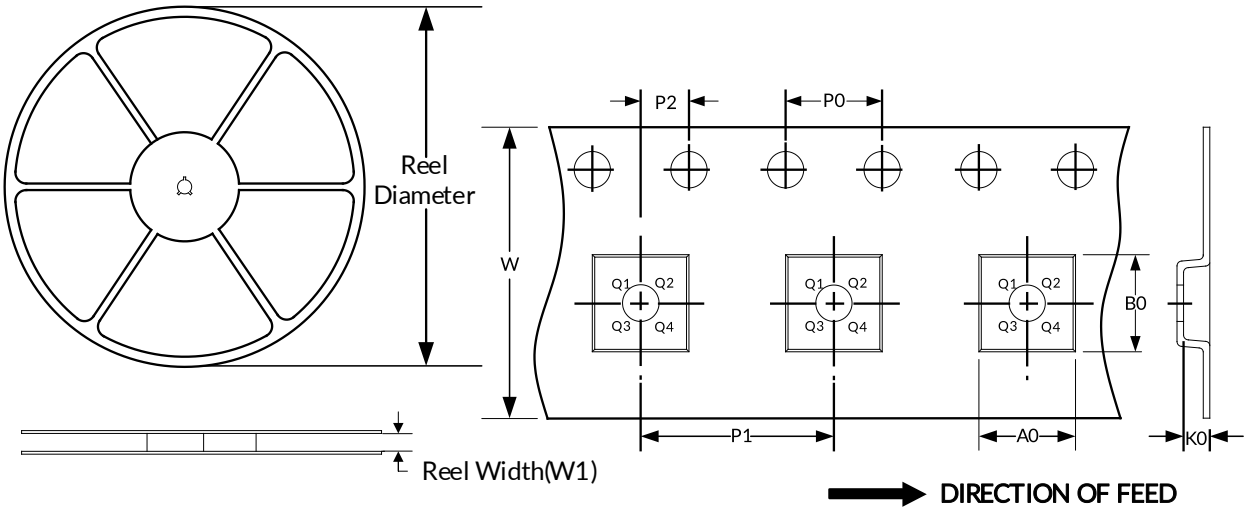
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. This drawing is subject to change without notice.

11 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP14	13”	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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