Automotive, Low-Distortion, Dual-Channel Operational Amplifier With Integrated Protection for Resolver Drive

1 FEATURES

- **RS8473-Q1 AEC-Q100 Qualification is Ongoing**
- **High Output Current Drive: 750 mA, Peak (Per Channel)**
  - **Replaces Discrete Op Amps and Transistors**
- **Wide Supply Range for Both Supplies (Up to 24 V)**
- **Overtemperature Shutdown**
- **Current Limit**
- **Shutdown Pin for Low I_Q Applications**
- **18 MHz Gain Bandwidth with 80 V/µs Slew Rate**
- **Package: ETSSOP14**

2 APPLICATIONS

- **Resolver-Based Automotive and Industrial Applications**
- **Inverter and Motor Control**
- **Brake System**
- **Electric Power Steering (EPS)**
- **Rearview Mirror Module**
- **Automotive eMirrors**
- **Servo Drive Power Stage Module**
- **Flight Control System**

3 DESCRIPTIONS

The RS8473-Q1 is a dual-power op amp with features and performance that make this device preferable for resolver-based applications. The high-gain bandwidth and slew rate of the device, along with a continuous high-output current-drive capability, make this device an excellent choice to provide the low distortion and differential high-amplitude excitation required for exciting the resolver primary coil. Current limiting and overtemperature detection enhance overall system robustness, especially when driving analog signals over wires that are susceptible to faults.

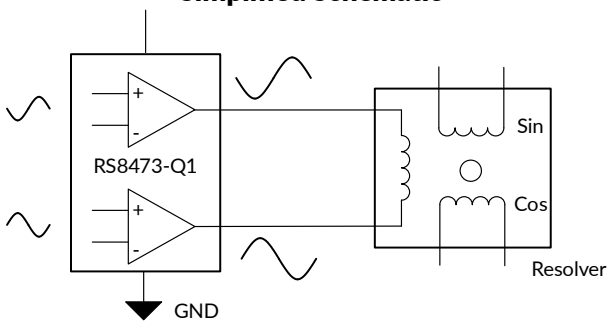
The small ETSSOP14 package with thermal pad and low $R_{\theta JA}$ allows high currents to be delivered to loads while minimizing board space. The higher gain bandwidth of the RS8473-Q1 allows the device to be configured as a filter stage while still providing high output drive, thus significantly reducing the total solution size of a resolver drive signal chain. This reduced solution size is a key advantage offered by the RS8473-Q1 when used in automotive and industrial applications.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS8473-Q1	ETSSOP14	5.00mm × 4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.0	2024/11/14	Preliminary version completed

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	Lead finish/Ball material (2)	MSL Peak Temp (3)	PACKAGE MARKING (4)	PACKAGE OPTION
RS8473-Q1	RS8473XEQ-Q1	-40°C~+125°C	ETSSOP14	SN	MSL1-260°-Unlimited	RS8473	Tape and Reel, 4000

NOTE:

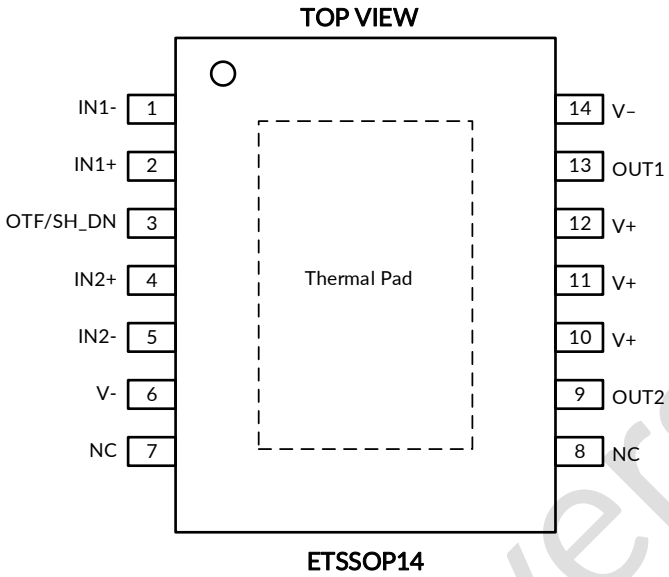
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

(4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

6 PIN CONFIGURATION AND FUNCTIONS



Pin Description

NAME	PIN	I/O (1)	DESCRIPTION
	ETSSOP14		
IN1-	1	I	Inverting op amp input for channel 1
IN1+	2	I	Noninverting op amp input for channel 1
OTF/SH_DN	3	I/O	Overtemperature flag and shutdown
IN2+	4	I	Noninverting op amp input for channel 2
IN2-	5	I	Inverting op amp input for channel 2
V-	6, 14	-	Negative supply pin (both negative supply pins must be used and connected together)
NC	7, 8	-	No internal connection (do not connect)
OUT2	9	O	Op amp output for channel 2
V+	10, 11, 12	-	Positive supply pin
OUT1	13	O	Op amp output for channel 1
Thermal Pad	Thermal Pad	-	Connect the exposed thermal pad to the most negative supply on the device, V–, for best thermal performance. The thermal pad can also be left floating electrically; the heat spread of the pad can be thermally maximized and conducted into the PCB.

(1) I = Input, O = Output.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_S	Supply voltage	Single-supply, V_S = (V+) – GND		26	V
		Dual-supply, V_S = (V+) – (V–)		±13	
	Signal input voltage	Common-mode	(V–) – 0.2	(V+) + 0.2	V
		Differential		(V+) – (V–) +0.2	
V_{OTF/SH_DN}	OTF/SH_DN pin voltage		(V–) – 0.2	(V+) + 0.2	V
	Signal input current			±10	mA
	Output short circuit (2)		Continues		
θ_{JA}	Package thermal impedance (3)	ETSSOP14		53	°C/W
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature (4)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.
(3) The package thermal impedance is calculated in accordance with JESD-51.
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 (1)	TBD	V
		Charged-Device Model (CDM), per AEC Q100-011	TBD	V
		Latch-Up (LU), per AEC Q100-004	TBD	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single-supply, V_S = (V+) – GND	5		24	V
		Dual-supply, V_S = (V+) – (V–)	±2.5		±12	
T_A	Operating temperature		-40		125	°C

7.4 Electrical Characteristics

at T_A = 25°C, V_S = V+ = 24V, V– = GND, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, Full [9] = –40°C to +125°C (unless otherwise noted) [1]

PARAMETER		TEST CONDITIONS	T_A	MIN[2]	TYP[3]	MAX[2]	UNIT
OFFSET VOLTAGE							
V_{OS}	Input Offset Voltage	V_S =24 V	25°C		±1	±3	mV
dV_{OS}/dT	Input Offset Voltage Drift	V_S =24 V	Full		±4.5	±10	µV/°C
PSRR	Power-Supply Rejection Ratio	V_S = 5 V to 24 V	25°C	93	102		dB
			Full	90			
INPUT BIAS CURRENT							
I_B	Input Bias Current [4] [5]		25°C		0.5	5	nA
			Full			20	nA
I_{OS}	Input Offset Current [5]		25°C		0.5	5	nA
			Full			20	nA
NOISE							
	Input Voltage Noise	V_S = 24 V, f = 0.1 Hz to 10 Hz	25°C		11		µVpp
e_N	Input Voltage Noise Density	f = 1 kHz	25°C		22		nV/√Hz
		f = 10 kHz	25°C		9		
INPUT VOLTAGE							
V_{CM}	Common-Mode Voltage		25°C	(V–)–0.1		(V+)+0.1	V
CMRR	Common-Mode Rejection Ratio	(V–) –0.1 V < V_{CM} < (V+) +0.1 V, 10 V < V_S < 24 V	25°C	69	76		dB
			Full	65			
		(V–) +2.5 V < V_{CM} < (V+) –2.5 V, 10 V < V_S < 24 V	25°C	80	89		
			Full	78			
OPEN-LOOP GAIN							
A_{OL}	Open-Loop Voltage Gain	(V–) +0.2 V < V_O < (V+) –0.2 V, R_L = 10kΩ, V_S = 24 V	25°C	115	132		dB
			Full	105			
FREQUENCY RESPONSE							
GBW	Gain-Bandwidth Product	V_S = 24 V	25°C		18		MHz
SR	Slew Rate [8]	V_S=24 V, 10-V step, Gain = +1	25°C		80		V/µs
t_S	Settling Time	To 0.1%, 10-V step, Gain = +1, C_L = 10 pF	25°C		0.30		µs
	Overload Recovery Time	V_{IN} × gain > V_S, V_S=24 V	25°C		0.09		µs
OUTPUT							
	Voltage Output Swing From Rail	I_{OUT} = ±5 mA	25°C		17	30	mV
I_{PK}	Transient Peak Output Current	Sinking	25°C		700		mA
		Sourcing	25°C		750		
I_{SC}	Short-Circuit Current [6] [7]	Sinking	25°C		450		mA
		Sourcing	25°C		550		
POWER SUPPLY							
I_Q	Total Quiescent Current	I_O = 0 A	25°C		8	10	mA
			Full			11	
I_{SD}	Shutdown Current	V_{OTF/SH_DN} = 0 V	25°C			215	µA

ENABLE							
V_{IH_OTF}	Enable High Input Voltage		25°C	1.2			V
V_{IL_OTF}	Enable Low Input Voltage		25°C			0.6	V
	Enable Hysteresis		25°C		200		mV
t_{OTF/SH_DN}	Enable Start-Up Time		25°C		5		μs
TEMPERATURE							
	Thermal Shutdown		25°C		150		°C
	Thermal Shutdown Recovery		25°C		135		°C

NOTE:
(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) Positive current corresponds to current flowing into the device.
(5) This parameter is ensured by design and/or characterization and is not tested in production.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
(7) Short circuit test is a momentary test.
(8) Number specified is the slower of positive and negative slew rates.
(9) Specified by characterization only.

7.5 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
at T_A= 25°C, V_S = 24 V, V_{CM} = V_S/2, and R_L = 10 kΩ (unless otherwise noted).

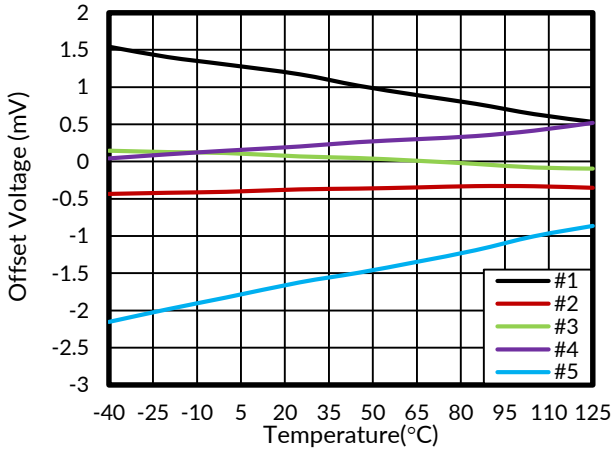


Figure 1. Offset Voltage vs Temperature

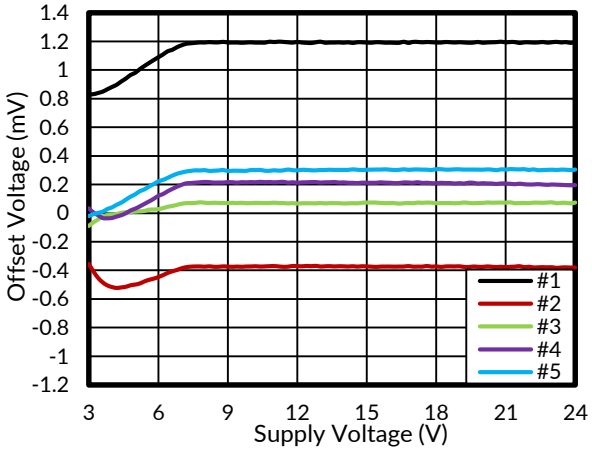


Figure 2. Offset Voltage vs Power Supply

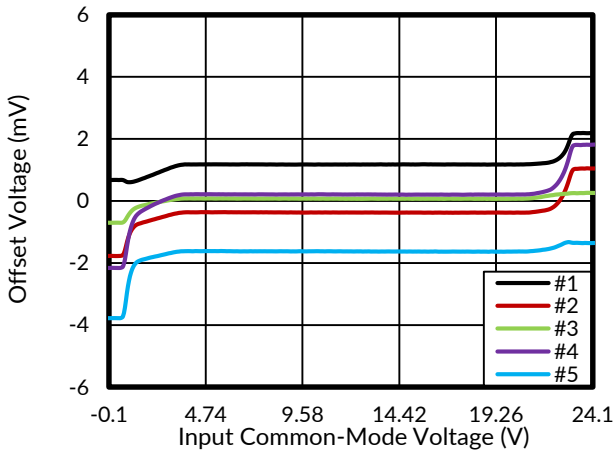


Figure 3. Offset Voltage vs Input Common-Mode Voltage

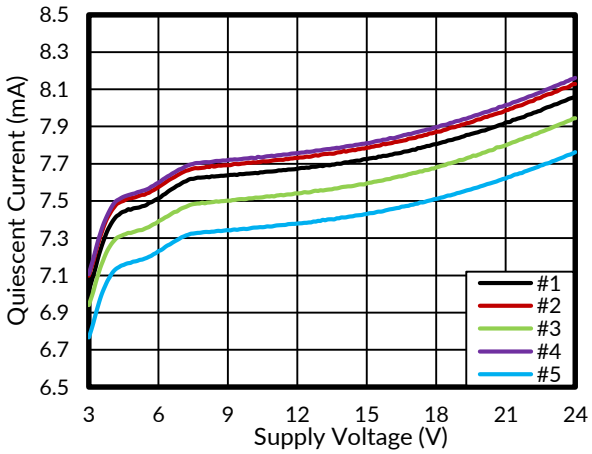


Figure 4. Quiescent Current vs Power Supply

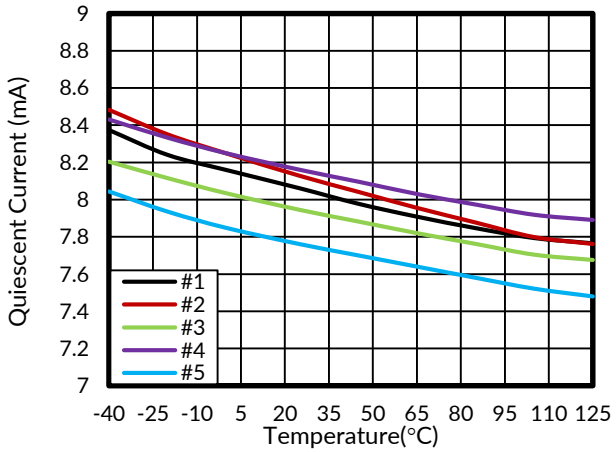


Figure 5. Quiescent Current vs Temperature

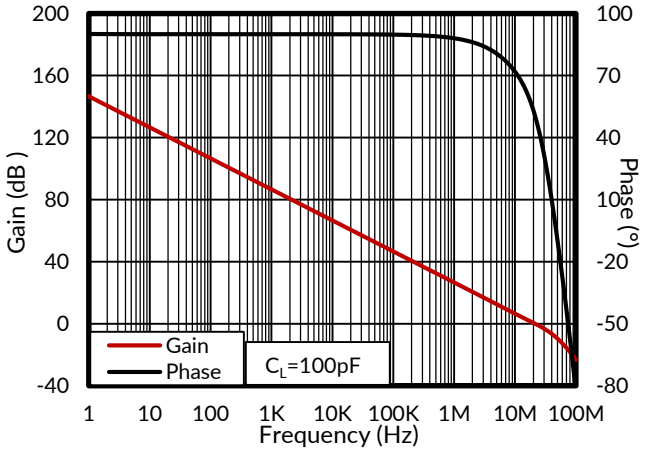


Figure 6. Open-Loop Gain and Phase vs Frequency

Typical Characteristics

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at T_A= 25°C, V_S = 24 V, V_{CM} = V_S/2, and R_L = 10 kΩ (unless otherwise noted).

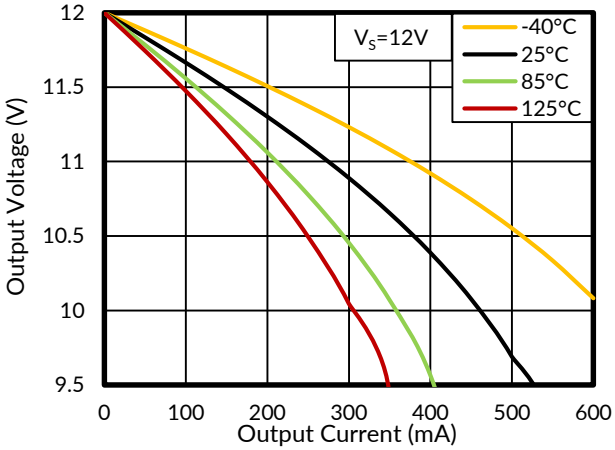

Figure 7. Output Voltage Swing vs Output Source Current

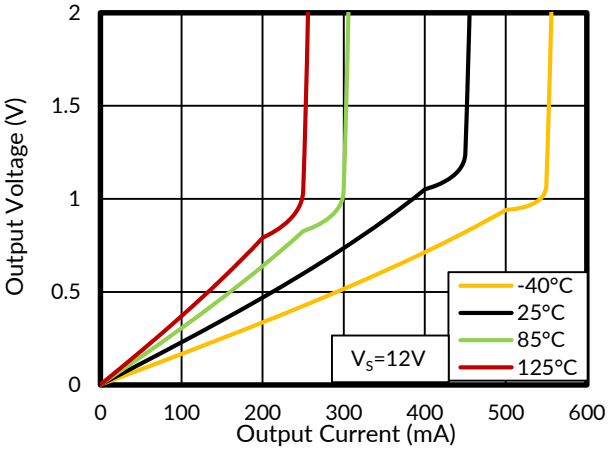

Figure 8. Output Voltage Swing vs Output Sink Current

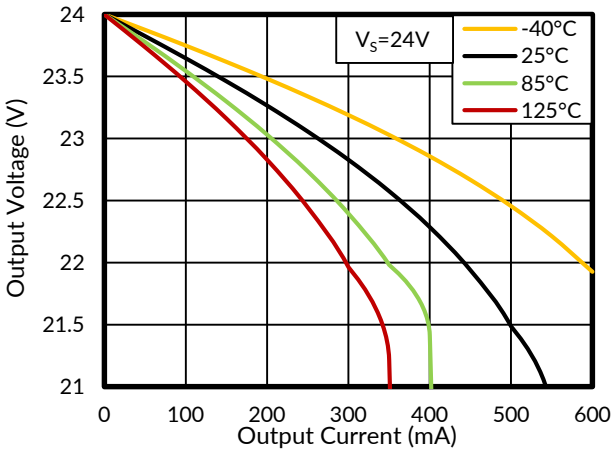

Figure 9. Output Voltage Swing vs Output Source Current

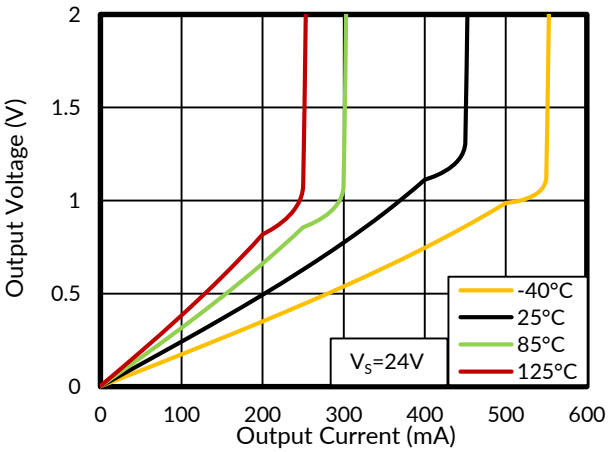

Figure 10. Output Voltage Swing vs Output Sink Current

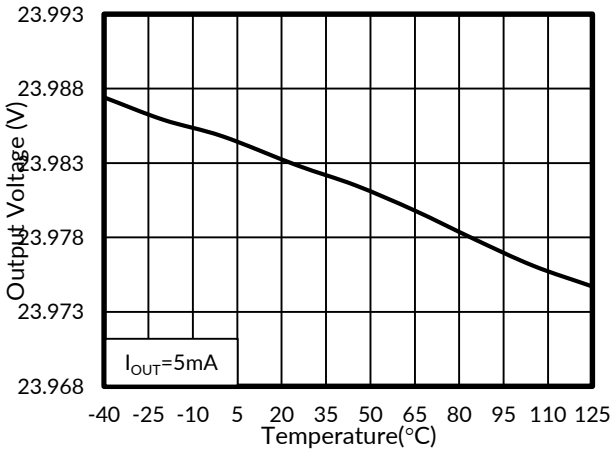

Figure 11. Output Voltage Swing (V_{OH}) vs Temperature

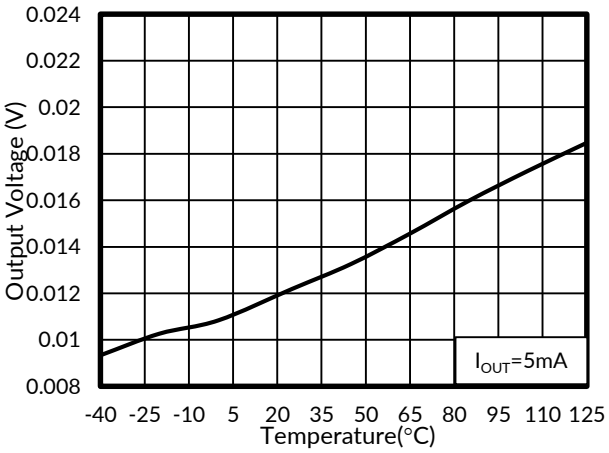

Figure 12. Output Voltage Swing (V_{OL}) vs Temperature

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
at T_A= 25°C, V_S = 24 V, V_{CM} = V_S/2, and R_L = 10 kΩ (unless otherwise noted).

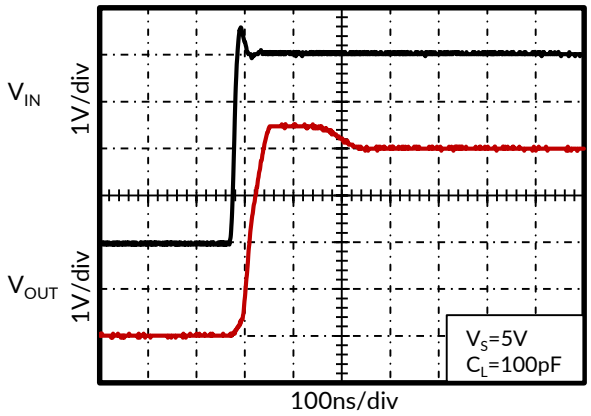

Figure 13. Large-Signal Rise Response

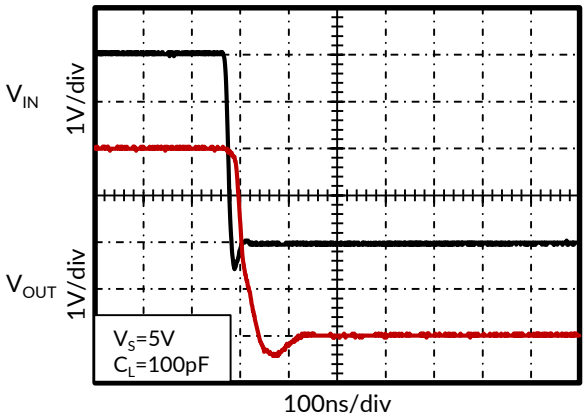

Figure 14. Large-Signal Fall Response

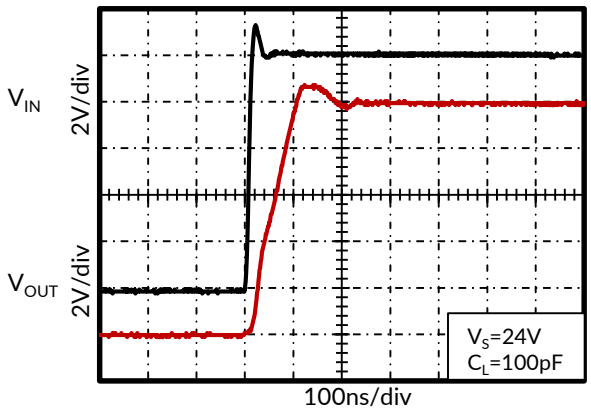

Figure 15. Large-Signal Rise Response

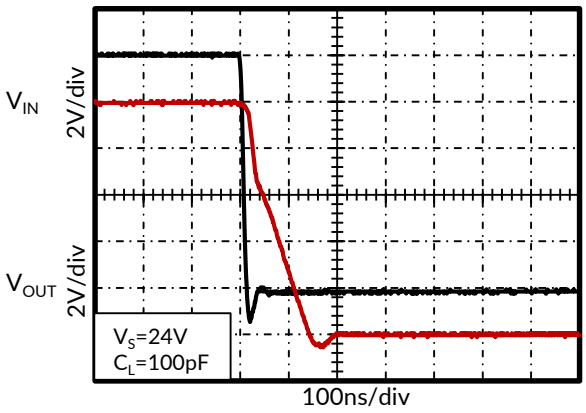

Figure 16. Large-Signal Fall Response

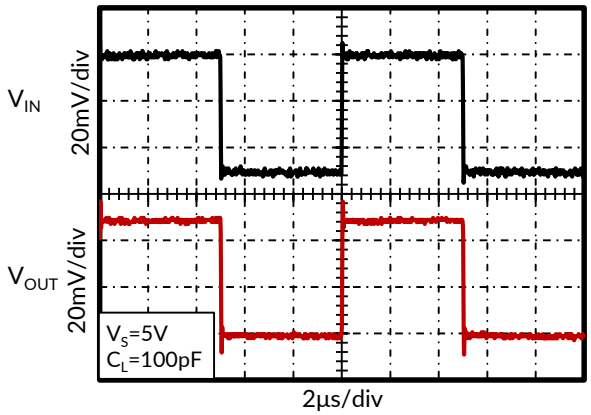

Figure 17. Small-Signal Step Response

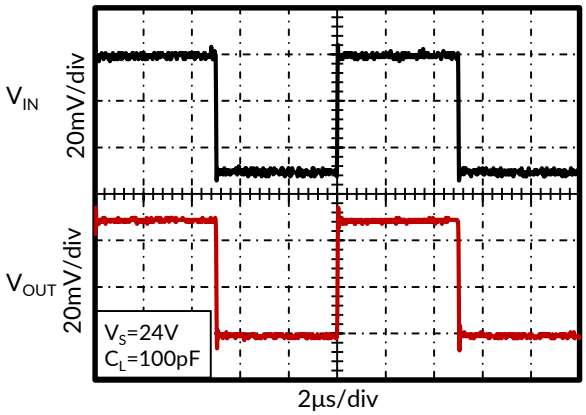

Figure 18. Small-Signal Step Response

Typical Characteristics

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at T_A= 25°C, V_S = 24 V, V_{CM} = V_S/2, and R_L = 10 kΩ (unless otherwise noted).

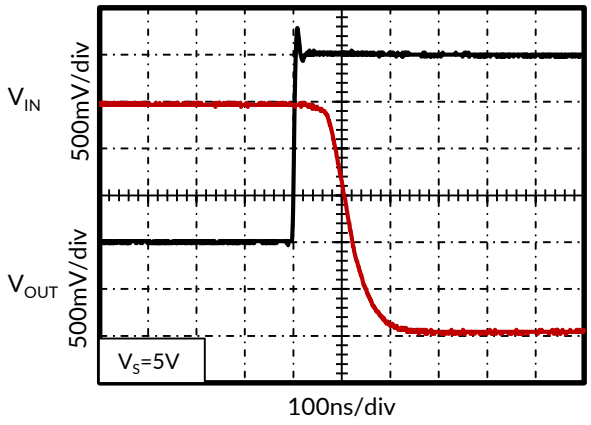

Figure 19. Positive Overload Recovery

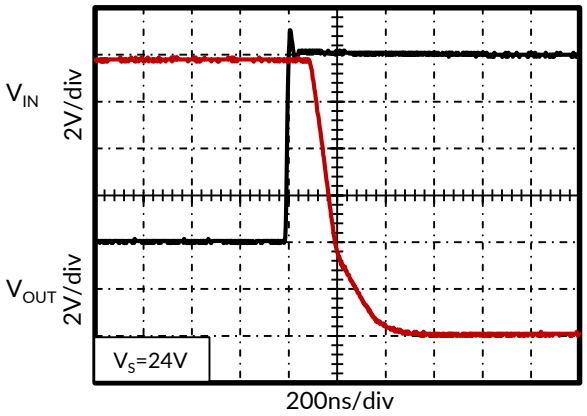

Figure 20. Positive Overload Recovery

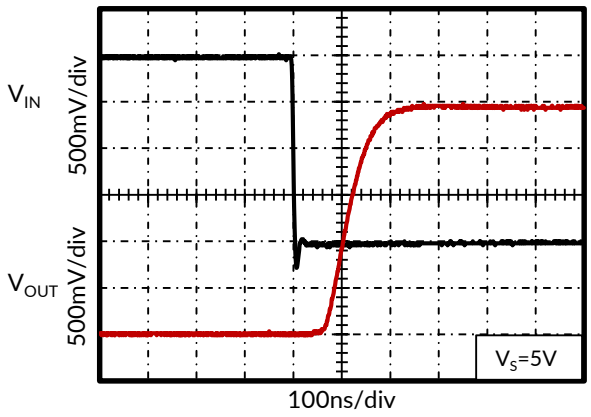

Figure 21. Negative Overload Recovery

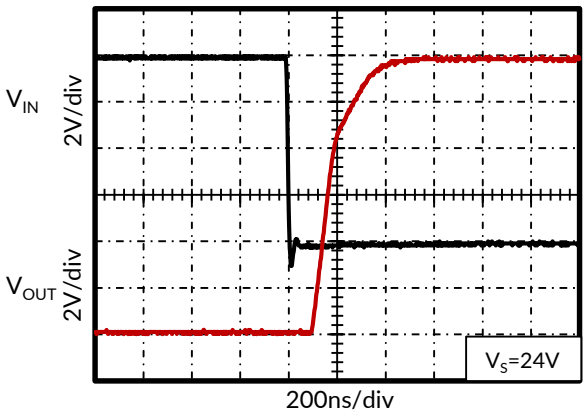

Figure 22. Negative Overload Recovery

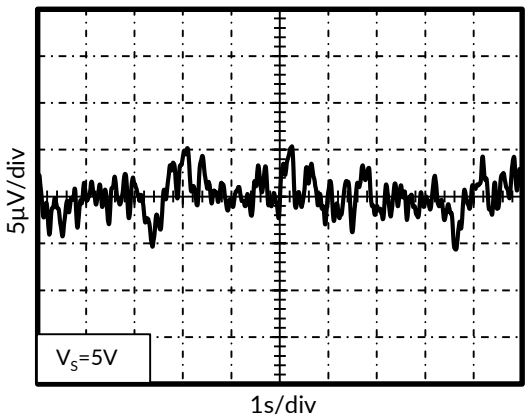

Figure 23. 0.1 Hz to 10 Hz Noise

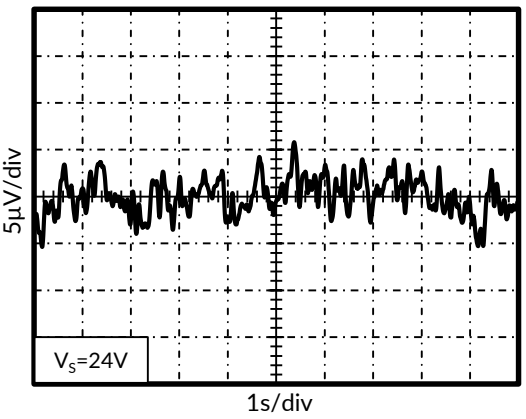

Figure 24. 0.1 Hz to 10 Hz Noise

Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
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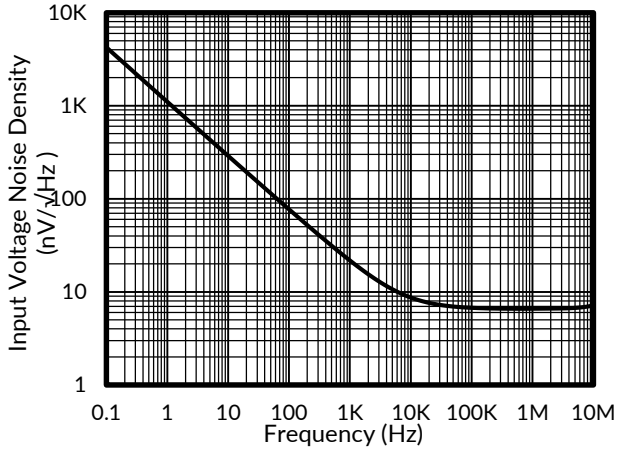


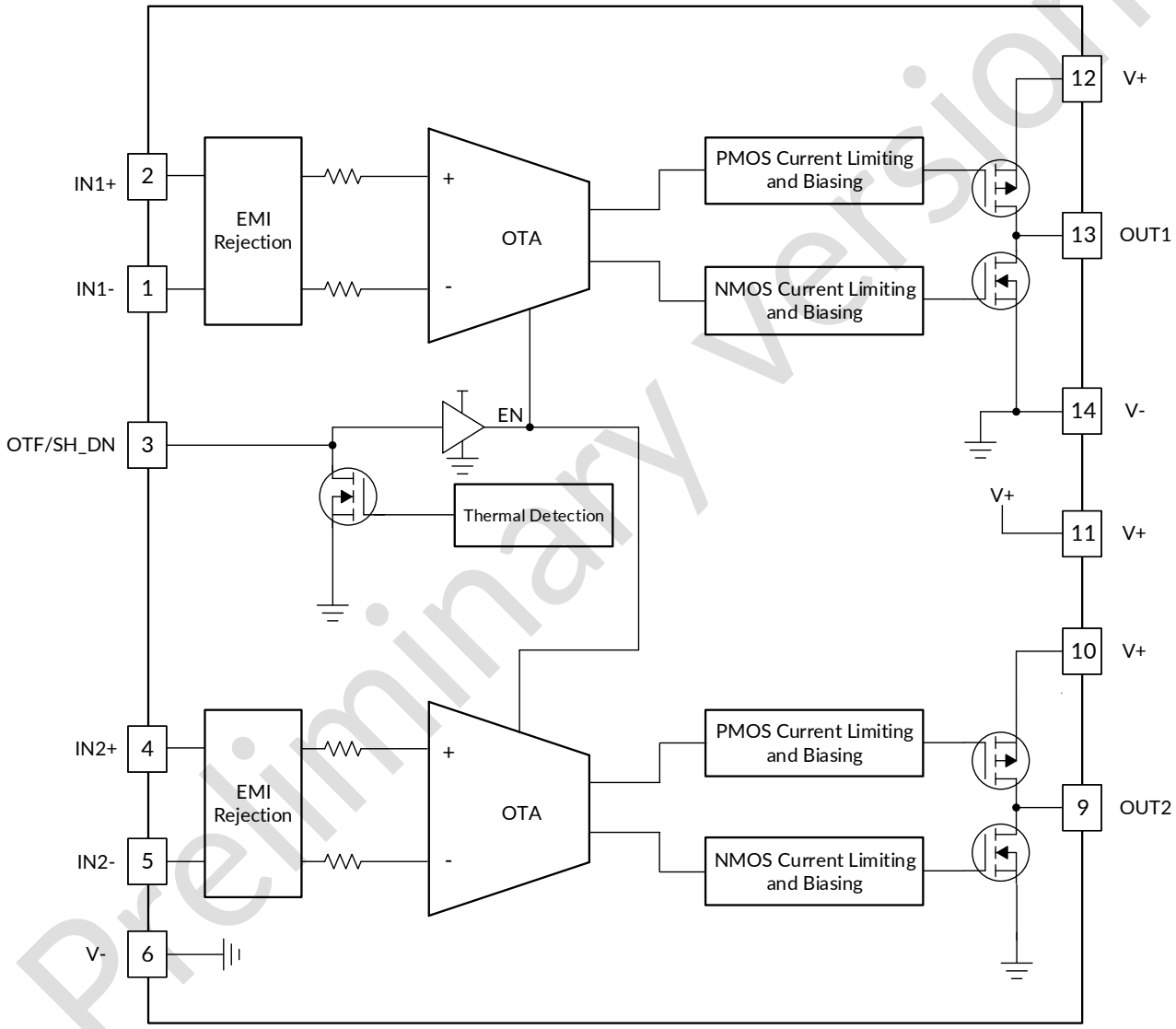
Figure 25. Input Voltage Noise Density vs Frequency

8 DETAILED DESCRIPTION

8.1 Overview

The RS8473-Q1 is a dual-power op amp qualified for use in automotive applications. Key features for this device are low offset voltage, high output current drive capability, and high FPBW capability. The device also offers protection features such as thermal shutdown and current limit. The ETSSOP14 package minimizes board space and power dissipation.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Overtemperature and Shutdown Pin (OTF/SH_DN)

The overtemperature and shutdown pin, OTF/SH_DN, is bidirectional and allows both op amps to be put into a low I_Q state when forced low or to less than V_{IL_OTF}. As a result of being bidirectional, and the respective enable and disable functionality, this pin must be pulled high or greater than V_{IH_OTF} through a pullup resistor.

When the junction temperature of the RS8473-Q1 exceeds the specified limits, OTF/SH_DN goes low to alert the application that both the outputs have turned off because of an overtemperature event.

When OTF/SH_DN is pulled low and the op amps are shut down, the op amps are in an open loop, even when there is negative feedback applied. This occurrence is due to the loss of the open-loop gain in the op amps when the biasing is disabled.

8.3.2 Thermal Shutdown

If the die temperature exceeds safe limits, all outputs are disabled, and the OTF/SH_DN pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The OTF/SH_DN pin is released after operation has resumed.

When operating the die at a high temperature, the op amp toggles on and off between the thermal shutdown hysteresis. In this event, the safe limits for the die temperature must be taken in to account. Do not continuously operate the device in thermal hysteresis for long periods of time.

8.3.3 Current-Limit and Short-Circuit Protection

Each op amp in the RS8473-Q1 has separate internal current limiting for the PMOS (high-side) and NMOS (low-side) output transistors. If the output is shorted to ground, then the PMOS (high-side) current limit is activated, and limits the current to 550 mA nominally. If the output is shorted to supply, then the NMOS (low-side) current limit is activated and limits the current to 450 mA nominally at 25°C. The current limit value is inversely proportional to temperature; therefore, the current limit value increases at low temperatures.

When current is limited, the safe limits for the die temperature must be taken in to account. With too much power dissipation, the die temperature can surpass thermal shutdown limits; the op amp shuts down and reactivates after the die has fallen below thermal limits.

8.3.4 Input Common-Mode Range

The input common-mode range of the RS8473-Q1 is between (V–) – 0.1 V and (V+) + 0.1 V. Staying within this range allows the op amps to perform and operate within specification. Operating beyond these limits can cause distortion and nonlinearities.

8.3.5 Reverse Body Diodes in Output-Stage Transistors

Designed as a high-voltage, high current operational amplifier, the RS8573-Q1 delivers robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. Different load conditions change the ability of the amplifier to swing close to the rails.

Each output transistor has internal reverse diodes between drain and source that conduct if the output is forced to greater than the supply or less than ground (reverse current flow). These diodes can be used as flyback protection in inductive-load-driving applications. Limit the use of these diodes to pulsed operation in order to minimize junction temperature overheating due to ($V_F \times I_F$). Internal current-limiting circuitry does not operate when current is flown in the reverse direction and the reverse diodes are active.

8.3.6 EMI Filtering

Op amps vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op-amp pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The RS8473-Q1 incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter.

8.4 Device Functional Modes

8.4.1 Open-Loop and Closed-Loop Operation

As a result of the very-high, open-loop dc gain of the RS8473-Q1, the device functions as a comparator in open loop for most applications. A majority of electrical characteristics are verified in negative feedback, closed-loop configurations. Certain dc electrical characteristics, like offset, may have a higher drift across temperature and lifetime when continuously operated in open loop over the lifetime of the device.

8.4.2 Shutdown

When the OTF/SH_DN pin is grounded, the op amp shuts down to a low I_Q state and does not operate; the op amp outputs go to a high-impedance state.

Table 1. Shutdown Truth Table

PIN NAME	LOGIC STATE	OP AMP STATE
OTF/SH_DN	High (> VIH_OTF)	Operating
	Low (< VIL_OTF)	Shutdown (low I_Q state)

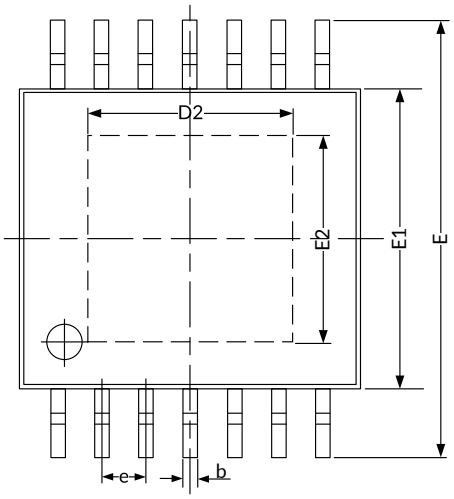
9 LAYOUT

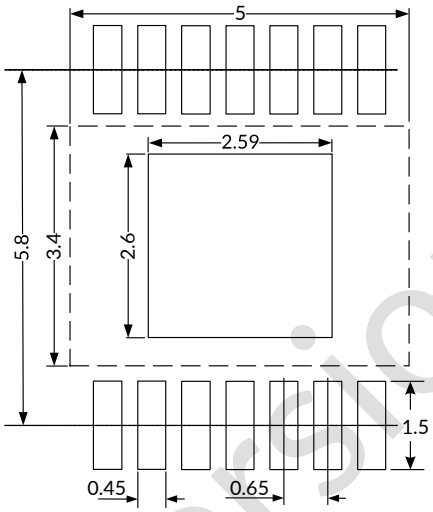
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1 µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If keeping the traces separate is not possible, then cross the sensitive trace perpendicular, as opposed to in parallel with the noisy trace.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.

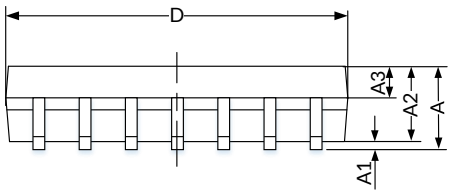
10 PACKAGE OUTLINE DIMENSIONS

ETSSOP14 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.035	0.041
A3	0.390	0.490	0.015	0.019
b	0.200	0.280	0.008	0.011
c	0.130	0.170	0.005	0.007
D (1)	4.900	5.100	0.193	0.201
D2	2.260		0.089	
E2	2.410		0.095	
E1 (1)	4.300	4.500	0.169	0.177
E	6.200	6.600	0.244	0.260
e	0.650 BSC (2)		0.026 BSC (2)	
L	0.450	0.750	0.018	0.030
L1	1.000 BSC (2)		0.039 BSC (2)	
θ	0°	8°	0°	8°

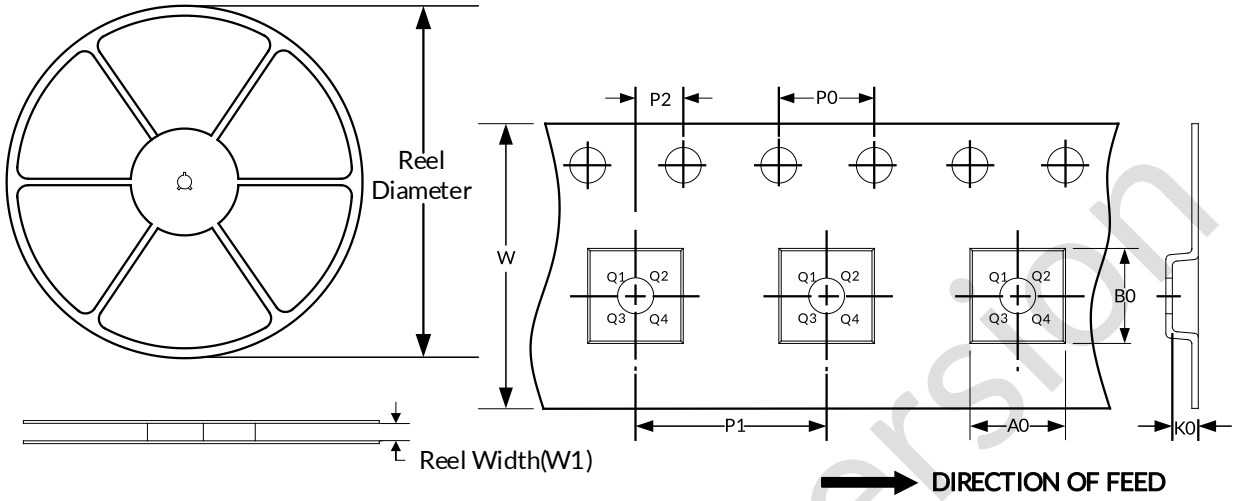
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

11 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
ETSSOP14	13”	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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