

RS911xC 3.3-V and 2.5-V LVCMOS High-Performance Clock Buffer Family

1 FEATURES

- **High-Performance 1:2, 1:3, 1:4 LVCMOS Clock Buffer Family**
- **Supply Voltage: 3.3 V or 2.5 V**
 $f_{max} = 250 \text{ MHz}$ for 3.3 V
 $f_{max} = 180 \text{ MHz}$ for 2.5 V
- **Operating Temperature Range: -40°C to 85°C**
- **Available in 8-Pin TSSOP Package**

2 APPLICATIONS

- **General-Purpose Communication, Industrial, and Consumer Applications**

3 DESCRIPTIONS

Three different fan-out variations, 1:2 to 1:4, are available. All of the devices are pin-compatible to each other for easy handling.

All family members share the same high performing characteristics such as low skew, and wide operating temperature range.

The RS911xC supports an asynchronous output enable control (1G) which switches the outputs into a low state when 1G is low.

The RS911xC family operates in a 2.5-V and 3.3-V environment and are characterized for operation from -40°C to 85°C .

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS9112C	TSSOP8	3.00 mm × 4.40 mm
RS9113C		
RS9114C		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Functional Block Diagram

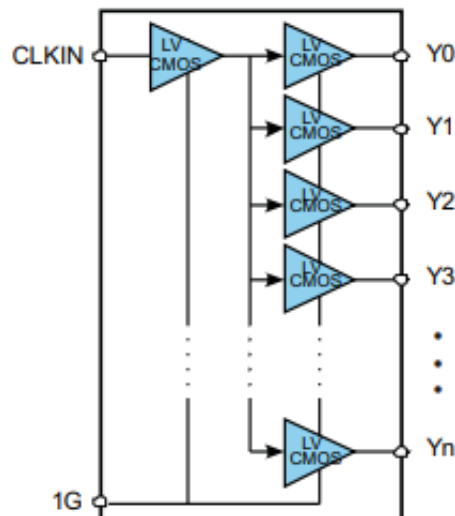


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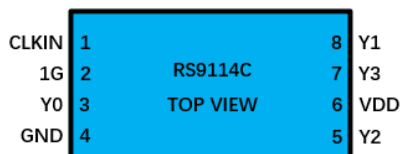
5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2024/02/27	Initial version completed

6 Pin Configuration and Functions

PW Package 8-Pin TSSOP Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	RS9112C	RS9113C	RS9114C		
LVC MOS CLOCK INPUT					
CLKIN	1	1	1	Input	Input Pin
CLOCK OUTPUT ENABLE					
1G	2	2	2	Input	Output Enable
LVC MOS CLOCK OUTPUT					
Y0	3	3	3	Output	LVC MOS output. Unused outputs can be left floating.
Y1	—	8	8		
Y2	—	5	5		
Y3	—	—	7		
SUPPLY VOLTAGE					
V _{DD}	6	6	6	Power	2.5-V or 3.3-V device supply
GROUND					
GND	4	4	4	GND	Device ground

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Supply voltage	-0.5	3.9	V
V _{IN}	Input voltage ⁽²⁾	-0.5	V _{DD} +0.5	V
V _O	Output voltage ⁽²⁾	-0.5	V _{DD} +0.5	V
I _{IN}	input current	-20	20	mA
I _O	Continuous output current	-50	50	mA
T _J	Maximum junction temperature		125	°C
T _{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) This value is limited to 3.9 V maximum.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	3.3V supply	3	3.3	3.6	V
		2.5V supply	2.3	2.5	2.7	
V _{IL}	Low-level input voltage	V _{DD} = 3.0 V to 3.6 V			V _{DD} /2 - 600	mV
		V _{DD} = 2.3 V to 2.7 V			V _{DD} /2 - 400	
V _{IH}	High-level input voltage	V _{DD} = 3.0 V to 3.6 V	V _{DD} /2 + 600			mV
		V _{DD} = 2.3 V to 2.7 V	V _{DD} /2 + 400			
V _{TH}	Input threshold voltage	V _{DD} = 2.3 V to 3.6 V	V _{DD} /2			mV
t _r / t _f	Input slew rate		1		4	V/ns
t _w	Minimum pulse width at CLKIN	V _{DD} = 3.0 V to 3.6 V	1.8			ns
		V _{DD} = 2.3 V to 2.7 V	2.75			
f _{CLK}	LVCMOS clock Input Frequency	V _{DD} = 3.0 V to 3.6 V	DC		250	MHz
		V _{DD} = 2.3 V to 2.7 V	DC		180	
T _A	Operating free-air temperature		-40		85	°C

7.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
OVERALL PARAMETERS FOR ALL VERSIONS						
I _{DD}	Static device current	1G = V _{DD} ; CLKIN = 0 V or V _{DD} ; I _O = 0 mA; V _{DD} = 3.6 V		3.5	10	mA
		1G = V _{DD} ; CLKIN = 0 V or V _{DD} ; I _O = 0 mA; V _{DD} = 2.7 V		1.5	6	
I _{PD}	Power-down current	1G = 0 V; CLKIN = 0 V or V _{DD} ; I _O = 0 mA; V _{DD} = 3.6 V or 2.7 V		34	60	μA
C _{PD}	Power dissipation capacitance per output ⁽²⁾	V _{DD} = 3.3 V; f = 10 MHz		10.7		pF
		V _{DD} = 2.5 V; f = 10 MHz		7.4		
I _I	Input leakage current at 1G	V _I = 0 or V _{DD} , V _{DD} = 3.6 V or 2.7 V		10		μA
	Input leakage current at CLKIN	V _I = 0 or V _{DD} , V _{DD} = 3.6 V or 2.7 V		28		
R _{OUT}	Output impedance	V _{DD} = 3.3 V		42		Ω
		V _{DD} = 2.5 V		49		
f _{OUT}	Output frequency	V _{DD} = 3 V to 3.6 V	DC		250	MHz
		V _{DD} = 2.3 V to 2.7 V	DC		180	
OUTPUT PARAMETERS FOR V_{DD} = 3.3 V ± 0.3 V						
V _{OH}	High-level output voltage	V _{DD} = 3 V, I _{OH} = -0.1 mA	2.9			V
		V _{DD} = 3 V, I _{OH} = -8 mA	2.5			
		V _{DD} = 3 V, I _{OH} = -12 mA	2.2			
V _{OL}	Low-level output voltage	V _{DD} = 3 V, I _{OL} = 0.1 mA			0.1	V
		V _{DD} = 3 V, I _{OL} = 8 mA			0.5	
		V _{DD} = 3 V, I _{OL} = 12 mA			0.8	
OUTPUT PARAMETERS FOR V_{DD} = 2.5 V ± 0.2 V						
V _{OH}	High-level output voltage	V _{DD} = 2.3 V, I _{OH} = -0.1 mA	2.2			V
		V _{DD} = 2.3 V, I _{OH} = -8 mA	1.7			
V _{OL}	Low-level output voltage	V _{DD} = 2.3 V, I _{OL} = 0.1 mA			0.1	V
		V _{DD} = 2.3 V, I _{OL} = 8 mA			0.5	

(1) All typical values are at respective nominal V_{DD}. For switching characteristics, outputs are terminated to 50 Ω to V_{DD}/2 (see Figure 1).

(2) This is the formula for the power dissipation calculation (see and the Power Considerations section).

$$P_{tot} = P_{stat} + P_{dyn} + P_{load} [W]$$

$$P_{stat} = V_{DD} \times I_{DD} [W]$$

$$P_{dyn} = C_{PD} \times V_{DD}^2 \times f [W]$$

$$P_{load} = C_{load} \times V_{DD}^2 \times f \times n [W]$$

n = Number of switching output pins

7.5 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
OUTPUT PARAMETERS FOR VDD = 3.3 V ± 0.3 V						
t _{PLH} / t _{PHL}	Propagation delay	CLKIN to Yn	0.8		2.0	ns
t _r / t _f	Rise and fall time	20%–80% (V _{OH} - V _{OL})	0.3		0.8	ns
t _{DIS}	Output disable time	1G to Yn			6	ns
t _{EN}	Output enable time	1G to Yn			6	ns
t _{sk(p)}	Pulse skew ; t _{PLH(Yn)} - t _{PHL(Yn)} ⁽¹⁾				180	ps
t _{jitter}	Additive jitter rms ⁽²⁾	12 kHz to 20 MHz, f _{OUT} = 250 MHz			100	fs
OUTPUT PARAMETERS FOR VDD = 2.5 V ± 0.2 V						
t _{PLH} / t _{PHL}	Propagation delay	CLKIN to Yn	1		2.6	ns
t _r / t _f	Rise and fall time	20%–80% (V _{OH} - V _{OL})	0.3		1.2	ns
t _{DIS}	Output disable time	1G to Yn			10	ns
t _{EN}	Output enable time	1G to Yn			10	ns
t _{sk(p)}	Pulse skew ; t _{PLH(Yn)} - t _{PHL(Yn)} ⁽¹⁾				220	ps
t _{jitter}	Additive jitter rms ⁽²⁾	12 kHz to 20 MHz, f _{OUT} = 180 MHz			350	fs

(1) t_{sk(p)} depends on output rise- and fall-time (t_r/t_f). The output duty-cycle can be calculated: $odc = (t_{w(OUT)} \pm t_{sk(p)}) / t_{period}$; t_{w(OUT)} is pulse-width of output waveform and t_{period} is 1/f_{OUT}.

(2) Parameter is specified by characterization. Not tested in production

7.6 Parameter Measurement Information

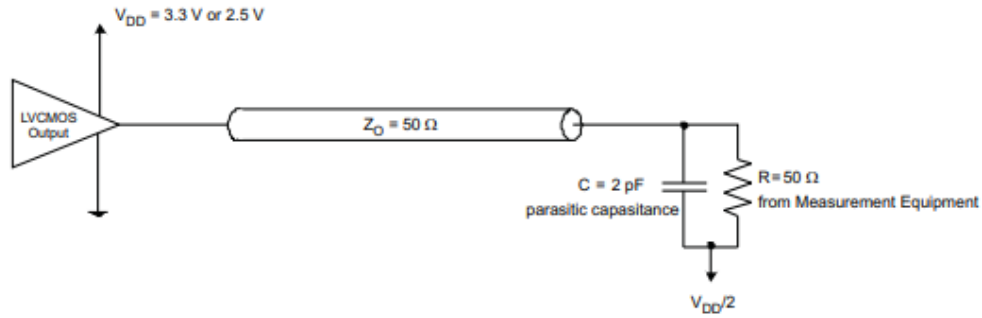


Figure 1. Test Load Circuit

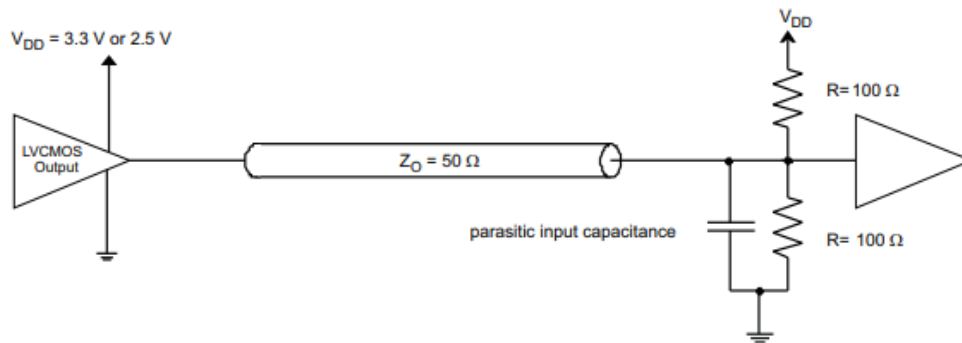


Figure 2. Application Load With 50-Ω Line Termination

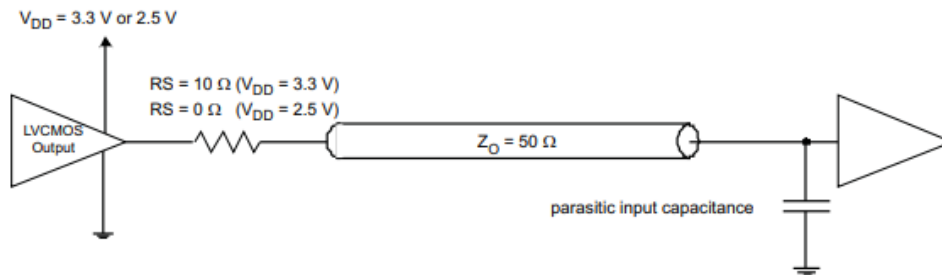


Figure 3. Application Load With Series Line Termination

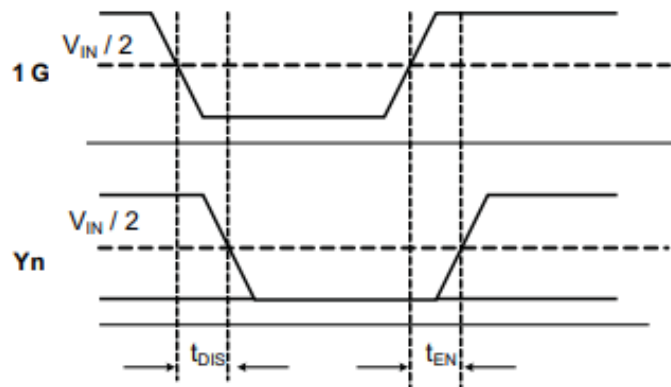
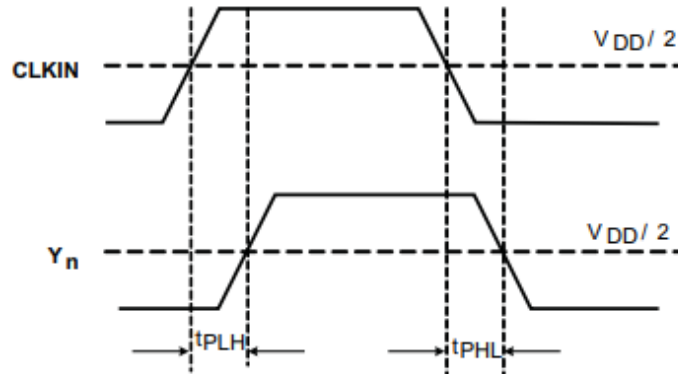


Figure 4. t_{DIS} and t_{EN} for Disable Low



Note: $t_{sk(p)} = |t_{PLH} - t_{PHL}|$

Figure 5. Pulse Skew $t_{sk(p)}$ and Propagation Delay t_{PLH}/t_{PHL}

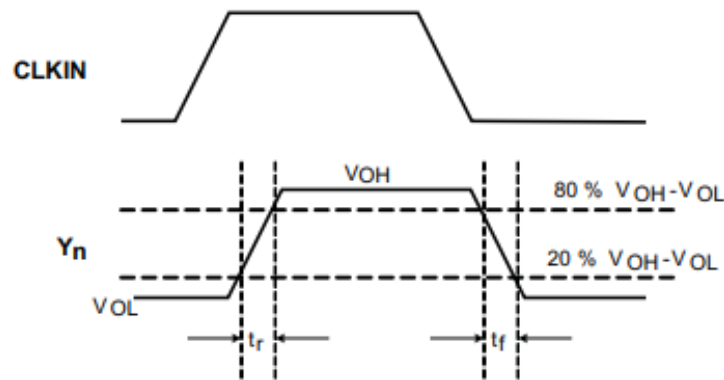


Figure 6. Rise/Fall Times t_r/t_f

8 Detailed Description

8.1 Overview

The RS911xC family of devices is a low-jitter and low-skew LVCMOS fan-out buffer solution. For best signal integrity, it is important to match the characteristic impedance of the RS911xC 's output driver with that of the transmission line. Figure 2 and Figure 3 show the proper configuration per configuration for both $V_{DD} = 3.3\text{ V}$ and $V_{DD} = 2.5\text{ V}$. RUNIC recommends placing the series resistor close to the driver to minimize signal reflection.

8.2 Functional Block Diagram

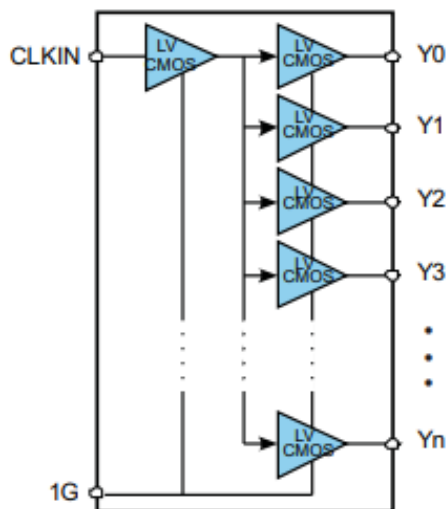


Figure 7. RS911xC functional block diagram

Table 1. Output Logic Table

INPUTS		OUTPUTS
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

8.3 Feature Description

The outputs of the RS911xC can be disabled by driving the asynchronous output enable pin (1G) low. Unused output can be left floating to reduce overall system component cost. All supply and ground pins must be connected to V_{DD} and GND, respectively.

8.4 Device Functional Modes

The RS911xC operates from supplies between 2.5 V and 3.3 V.

9 Application and Implementation

9.1 Application Information

The RS911xC family is a low additive jitter LVCMOS buffer solution that can operate up to 250 MHz at and 180 MHz at $V_{DD} = 2.5$ V. Low output skew as well as the ability for asynchronous output enable is featured to simultaneously enable or disable buffered clock outputs as necessary in the application.

9.2 Typical Application

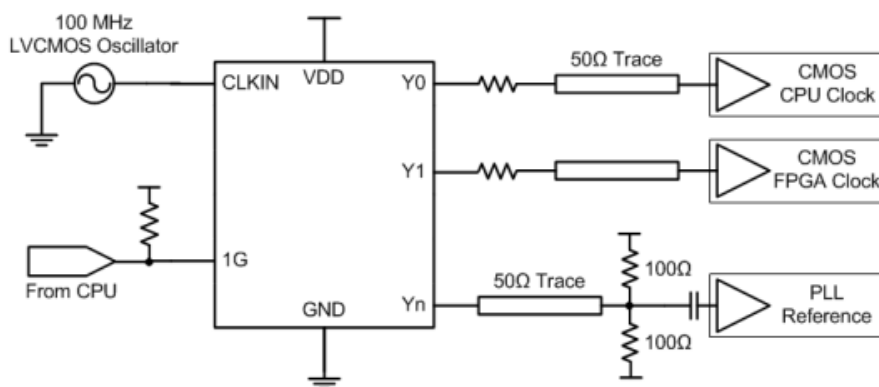


Figure 8. Example System Configuration

9.3 Design Requirements

The RS911xC shown in Figure 8 is configured to fan out a 100-MHz signal from a local LVCMOS oscillator. The CPU is configured to control the output state through 1G. The configuration example is driving three LVCMOS receivers in a backplane application with the following properties:

- The CPU clock can accept a full swing DC-coupled LVCMOS signal. A series resistor is placed near the RS911xC to closely match the characteristic impedance of the trace to minimize reflections.
- The FPGA clock is similarly DC-coupled with an appropriate series resistor placed near the RS911xC.
- The PLL in this example can accept a lower amplitude signal, so a Thevenin's equivalent termination is used. The PLL receiver features internal biasing, so AC coupling can be used when common-mode voltage is mismatched.

9.4 Detailed Design Procedure

Refer to Figure 3 and the Electrical Characteristics table to determine the appropriate series resistance needed for matching the output impedance of the RS911xC to that of the characteristic impedance of the transmission line.

Unused outputs can be left floating. See the Power Supply Recommendations section for recommended filtering techniques.

10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when the jitter and phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guards the power supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply terminals and laid out with short loops to minimize inductance. RUNIC recommends adding as many high-frequency (for example, 0.1 μF) bypass capacitors, as there are supply terminals in the package. RUNIC recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer; these beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

Figure 9 shows this recommended power supply decoupling method.

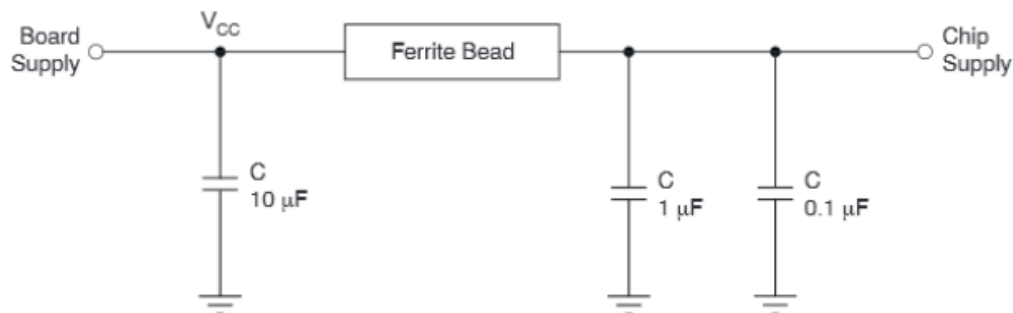


Figure 9. Power Supply Decoupling

10.1 Power Considerations

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

- Power used by the device as it switches states.
- Power required to charge any output load.

The output load can be capacitive only or capacitive and resistive. The following formula and the power graphs in and Figure 1 can be used to obtain the power consumption of the device:

$$P_{\text{dev}} = P_{\text{stat}} + n (P_{\text{dyn}} + P_{\text{Cload}})$$

$$P_{\text{stat}} = V_{\text{DD}} \times I_{\text{DD}} \quad P_{\text{dyn}} + P_{\text{Cload}}$$

where:

$$V_{\text{DD}} = \text{Supply voltage (3.3V or 2.5 V)}$$

$$I_{\text{DD}} = \text{Static device current (typical 3.5 mA for } V_{\text{DD}} = 3.3 \text{ V; typical 1.5 mA for } V_{\text{DD}} = 2.5 \text{ V)}$$

$$n = \text{Number of switching output pins}$$

Example for device power consumption for RS9114C: four outputs are switching, $f = 120 \text{ MHz}$, $V_{\text{DD}} = 3.3 \text{ V}$, and $C_{\text{load}} = 2 \text{ pF}$ per output:

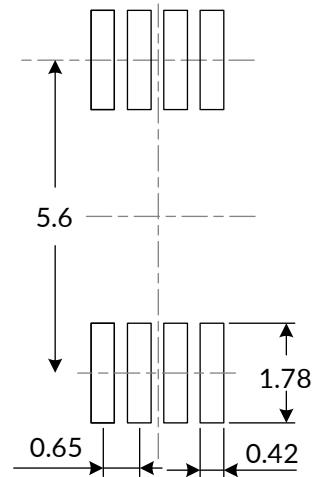
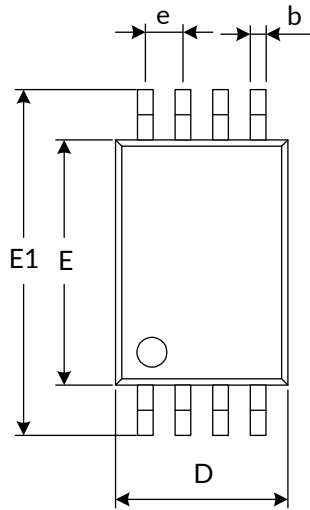
$$P_{\text{dev}} = P_{\text{stat}} + n (P_{\text{dyn}} + P_{\text{Cload}}) = 11.55 \text{ mW} + 50 \text{ mW} = 61.55 \text{ mW}$$

$$P_{\text{stat}} = V_{\text{DD}} \times I_{\text{DD}} = 3.5 \text{ mA} \times 3.3 \text{ V} = 11.55 \text{ mW}$$

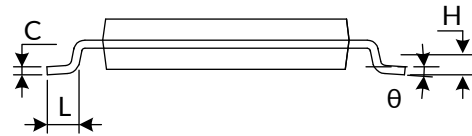
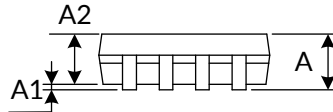
$$n (P_{\text{dyn}} + P_{\text{Cload}}) = 4 \times 12.5 \text{ mW} = 50 \text{ mW}$$

11 PACKAGE OUTLINE DIMENSIONS

TSSOP8⁽³⁾



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D ⁽¹⁾	2.900	3.100	0.114	0.122
E ⁽¹⁾	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650(BSC) ⁽²⁾		0.026(BSC) ⁽²⁾	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.