

2-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation and 3-State Outputs

1 FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the Grade 1**
- **Control Input threshold Referenced to V_{CCA} Voltage**
- **Power-Supply Range:**
 V_{CCA} and V_{CCB} : 1.65V to 5.5V
- **V_{CC} Isolation: If Either V_{CC} is at GND, Both Ports are in the High-Impedance State**
- **Low power consumption, 4 μ A Max**
- **Output drive up to ± 24 mA @ 3.0V**
- **No Power-Supply Sequencing Required: Either V_{CCA} or V_{CCB} can be Ramped First**
- **I_{OFF} : Supports Partial-Power-Down Mode Operation**
- **Extended Temperature: -40°C to +125°C**

2 APPLICATIONS

- **Automotive Infotainment**
- **Advance Driver Assistance Systems (ADAS)**
- **Telematics**
- **Navigation Systems**
- **Cluster**

3 DESCRIPTIONS

The RS2T45-Q1 is 2-bit non-inverting bus transceiver uses two separate configurable power supply rails. The A port and DIR are designed to track V_{CCA} , which supporting operating voltages from 1.65V to 5.5V, and the B port supporting operating voltages from 1.65V to 5.5V while it tracks the V_{CCB} supply. This allows for universal low-voltage bidirectional translation between any of the 1.8V, 2.5V, 3.3V and 5V voltage nodes.

The RS2T45-Q1 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry is always active on both A and B ports and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ} .

The RS2T45-Q1 is available in Green VSSOP-8 packages. It operates over an ambient temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE(NOM)
RS2T45-Q1	VSSOP-8	2.00mmx2.30mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Functional Block Diagram

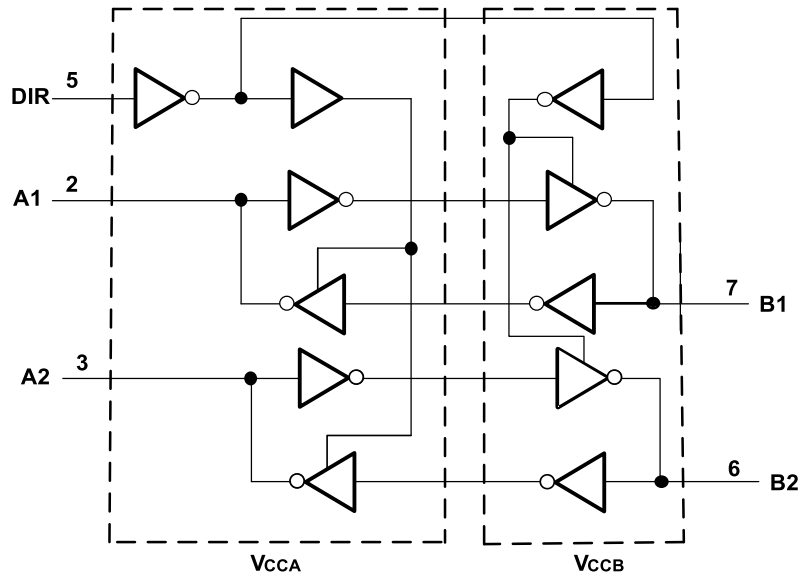


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5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2023/06/16	Initial version completed

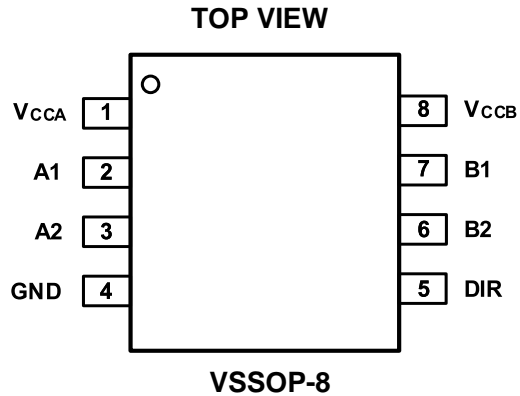
6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	PACKAGE LEAD	TEMPERATURE RANGE	Lead finish/Ball material (2)	MSL Peak Temp (3)	PACKAGE MARKING (4)	PACKAGE OPTION
RS2T45 -Q1	RS2T45XVS8 -Q1	VSSOP-8	-40°C ~+125°C	NIPDAUAG	MSL1-260° -Unlimited	2T45	Tape and Reel,3000

NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (3) MSL Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

7 PIN CONFIGURATIONS



7.1 PIN DESCRIPTION

PIN	NAME	TYPE ⁽¹⁾	FUNCTION
VSSOP-8			
1	V _{CCA}	P	A Port Supply Voltage. $1.65V \leq V_{CCA} \leq 5.5V$
2	A1	I/O	Input/output A1. Reference to V _{CCA} .
3	A2	I/O	Input/output A2. Reference to V _{CCA} .
4	GND	–	Ground.
5	DIR	I	Direction control. Referenced to V _{CCA} .
6	B2	I/O	Input/output B2. Reference to V _{CCB} .
7	B1	I/O	Input/output B1. Reference to V _{CCB} .
8	V _{CCB}	P	B Port Supply Voltage. $1.65V \leq V_{CCB} \leq 5.5V$.

(1) I=input, O=output, I/O=input and output, P=power.

7.2 Function Table ⁽²⁾

CONTROL INPUTS ⁽¹⁾	OUTPUT CIRCUITS		OPERATION
DIR	A PORT	B PORT	
L	Enabled	Hi-Z	B data to A bus
H	Hi-Z	Enabled	A data to B bus

Note:

(1) The input circuit of the data I/O is always active.

(2) When either V_{CCA} or V_{CCB} is at GND level, the device goes into suspend mode.

(3) H=High voltage level, L=Low voltage level, X=don't care, Z=high-impedance OFF-state.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

SYMBOL	PARAMETER		MIN	MAX	UNIT
V _{CCA} ⁽³⁾	Supply Voltage Range		-0.5	6.5	V
V _{CCB} ⁽³⁾	Supply Voltage Range		-0.5	6.5	V
V _I ⁽²⁾	Input Voltage Range	A port	-0.5	6.5	V
		B port	-0.5	6.5	
V _O ⁽²⁾	Voltage range applied to any output in the high-impedance or power-off state	A port	-0.5	V _{CCA} +0.5	V
		B port	-0.5	V _{CCB} +0.5	
I _{IK}	Input clamp current	V _I <0		-50	mA
I _{OK}	Output clamp current	V _O <0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CCA} , V _{CCB} or GND			±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	VSSOP-8		205	K/W
T _J	Junction Temperature ⁽⁵⁾		-40	150	°C
T _{stg}	Storage temperature		-65	+150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged-Device Model (CDM), per AEC Q100-011	±500	
		Latch-Up (LU), per AEC Q100-004	±100	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

PARAMETER		$V_{CCI}^{(1)}$	$V_{CCO}^{(2)}$	MIN	TYP	MAX	UNIT
Supply voltage ⁽¹⁾	V_{CCA}			1.65		5.5	V
	V_{CCB}			1.65		5.5	
High-level input Voltage (V_{IH})	A&B-port I/Os ⁽⁵⁾	1.65V to 1.95V		$V_{CCI} \times 0.75$			V
		2.3V to 2.7V		$V_{CCI} \times 0.7$			
		3V to 3.6V		$V_{CCI} \times 0.7$			
		4.5V to 5.5V		$V_{CCI} \times 0.7$			
Low-level input Voltage (V_{IL})	A&B-port I/Os ⁽⁵⁾	1.65V to 1.95V				$V_{CCI} \times 0.35$	V
		2.3V to 2.7V				$V_{CCI} \times 0.3$	
		3V to 3.6V				$V_{CCI} \times 0.3$	
		4.5V to 5.5V				$V_{CCI} \times 0.3$	
High-level input Voltage (V_{IH})	DIR (referenced to V_{CCA}) ⁽⁶⁾	1.65V to 1.95V		$V_{CCA} \times 0.75$			V
		2.3V to 2.7V		$V_{CCA} \times 0.7$			
		3V to 3.6V		$V_{CCA} \times 0.7$			
		4.5V to 5.5V		$V_{CCA} \times 0.7$			
Low-level input Voltage (V_{IL})	DIR (referenced to V_{CCA}) ⁽⁶⁾	1.65V to 1.95V				$V_{CCA} \times 0.35$	V
		2.3V to 2.7V				$V_{CCA} \times 0.3$	
		3V to 3.6V				$V_{CCA} \times 0.3$	
		4.5V to 5.5V				$V_{CCA} \times 0.3$	
V_I	Input voltage ⁽⁴⁾			0		5.5	V
V_O	Output voltage			0		V_{CCO}	V
High-level output current (I_{OH})		1.65V to 1.95V				-4	mA
		2.3V to 2.7V				-8	
		3V to 3.6V				-24	
		4.5V to 5.5V				-32	
Low-level output current (I_{OL})		1.65V to 1.95V				4	mA
		2.3V to 2.7V				8	
		3V to 3.6V				24	
		4.5V to 5.5V				32	
Input transition rise or fall rate ($\Delta t/\Delta v$)	Data inputs ⁽³⁾	1.65V to 1.95V				20	ns/V
		2.3V to 2.7V				20	
		3V to 3.6V				10	
		4.5V to 5.5V				5	
	Control input	1.65 V to 5.5 V				5	
T_A Operating free-air temperature				-40		125	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power.

(4) All unused control inputs must be held at V_{CCA} or GND to ensure proper device operation and minimize power consumption.

(5) For V_{CCI} values not specified in the data sheet, $V_{IH} \text{ min} = V_{CCI} \times 0.7 \text{ V}$, $V_{IL} \text{ max} = V_{CCI} \times 0.3 \text{ V}$.

(6) For V_{CCA} values not specified in the data sheet, $V_{IH} \text{ min} = V_{CCA} \times 0.7 \text{ V}$, $V_{IL} \text{ max} = V_{CCA} \times 0.3 \text{ V}$.

8.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) ^{(1) (2)}

PARAMETER		CONDITIONS	V _{CCA}	V _{CCB}	TEMP	MIN ⁽³⁾	TYP ⁽⁴⁾	MAX ⁽³⁾	UNIT	
V _{OH}		I _{OH} = -100 μA V _I = V _{IH}	1.65V to 4.5V	1.65V to 4.5V	Full	V _{CCO} - 0.1			V	
		I _{OH} = -4mA V _I = V _{IH}	1.65V	1.65V		1.2				
		I _{OH} = -8mA V _I = V _{IH}	2.3V	2.3V		1.9				
		I _{OH} = -24mA V _I = V _{IH}	3V	3V		2.4				
		I _{OH} = -32mA V _I = V _{IH}	4.5V	4.5V		3.8				
V _{OL}		I _{OL} = 100 μA V _I = V _{IL}	1.65V to 4.5V	1.65V to 4.5V					0.1	V
		I _{OL} = 4mA V _I = V _{IL}	1.65V	1.65V					0.45	
		I _{OL} = 8mA V _I = V _{IL}	2.3V	2.3V					0.3	
		I _{OL} = 24mA V _I = V _{IL}	3V	3V					0.55	
		I _{OL} = 32mA V _I = V _{IL}	4.5V	4.5V					0.55	
I _I	DIR Input leakage current	V _I = V _{CCA} or GND	1.65V to 5.5V	1.65V to 5.5V	+25°C			±1	μA	
					Full			±2		
I _{off}	A or B Port	V _I or V _O = 0 to 5.5V	0V	0V to 5.5V	+25°C			±1	μA	
			0V to 5.5V	0V	Full			±2		
I _{OZ} ⁽⁵⁾	A or B Port	V _O = V _{CCO} or GND	1.65V to 5.5V	1.65V to 5.5V	+25°C			±1	μA	
					Full			±2		
I _{CCA}	V _{CCA} supply current	V _I = V _{CCI} or GND ⁽⁶⁾ I _O = 0	1.65V to 5.5V	2.3V to 5.5V	Full			3	μA	
			5V	0V	Full			2		
			0V	5.5V	Full			-2		
I _{CCB}	V _{CCB} supply current	V _I = V _{CCI} or GND I _O = 0	1.65V to 5.5V	1.65V to 5.5V	Full			3	μA	
			5V	0V	Full			-2		
			0V	5V	Full			2		
I _{CCA} + I _{CCB}	Combined supply current	V _I = V _{CCI} or GND I _O = 0	1.65V to 5.5V	1.65V to 5.5V	Full			5	μA	
ΔI _{CCA}	A port	One A port at V _{CCA} - 0.6 V, DIR at V _{CCA} , B port = open	3V to 5.5V	3V to 5.5V	Full			50	μA	
	DIR	DIR at V _{CCA} - 0.6V, B port = open, A port at V _{CCA} or GND			Full			50		
ΔI _{CCB}	B port	One B port at V _{CCB} - 0.6 V, DIR at GND, A port = open	3V to 5.5V	3V to 5.5V	Full			50	μA	
C _I	Input capacitance	DIR input V _I = V _{CCA} or GND	3.3V	3.3V	+25°C		4		pF	
C _{IO}	Input-to-output internal capacitance	A port V _O = V _{CCA} or GND	3.3V	3.3V	+25°C		8.5		pF	
		B port V _O = V _{CCB} or GND	3.3V	3.3V	+25°C		8.5			

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(5) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(6) Hold all unused data inputs of the device at V_{CCI} or GND to assure proper device operation.

8.5 Timing Requirements

8.5.1 $V_{CCA}=1.8V\pm 0.15V$

over recommended operating free-air temperature range, Full=-40°C to 125°C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	$V_{CCB}=1.8V \pm 0.15V^{(1)}$		$V_{CCB}=2.5V \pm 0.2V^{(1)}$		$V_{CCB}=3.3V \pm 0.3V^{(1)}$		$V_{CCB}=5V \pm 0.5V^{(1)}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	Full	3.5	24.6	2.6	17.2	2.0	18.6	1.6	18.5	ns
t_{PHL}			Full	3.3	18.4	2.6	15.5	2.1	16.4	2.0	16.8	
t_{PLH}	B	A	Full	3.5	24.6	2.7	24.5	2.5	23.2	2.2	23.2	ns
t_{PHL}			Full	3.3	18.4	2.5	18.4	2.4	15.3	2.1	14.1	
t_{PHZ}	DIR	A	Full	6.2	33.9	5.7	37.1	5.6	32.3	6.1	31.9	ns
t_{PLZ}			Full	2.7	35.9	2.5	37.3	2.8	17.8	3.7	41.7	
t_{PHZ}	DIR	B	Full	8.8	33.9	5.8	30.0	4.3	33.2	2.7	34.6	ns
t_{PLZ}			Full	5.0	35.9	2.6	23.6	2.7	22.4	2.4	22.2	
$t_{PZH}^{(2)}$	DIR	A	Full		60.5		48.1		45.6		45.4	ns
$t_{PZL}^{(2)}$			Full		52.3		48.4		48.5		48.7	
$t_{PZH}^{(2)}$	DIR	B	Full		60.5		54.5		36.4		60.2	ns
$t_{PZL}^{(2)}$			Full		52.3		52.6		48.7		48.7	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

(2) The enable time is a calculated value, derived using the formula shown in Enable Times.

8.5.2 $V_{CCA}=2.5V\pm 0.2V$

over recommended operating free-air temperature range, Full=-40°C to 125°C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	$V_{CCB}=1.8V \pm 0.15V^{(1)}$		$V_{CCB}=2.5V \pm 0.2V^{(1)}$		$V_{CCB}=3.3V \pm 0.3V^{(1)}$		$V_{CCB}=5V \pm 0.5V^{(1)}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	Full	2.7	24.5	1.8	16.5	1.5	15.4	1.3	16.6	ns
t_{PHL}			Full	2.5	18.4	1.6	12.7	1.5	11.3	1.0	10.4	
t_{PLH}	B	A	Full	2.6	17.2	1.8	16.5	1.6	16.2	1.2	16.2	ns
t_{PHL}			Full	2.6	15.5	1.6	12.7	1.5	12.5	1.0	11.4	
t_{PHZ}	DIR	A	Full	3.6	30.0	2.5	32.8	2.7	33.2	3.8	32.4	ns
t_{PLZ}			Full	1.5	23.6	1.5	25.7	1.5	14.8	1.2	18.1	
t_{PHZ}	DIR	B	Full	7.8	37.1	4.9	32.8	3.6	33.2	2.2	34.3	ns
t_{PLZ}			Full	4.2	37.3	2.6	25.7	3.0	26.4	1.9	26.4	
$t_{PZH}^{(2)}$	DIR	A	Full		54.5		42.2		42.6		42.6	ns
$t_{PZL}^{(2)}$			Full		52.6		45.5		45.7		45.7	
$t_{PZH}^{(2)}$	DIR	B	Full		48.1		42.2		30.2		34.7	ns
$t_{PZL}^{(2)}$			Full		48.4		45.5		44.5		42.8	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

(2) The enable time is a calculated value, derived using the formula shown in Enable Times.

8.5.3 $V_{CCA}=3.3V\pm 0.3V$

over recommended operating free-air temperature range, Full=-40°C to 125°C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	$V_{CCB}=1.8V \pm 0.15V^{(1)}$		$V_{CCB}=2.5V \pm 0.2V^{(1)}$		$V_{CCB}=3.3V \pm 0.3V^{(1)}$		$V_{CCB}=5V \pm 0.5V^{(1)}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	Full	2.5	23.2	1.6	16.2	0.8	15.2	0.8	15.1	ns
t_{PHL}			Full	2.4	15.3	1.5	12.5	0.9	10.2	0.8	10.0	
t_{PLH}	B	A	Full	2.0	18.6	1.5	15.4	0.8	15.2	0.7	15.8	ns
t_{PHL}			Full	2.1	16.4	1.5	11.3	0.9	10.2	0.8	10.4	
t_{PHZ}	DIR	A	Full	2.7	33.2	2.8	33.2	1.8	34.3	2.8	32.8	ns
t_{PLZ}			Full	2.1	22.4	1.9	26.4	2.2	15.1	2.4	19.5	
t_{PHZ}	DIR	B	Full	6.4	32.3	4.6	33.2	3.4	34.3	2.0	34.1	ns
t_{PLZ}			Full	2.7	17.8	2.5	14.8	2.8	15.1	1.8	14.8	
$t_{PZH}^{(2)}$	DIR	A	Full	36.4		30.2		30.3		30.6		ns
$t_{PZL}^{(2)}$			Full	48.7		44.5		44.5		44.5		
$t_{PZH}^{(2)}$	DIR	B	Full	45.6		42.6		30.3		34.6		ns
$t_{PZL}^{(2)}$			Full	48.5		45.7		44.5		42.8		

(1) This parameter is ensured by design and/or characterization and is not tested in production.

(2) The enable time is a calculated value, derived using the formula shown in Enable Times.

8.5.4 $V_{CCA}=5V\pm 0.5V$

over recommended operating free-air temperature range, Full=-40°C to 125°C.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMP	$V_{CCB}=1.8V \pm 0.15V^{(1)}$		$V_{CCB}=2.5V \pm 0.2V^{(1)}$		$V_{CCB}=3.3V \pm 0.3V^{(1)}$		$V_{CCB}=5V \pm 0.5V^{(1)}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	Full	2.2	23.2	1.2	16.2	0.7	15.8	0.6	15.2	ns
t_{PHL}			Full	2.1	14.1	1.0	11.4	0.8	10.4	0.6	9.5	
t_{PLH}	B	A	Full	1.6	18.5	1.3	16.6	0.8	15.1	0.6	15.2	ns
t_{PHL}			Full	2.0	16.8	1.0	10.4	0.8	10.0	0.6	9.5	
t_{PHZ}	DIR	A	Full	2.5	34.6	2.4	34.3	2.6	34.1	2.4	33.4	ns
t_{PLZ}			Full	1.0	22.2	1.2	26.4	1.2	14.8	1.0	19.0	
t_{PHZ}	DIR	B	Full	5.7	31.9	3.0	32.4	1.2	32.8	2.0	33.4	ns
t_{PLZ}			Full	3.1	41.7	2.4	18.1	3.0	19.5	1.9	19.0	
$t_{PZH}^{(2)}$	DIR	A	Full	60.2		34.7		34.6		34.2		ns
$t_{PZL}^{(2)}$			Full	48.7		42.8		42.8		42.9		
$t_{PZH}^{(2)}$	DIR	B	Full	45.4		42.6		30.6		34.2		ns
$t_{PZL}^{(2)}$			Full	48.7		45.7		44.5		42.9		

(1) This parameter is ensured by design and/or characterization and is not tested in production.

(2) The enable time is a calculated value, derived using the formula shown in Enable Times.

8.6 Operating Characteristics

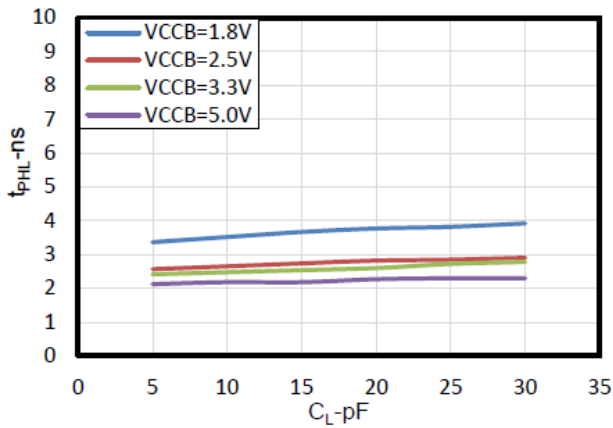
 $T_A=25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CCA}=$ $V_{CCB}=1.8\text{V}$	$V_{CCA}=$ $V_{CCB}=2.5\text{V}$	$V_{CCA}=$ $V_{CCB}=3.3\text{V}$	$V_{CCA}=$ $V_{CCB}=5\text{V}$	UNIT
			TYP	TYP	TYP	TYP	
$C_{pdA}^{(1)}$	A-port input, B-port output	$C_L=0,$ $f=10\text{MHz},$ $t_r=t_f=5\text{ns}$	3	4	6	9	pF
	B-port input, A-port output		14	17	22	32	
$C_{pdB}^{(1)}$	A-port input, B-port output		14	16	21	32	
	B-port input, A-port output		3	4	6	9	

(1) Power dissipation capacitance per transceiver.

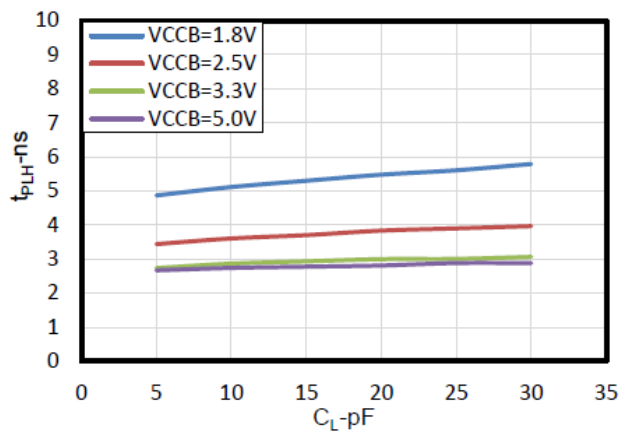
8.7 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.



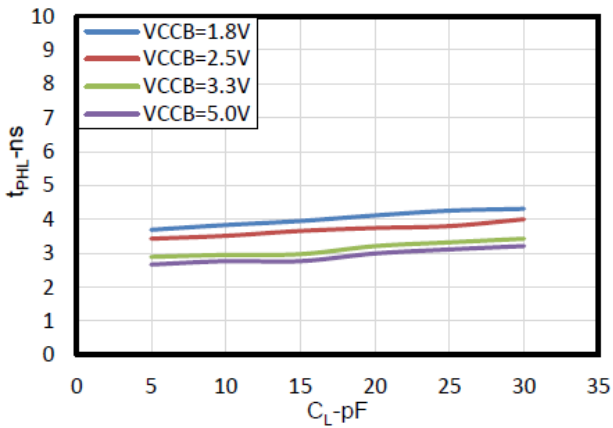
$T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

Figure 1. Typical Propagation Delay High-to-Low (A to B) vs Load Capacitance



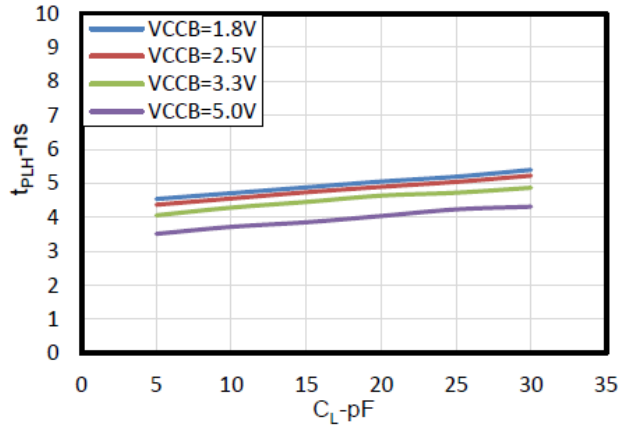
$T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

Figure 2. Typical Propagation Delay Low-to-High (B to A) vs Load Capacitance



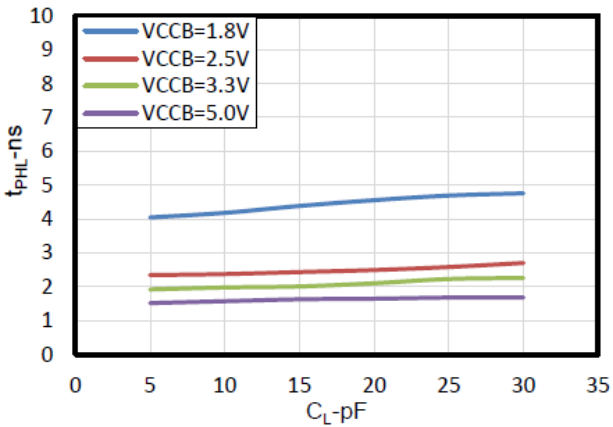
$T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

Figure 3. Typical Propagation Delay High-to-Low (A to B) vs Load Capacitance



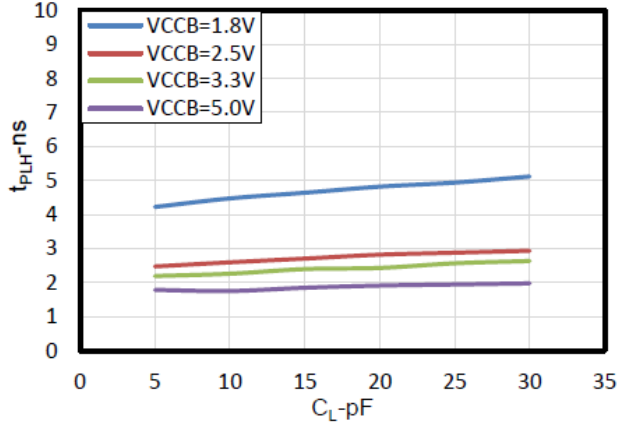
$T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

Figure 4. Typical Propagation Delay Low-to-High (B to A) vs Load Capacitance



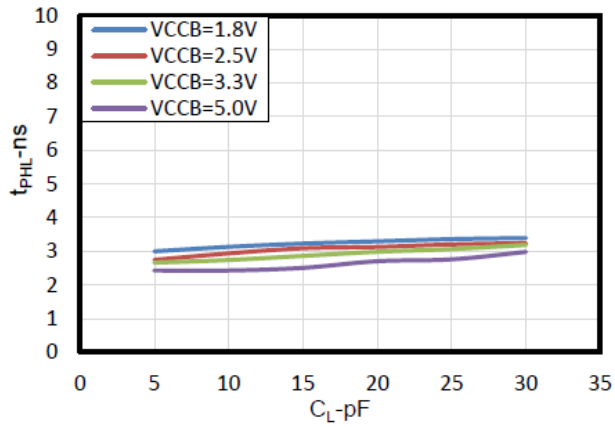
$T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

Figure 5. Typical Propagation Delay High-to-Low (A to B) vs Load Capacitance



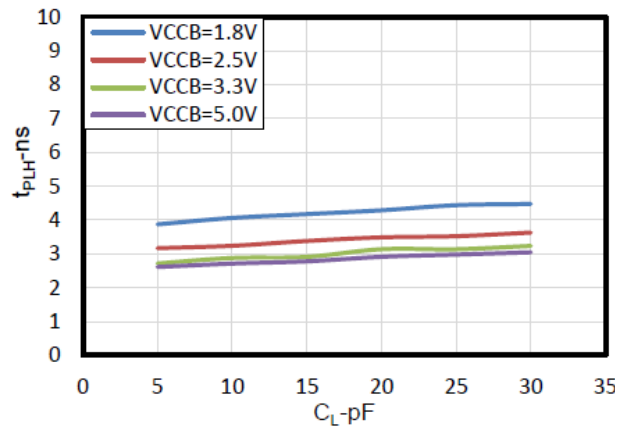
$T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

Figure 6. Typical Propagation Delay Low-to-High (B to A) vs Load Capacitance



T_A = 25°C, V_{CCA} = 5 V

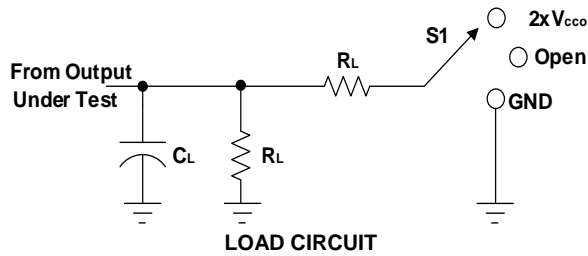
Figure 7. Typical Propagation Delay High-to-Low (A to B) vs Load Capacitance



T_A = 25°C, V_{CCA} = 5 V

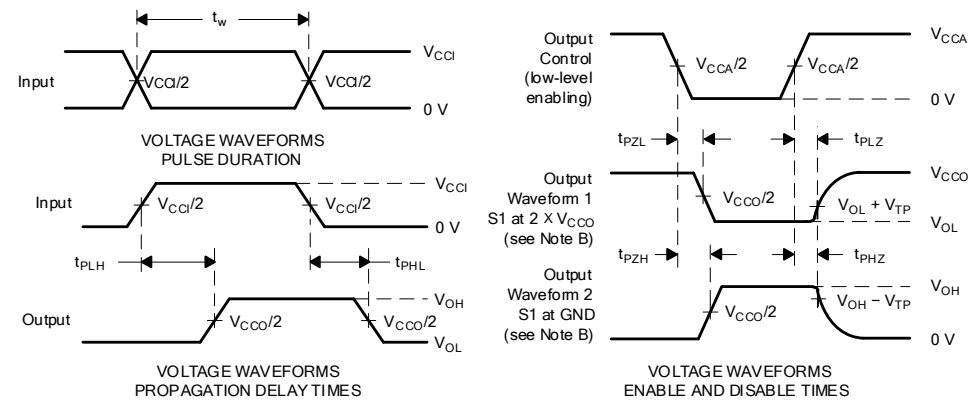
Figure 8. Typical Propagation Delay Low-to-High (B to A) vs Load Capacitance

9 Parameter Measurement Information



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 X V_{CCO}
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{TP}
$1.8V \pm 0.15V$	15pF	2k Ω	0.15V
$2.5V \pm 0.2V$	15pF	2k Ω	0.15V
$3.3V \pm 0.3V$	15pF	2k Ω	0.3V
$5V \pm 0.5V$	15pF	2k Ω	0.3V



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1V/ns$.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

H. V_{CCi} is the V_{CC} associated with the input port.

I. All parameters and waveforms are not applicable to all devices.

Figure 9. Load Circuit and Voltage Waveforms

10 Application and Implementation

Information in the following applications sections is not part of the Runic component specification, and Runic does not warrant its accuracy or completeness. Runic's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The RS2T45-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum output current can be up to 32 mA when device is powered by 5 V.

10.1.1 Enable Times

Calculate the enable times for the RS2T45-Q1 using the following formulas:

- $t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)}$
- $t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)}$
- $t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)}$
- $t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the RS2T45-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

10.2 Typical Application

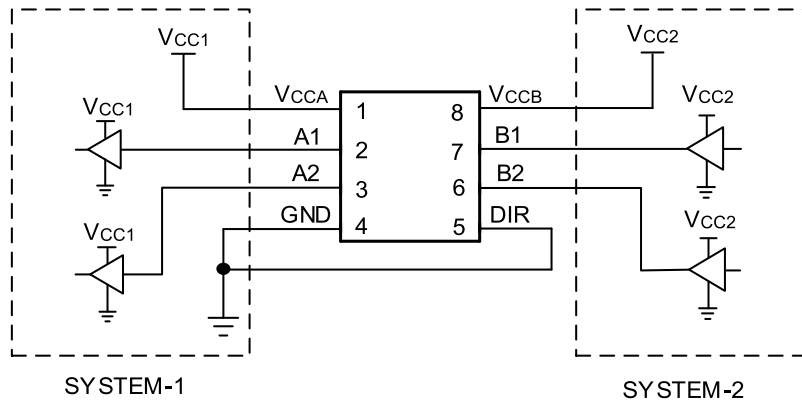


Figure 10. Unidirectional Logic Level-Shifting Application (B to A)

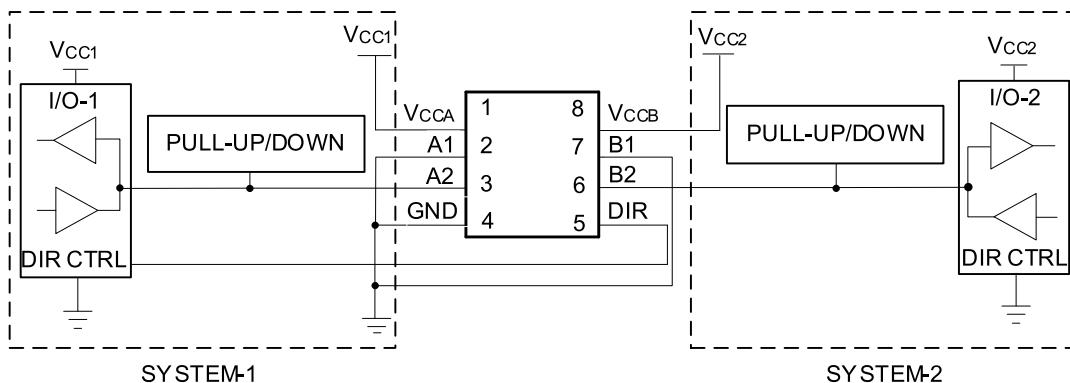


Figure 11. Bidirectional Logic Level-Shifting Application (B to A or A to B)

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

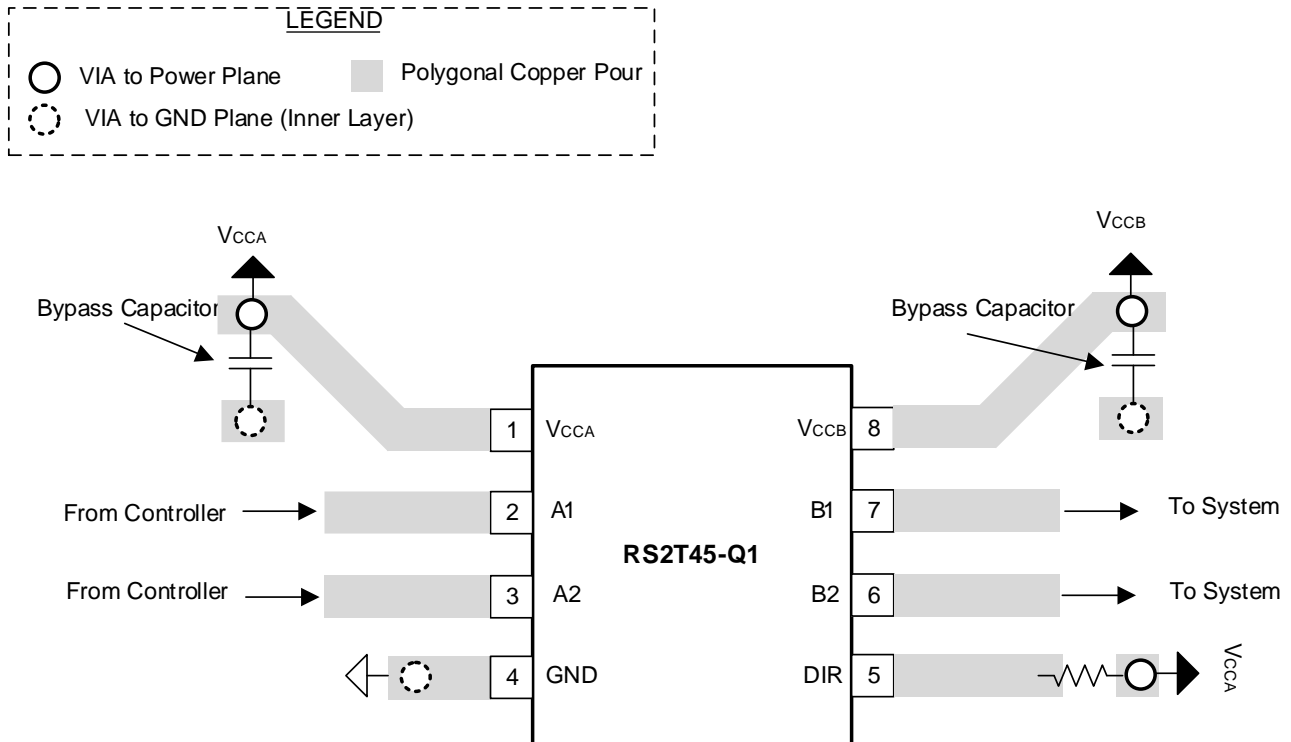
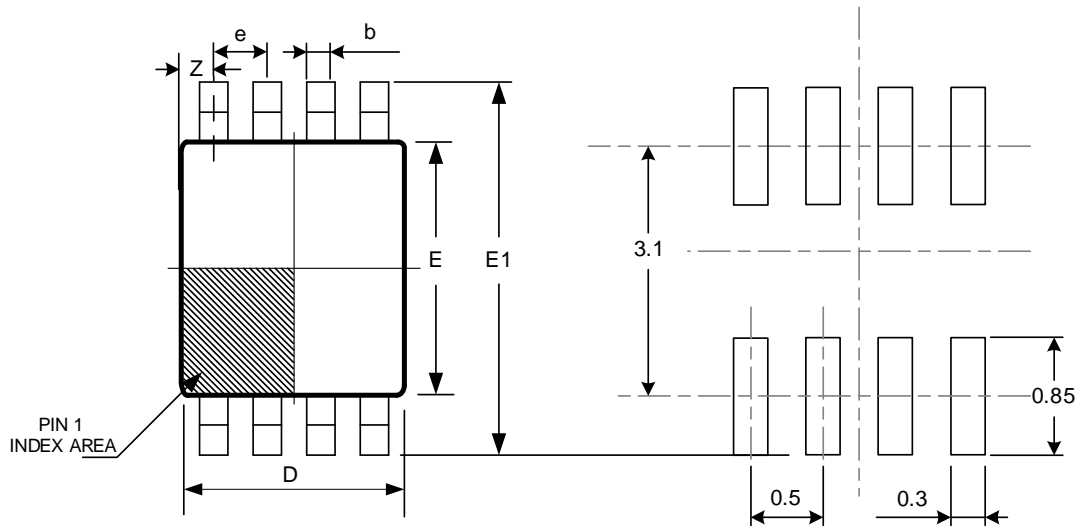
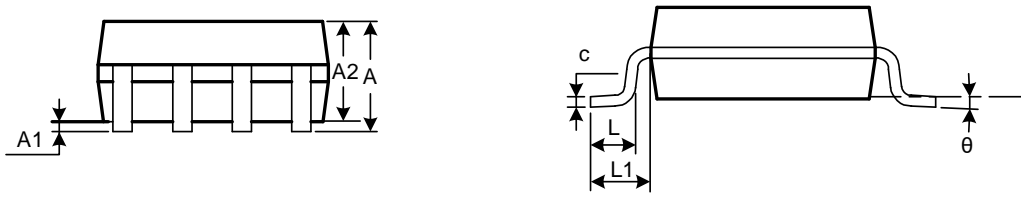


Figure 12. Layout Example

12 PACKAGE OUTLINE DIMENSIONS

VSSOP-8


RECOMMENDED LAND PATTERN (Unit: mm)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		0.100		0.004
A1	0.000	0.150	0.000	0.006
A2	0.600	0.850	0.023	0.034
b	0.170	0.270	0.007	0.010
c	0.080	0.230	0.003	0.009
D	1.900	2.100	0.075	0.083
e	0.500 (BSC)		0.020 (BSC)	
E	2.200	2.400	0.087	0.095
E1	3.000	3.200	0.118	0.126
L	0.150	0.400	0.006	0.016
L1	0.400 (BSC)		0.016 (BSC)	
Z	0.100	0.400	0.004	0.016
θ	0°	8°	0°	8°

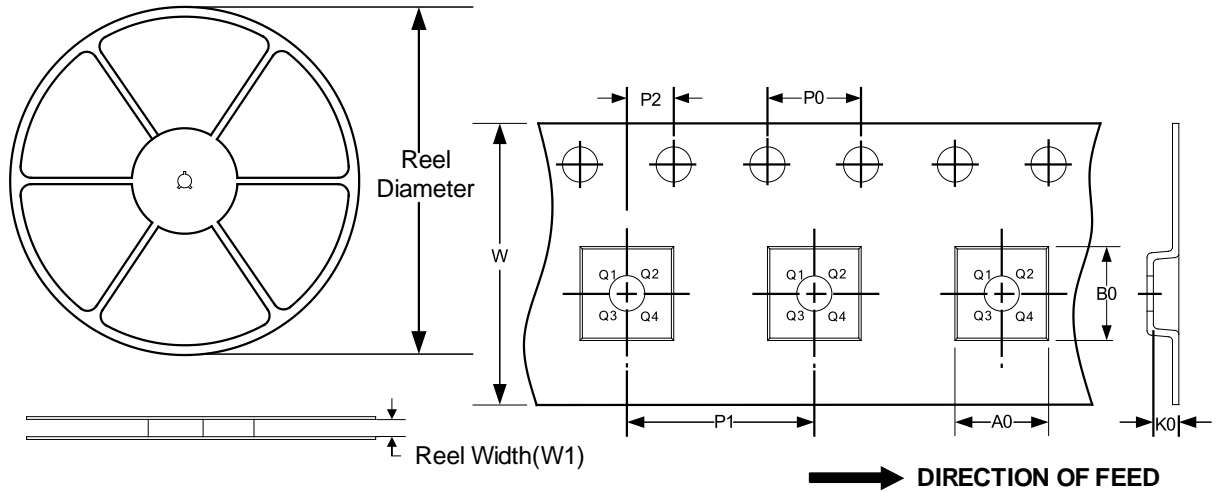
NOTE:

- A. All linear dimension is in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
VSSOP-8	7"	9.5	2.25	3.35	1.40	4.0	4.0	2.0	8.0	Q3

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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